Effects of corner angle of trapezoidal and triangular channel cross-sections on electrical performance of silicon nanowire field-effect transistors with semi gate-around structure

Soshi Sato[1*], Kuniyuki Kakushima[2], Parhat Ahmet[1], Kenji Ohmori[3], Kenji Natori[1], Keisaku Yamada[3], and Hiroshi Iwai[1].

[1] Frontier Research Center, Tokyo Institute of Technology, 4259-S2-20, Nagatsuta-cho, Midori-ku, Yokohama, 206-8502 Japan.

[2] Interdisciplinary Graduate School of Science and Engineering, Tokyo Institute of Technology, 4259-S2-20, Nagatsuta-cho, Midori-ku, Yokohama, 206-8502 Japan.

[3] Institute of Applied Science and Physics, University of Tsukuba, 1-1-1 Tennodai, Ibaraki, 305-8573 Japan.

*Corresponding author

e-mail: sato@iwailab.ep.titech.ac.jp Tel: +81-45-924-5847; Fax: +81-45-924-5846

Abstract

Structural effects, especially corner angle of upper-corners of trapezoidal and rectangular, and triangular cross-sectional shapes of silicon nanowire field-effect transistors on effective carrier mobility and normalized inversion charge density have been investigated. <100>-directed silicon nanowire field-effect transistors with semi-gate around structure fabricated on (100)-oriented silicon-on-insulator wafers were evaluated. As the upper-corner angle decreased from obtuse to acute angle, we observed an increased amount of inversion charge using split-CV measurement. On the other hand, the effective carrier mobility dependence on the upper-corner angle seems to have an optimized point near 100^{o} at 296 K. Although normalized inversion charge density was the largest with acute angles, effective carrier mobility with acute upper-corner angle was severely degraded. Considering the intrinsic delay time of SiNW FET, SiNW FETs with trapezoidal cross-section with upper-corner angle of 100^{o} is more suitable in this work to achieve high electrical performance. We believe these findings could represent guidelines for the design of high-performance SiNW FETs.

1. Introduction

Silicon nanowire (SiNW) field-effect transistors (FETs) attract much attention as an ultimate structure at the end of the scaling of complementary metal-oxide-silicon (CMOS) technology. This is mainly due to their excellent normalized on-current (I_{ON}) with steep normalized off-current (I_{OFF}) by superior electrostatic controllability to channel. A promising application represents low power consumption devices by reduction of power supply voltages, which can be realized due to the superiority of the I_{ON} of SiNW FETs.

Many fabrication processes of the SiNW channel have been proposed with a top-down approach [1, 2]. The cross-sectional shapes of the SiNW channel depend on the initial shape and dimensions of silicon fins and additional thermal oxidation process conditions [3]. The initial shape is usually rectangular and can be modified with anisotropic dry etching with SiN hard mask [4]. Oxidation temperature, time, dopant concentration and ambient (dry or wet) affect the cross-sectional shape of the fabricated SiNW because stress in sacrificial silicon oxide, which surrounds the SiNW channel during the process, is highly significant for determining the cross-sectional shape of the SiNW channel [5]. The oxidation process predominantly employs stress-limited oxidation [6] for the fabrication of the narrow SiNW channels. A problem of the top-down process is the line edge roughness (LER) of the SiNW channel. Therefore, smoothing technologies, such as hydrogen annealing [7] and hydrogen thermal etching [8], have also been proposed for rounding the SiNW channel or etching the LER of the SiNW channel. As a result, there exist various cross-sectional shapes of the SiNW channels: triangular [2, 4], circular [1], ellipsoidal [9], and rectangular [10]. The effects of the various cross-sectional shapes of the SiNW FETs on their electrical properties have been reported, for example, the gate capacitance [11], the on-current I_{ON} [12], the threshold voltage (V_{th}) [13], the effective carrier mobility (μ_{eff}) [14], and the interfacial state density (D_{it}) [15]. However, the number of reports on the analysis of electrical characteristics dependence on the cross-sectional shape is smaller than that of the reports on device fabrication processes.

In this work, we fabricated <100>-directed SiNW FETs with triangular, trapezoidal and rectangular cross-sections with semi gate-around structure [16] on (100)-oriented silicon-on-insulator wafers. We electrically characterized the FETs focusing on the angle θ of the upper-corner of the channel cross-section of the SiNW channel, which has corners with acute and obtuse angles. We found a monotonic relationship between the corner angle θ and $Q_{inv.}$ The relationship between μ_{eff} and θ have an optimized point near 100^{o}. We speculated that the acute angle in the channel cross-section degrades the effective carrier mobility because of severe surface roughness scattering.

2. Experiments

<100>-directed SiNW FETs and planar SOI FETs were fabricated simultaneously on (100)-oriented silicon-on-insulator (SOI) wafers with (*i*) a SOI layer thickness of 50 nm and buried oxide (BOX) layer thickness of 145 nm, and (*ii*) 75 nm of SOI layer and 50 nm of BOX layer, and (*iii*) 61 nm of SOI layer and 145 nm of BOX layer. We used p-type SOI wafers with resistivity of 10 Ω−cm. The dopant concentration in SiNW channel was nearly 1×10^{17} cm^{-3}. After thinning of the SOI layer by sacrificial oxidation, mesa-type Si fin structures with embedded source/drain (S/D) pads were fabricated with lithography and dry etching process with a silicon nitride (SiN) hard mask deposited by low-pressure chemical-vapor deposition method (LP-CVD) using dichlorosilane (DCS) with a thickness of 50 nm for (*i*) and (*ii*), and with a silicon oxide hard mask with a thickness of 30 nm deposited by CVD method with tetraethylorthosilicate (TEOS) for (*iii*), followed by a sacrificial oxidation process in dry oxygen ambient for 1 hour at 1000 ^{o}C. A tri-gate-like semi gate-around structure [16] with a gate oxide (SiO_2) thickness (T_{ox}) of 3 nm (except the sample (f) with T_{ox} of 5 nm) and poly-Si gate electrode of 75 nm were formed by the following processes, which are based on conventional CMOS process technology. We confirmed the gate oxide thickness of 3 nm using a monitor bulk Si wafer and not using a SOI wafer for device fabrication. After S/D ion implantation processes, a nickel self-align silicidation process was performed. The detailed fabrication process flow is described in [16].

For the electrical evaluation of transfer and output characteristics, single-channel SiNW FETs were measured. For the evaluation of effective carrier mobility (μ_{eff}) and gate-to-channel capacitance (C_{gc}), the multi-channel SiNW FET was measured with the advanced split-CV method [17] for an accurate evaluation of C_{gc} by elimination of the effects of parasitic capacitance and resistance, and ambiguity of the gate length of the FETs.

Cross-sectional transmission electron microscope (TEM) images of SiNW channels are shown in **figure 1**. As can be seen, triangular, trapezoidal, and rectangular cross-sections were obtained. The samples (a), (d), and (e) were fabricated using SOI wafer (*i*): the samples (b) and (c) were fabricated using SOI wafer (*ii*), and the sample (f) was fabricated using SOI wafer (*iii*) as described above. We could not observe an encroachment of nickel silicide between source and drain along the channel direction as in our earlier experiments [18, 19]. The top-width (w_{TOP}) and bottom-width (w_{BOTTOM}) of the samples (a), (b), and (c) were defined and the w_{TOP} of the cross-sections were 0, 13.0 and 18.0 nm, respectively, (we define that the w_{TOP} of 0 nm is related to the triangular cross-sections), whereas w_{BOTTOM} were 24.4 and 25.4 nm, respectively. The difference in w_{TOP} is larger than that in w_{BOTTOM}, and we also characterized the shape with the upper-corner angle θ.

Although the initial cross-sectional shapes of the SiNW channel of all samples were rectangular, the cross-sectional shapes of the SiNW channel depended on the hard mask material. The cross-section of the SiNW channel with SiN hard mask resulted in triangular and rectangular

cross-sections (samples from (a) to (e)). The SiNW channel with silicon dioxide resulted in a rectangular cross-section (sample (f)) in **figure 1**. As the cross-section of <110>-directed SiNW channel with SiN hard mask was rectangular in our previous experiments [20], the triangular and trapezoidal shapes were not simply due to a bird's beak induced by the SiN hard mask. This result suggests an additional cause of the formation of the triangular cross-section. One possibility is that the oxidation of (110)-oriented surface is enhanced by the SiN hard mask. One reason might be the stress induced by the SiN hard mask because the cross-section of silicon nanowire is strongly related to the stress in silicon dioxide layer [5], and the SiN layer tends to induce compressive stress on the under layer [21].

The electrically determined gate oxide thickness of planar SOI FETs was 2.5 nm as shown in the results section. This thickness was different from the oxide thickness confirmed by the monitor wafer, which was a bulk silicon wafer, measured with ellipsometry. During the gate oxidation process, the SOI wafers were heated with an infra-red lamp. As the optical properties were different between the SOI wafers and bulk Si wafers, the process temperature might have been different between the SOI wafer and the monitor wafer. The potentially different process temperature could have caused the reduction of oxidation rate of the gate oxide thin firm.

3. Computer simulation procedures

The inversion charge distribution across the SiNW channel and the gate-to-channel capacitance (C_{gc}) of the SiNW FET were calculated using technical computer-aided design software (TCAD). A two-dimensional structure, which was a cross-section of the channel of the SiNW FET, was designed with the Taurus-MEDICI. The gate capacitance was calculated using the Taurus-DAVINCI with a three-dimensional SiNW FET structure. Quantum-mechanical effects were introduced using the modified local density approximation (MLDA) method [22, 23]. We used the MLDA method in [22, 23] instead of an improved method described in the appendix of [22] because of shorter calculation time of the prior method. The MLDA method is effective for devices with large dimensions. However, it might not be appropriate for the calculation of inversion carrier near the center and also near the corner of the channel cross-section of the devices with smaller cross-sectional dimensions. The gate length of the three-dimensional structure was designed to be 1 μm. The source and drain electrodes were grounded during the calculation of C_{gc} in the same manner as in the split-CV measurement in the experiments. The parameters of the gate materials used in the simulation were those of a p-type polycrystalline silicon for pFETs and a n-type poly-Si for nFETs. The gate oxide thickness was set to 2.5 nm and uniform around the SiNW channel. C_{gc} was calculated using a quasi-static computation scheme implemented in the Taurus-DAVINCI. C_{gc} of the triangular cross-section with h_{NW} of 8 nm and θ of 60, 70, 80 and 90° and a trapezoidal structure with w_{TOP} of 12 nm, h_{NW} of 12 nm and θ of 90, 100, 110, 120, 130 and 140° were calculated. A

transfer characteristic was also calculated with the same structure as used for the calculation of the C_{gc} characteristics. The threshold voltage of the SiNW FET was calculated using a linear extrapolation method at the maximum of transconductance.

4. Results

4.1 Experiments

Typical transfer and output characteristics of SiNW FETs with a gate length of 190 nm and the cross-sectional shape (a) in **figure 1** are shown in **figure 2**. Steep subthreshold swing (S. S.) of 61 and 64 mV/dec. and threshold voltage (V_{th}) of -0.25 and -0.15 V for the nFET and the pFET, respectively, were obtained. A hump reflecting the corner effect was not observed in the transfer characteristics, which is due to the low channel doping concentration [24]. We have evaluated inversion charge density and effective carrier mobility focusing on the upper-corner angle of SiNW channels. However, it has also been reported that effective carrier mobility is also influenced by the size of cross-section [14]. We will demonstrate that the upper-corner angle of the SiNW channel has more important roles on the electrical characteristics of SiNW FET in the discussion section. **Figure 3** shows (a) μ_{eff} and (b) inversion charge density normalized by the peripheral length of side channels and top channel (Q_{inv}). μ_{eff} was extracted at the normalized inversion carrier density (N_S) of 7×10^{12} cm^{-2}, and Q_{inv} was extracted at the overdrive voltage V_{OV} (=$|V_g-V_{th}|$) = 1.0 V using the split-CV method. As θ decreased, Q_{inv} monotonically increased. On the other hand, the trend of μ_{eff} was not monotonic for either pFETs or nFETs. The highest μ_{eff} was obtained for SiNW nFET of device (f) with the upper corner angle of 100^o. SiNW pFET of device (f) was not fabricated and Q_{inv} and μ_{eff} were not available. Therefore, the trend of μ_{eff} of SiNW pFET was not available, and a scenario similar to that of nFET was assumed in **figure 3 (a)**. However, there is a possibility that another reason of the highest μ_{eff} of device (f) might be due to its large cross-sectional shapes.

There is a possibility that calculation of inversion charge density at the same overdrive voltage might not be coherent because electric field of multi-gate device depends on each cross-sectional shape.

We calculated the additional amount of inversion charge (Q_{add}) for the evaluation of a structural advantage of the SiNW FETs on the inversion charge density. We calculated the additional amount of inversion charge (Q_{add}) as shown in equation (1).

$$Q_{add} = \int_{-\infty}^{V_{ov}} c_{gc\_NW}\,dV - A \cdot \int_{-\infty}^{V_{ov'}} C_{gc\_SOI}\,dV \,, \tag{1}$$

where c_{gc_NW} is the gate-to-channel capacitance of the SiNW FET (not normalized). V_{ov} is the overdrive voltage of SiNW FET above 1.0 V from the threshold voltage. A is the channel area of the SiNW FET. C_{gc_SOI} is the normalized gate-to-channel capacitance of the planar SOI FET. $V_{ov'}$ is the

overdrive voltage of the planar SOI FET above 1.0 V from the threshold voltage. The additional amounts of inversion charge Q_{add} are shown in **figure 4**. A larger value of Q_{add} was obtained with a smaller value θ for both pFETs and nFETs, which reflects structural gain due to the upper-corner angles. One possible reason is a concentration of the electrical field around the corners of the SiNW channel and a resulting increased inversion charge density. Similar results were obtained with two-dimensional device simulations in [25], which support the experimental and simulation results in our present work.

To further investigate μ_{eff} and Q_{inv} of the SiNW FET with triangular cross-section, we compared μ_{eff} at N_S of 7×10^{12} cm^{-2} and Q_{inv} at V_{OV} = 1.0 V for the devices (a), (d), and (e) (cf. **tables 1** and **2)**. With h_{NW} = 8 nm, the inversion charge density of device (a) was the largest compared to device (d) with h_{NW} = 16 nm and device (e) with h_{NW} = 20 nm. Therefore, device (a) has an advantage with respect to the inversion charge density. With respect to μ_{eff} at V_{OV} = 1 V, device (a) was comparable with the other devices.

For the evaluation of the degradation in effective carrier mobility μ_{eff} of the SiNW FET with triangular and trapezoidal cross-section, μ_{eff} at V_{OV} = 1.0 V of the SiNW pFET with cross-sections (a), (b) and (c) in **figure 1** was evaluated at 296, 213, 155, 112, 81, 59 and 43 K to extract values of the surface roughness limited mobility, which are summarized in **figure 5**. As the measurement temperature decreased, μ_{eff} at V_{OV} = 1.0 V increased and saturated at approximately 43 K.

The parasitic S/D resistance (R_{SD}) was characterized using Chern's channel-resistance method [26]. R_{SD} of <100>-directed pFETs was drastically reduced compared with R_{SD} of <100>-directed planar SOI pFETs, which were 72 Ωμm with cross-section (c) and 376 Ωμm with planar SOI pFET. However, as the peripheral length decreased, the normalized R_{SD} by the peripheral length of three channel surfaces of the SiNW pFETs increased to 171 Ωμm with cross-section (a).

Finally, we evaluated the drain current of pFETs, which is shown in **figure 7**. The drain current was normalized by the peripheral length of side surfaces and the top surface of the cross-sectional shape. The drain current of the SiNW pFET with the narrowest SiNW channel at V_{OV} = 1.0 V of the SiNW pFETs (sample (a)) with the L_g of 490 nm was the highest, which suggests that the effect of an increased Q_{inv} is superior to the effect of μ_{eff} degradation. However, the I_{ON} of SiNW pFET (sample (a)) with the L_g of 56 nm was degraded compared with the SiNW pFET that had larger θ because of larger R_{SD} with smaller cross-sectional channel dimensions. Considering the footprint of the SiNW channel, the small triangular cross-section might be more favorable for device integration.

4.2 Computer simulation results

First, we calculated the gate-to-channel capacitance C_{gc} of the planar SOI nFET and pFET. Then, we compared the simulated results with our experimental results for the planar SOI FETs fabricated simultaneously with SiNW FETs. After comparing the results of the simulation and experiments, we

found that the electrically determined value for T_{ox} of the fabricated SOI FETs was 2.5 nm. Therefore, T_{ox} for the computer simulation was set to 2.5 nm.

The inversion charge distribution calculated using the Taurus-DAVINCI is shown in **figure 8**. We can see higher inversion charge density regions around the corners of each cross-section. As the corner angle θ decreases, the area of the high inversion charge density region increases. Black and red lines in **figure 3 (b)** indicate the calculated Q_{inv} of the triangular cross-section with θ less than 90^o and Q_{inv} of the trapezoidal cross-section with θ more than 90^o of SiNW nFETs and pFETs, respectively. Both results of Q_{inv} of nFETs and pFETs suggest an increase of Q_{inv} with decreasing value of θ. The channel height h_{NW} = 8 nm of the triangular cross-section for the computer simulation was set to be similar to that of sample (a) in **figure 1**. The channel height h_{NW} = 12 nm of the trapezoidal cross-section for the simulation is also determined to be similar to those of samples (b) and (c) in **figure 1**. The breakpoint at the corner angle around 90^o is due to the difference of the cross-sectional shapes for the computer simulation between θ more than 90^o and θ less than 90^o. When the corner angle θ was large, the simulation results agreed well with the experimental results. However, as the corner angle θ decreased, the differences between the simulation and experimental results became larger. We suppose that the differences between our experimental results of fabricated devices and simulation results are due to the thinning of gate oxide thickness around the corners of the fabricated devices. In contrast, the gate oxide thickness T_{ox} of the simulation was designed to be uniform both around the corners and along the flat channel surface.

We observed a larger inversion charge density of nFET than the inversion charge density of pFET in our simulations. However, the inversion charge density of pFET was larger in our experiment as shown in **figure 3 (b)**. In our simulations, distance of inversion layer from the channel surface in the cross-section of nFET was smaller than the distance of the inversion layer from the channel surface of pFETs. Therefore, the gate capacitance of nFET was larger than the gate capacitance of pFET in our simulation results. We suppose that the experimental results suggest that the increase of the amount of inversion charge near the center of channel cross-section of pFET, which might not well be considered in the simulation using MLDA method.

5. Discussion

There is a geometrical restriction in trapezoidal cross-sections: the sum of the lower-corner angles and the upper-corner angles must be 180^o. Therefore, as the upper corner angle θ increases, the lower-corner angles must decrease, which results in an increase of the contribution of the lower-corner to Q_{inv}. However, the lower-corner is not entirely surrounded by the gate electrode and the contribution to Q_{inv} is smaller than that of the upper-corner. Therefore, we speculate that the contribution of the upper-corner is larger than that of the lower-corner.

Q_{inv} in the experiment agrees well with the calculated Q_{inv} in large θ regions. However, as θ

decreased, the difference between our experimental and simulated results became larger. One possible reason is the oxide thinning around the corners because of the stress introduced into the silicon channel during the gate oxidation process [27-29]. We assume that as the corner angle θ decreases, the stress induced around corners increases and the oxidation rate decreases. We can see similar phenomena in the TEM images of **figure 1**. **Figure 1 (b)** and **(c)** show a smaller deviation than other TEM images, which are suitable for direct observation. The oxide thicknesses of the lower-corners are thinner than in other regions in **figures 1 (b) and (c)**. The oxide thickness of the upper-corners is also thinner in the TEM image in **figure 1 (c)**.

The effective carrier mobility μ_{eff} of the sample (a) (triangular cross-section) was the most degraded for both nFETs and pFETs as shown in **figure 3 (a)** at 296 K. The degradation of μ_{eff} because of the acute corner angle is also confirmed by sample (d) and (e) in **figure 1**. The devices (d) and (e) have larger h_{NW} than the device (a). However, the values for the effective carrier mobility μ_{eff} of the devices (d) and (e) are comparable with μ_{eff} of the device (a) for both nFETs and pFET (cf. **tables 1** and **2**). This result suggests that an acute angle in a SiNW cross-section degrades μ_{eff} severely even when the cross-sectional dimensions are enlarged.

We also evaluated using carrier mobility of pFETs (a), (d), and (e) using Y-function method [30, 31] and the low-field mobility μ_0 of 65.7, 43.9, and 68.1 cm^2/Vs, respectively, was obtained. Theses values are consistent with our results in **table 2**. We could not conclude why μ_{eff} of pFET (d) was much lower than (a) and (e). However, we would like to stress that the acute upper-corner angle degraded effective carrier mobility of SiNW FETs, overall.

We interpret the result in **figure 3 (a)** as follows. When the upper corner angle θ is 133^o, which is the largest θ in the samples in this work, μ_{eff} is the most degraded because the lower-corner angle is the smallest, and the charge around the lower-corner angle suffered from a severe mobility degradation. As θ decreased to 121^o and 100^o, the lower-corner angle increased and the mobility degradation around corners was suppressed. We also speculate that the upper-corner degrades μ_{eff} only marginally when θ decreased in the obtuse angle region. In fact, in **figure 3 (a)**, we failed to observe a degradation of μ_{eff} caused by the reduction of the upper-corner angle θ. Therefore, a balance between the upper-corner angle and the lower-corner angles might determine the optimized point of μ_{eff} of SiNW FET. Based on our results, we conclude that this optimized point is around 100^o for nFETs at 296 K.

For investigation of the causes of effective mobility degradation of SiNW FETs, surface-roughness-limited mobility (μ_{surf}) was evaluated. As the measurement temperature decreased, the effect of the phonon-scattering-limited mobility (μ_{ph}) was reduced. At the temperature nearly 40 K, we can extract surface-roughness-limited mobility μ_{surf} (cf. **figure 5**). μ_{surf} of each device was summarized in **figure 6**. μ_{eff} at the inversion density (N_s) = 7×10^{12} cm^{-2} was 123 cm^2/Vs for nFET and 97.5 cm^2/Vs for pFET, respectively. This result suggests a strong surface roughness scattering of

sample (a). It is reasonable to assume that, as the corner angle decreases, the surface-roughness scattering has a severe effect because the inversion charge near overly tight corners is surrounded by channel surfaces and may therefore be affected more aggressively by the surface roughness of the channel-oxide interface. In **figure 6**, μ_{surf} of SiNW nFET with θ of 133° was more degraded compared with SiNW nFETs with θ of 121° and 100°. We suppose that acute angle of lower-corners degraded μ_{surf} and that obtuse angles of upper-corners affect little on μ_{surf}.

μ_{eff} can be calculated as follows at high inversion carrier density:

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_{surf}} + \frac{1}{\mu_{ph}} \tag{2}$$

, where μ_{ph} is phonon-scattering-limited mobility. μ_{surf} of nFET with θ of 100° was smaller than nFET with θ of 121°. However, phonon-scattering-limited mobility (μ_{ph}) of SiNW nFET with θ of 100° was 912 cm^2/Vs, which was larger than μ_{ph} of SiNW nFET with θ of 121°, 666 cm^2/Vs. Therefore, μ_{eff} of SiNW nFET with θ of 100° was the largest at 296 K.

An increase of μ_{eff} of SiNW nFETs due to a triangular cross-sectional shape with a gate oxide thickness of 20 nm has previously been reported [25]. We assume that the difference between our results and the reported results on μ_{eff} is due to a deposited thick gate oxide, which retards the electrical field near corners because of a structural relaxation of the corner sharpness by deposition, not by thermal oxidation. Another possible reason could be the strong stress because of the SiN hard mask, which resulted in a bended SiNW channel in [4, 25].

The value for R_{SD} of <100>-directed SiNW pFETs was also smaller than the corresponding value of the planar SOI pFETs. R_{SD} of <100>-directed SiNW pFETs was also substantially reduced compared with those of <110>-directed SiNW pFETs. These results suggest that the boron diffusion is different for SiNW or planar devices and SiNW channel directions. For <100>-directed SiNW pFETs, R_{SD} normalized by the peripheral length of three surfaces is also different, and as the dimensions decreased, the normalized R_{SD} increased. This phenomenon could be explained by an additional access resistance (R_{acc}) from the S/D region to the SiNW channel, as shown in **figure 9**, where tapered shapes were realized during the lithography steps. Therefore, an additional treatment including tilted implantations or dopant segregation with a nickel silicidation technology is especially required to reduce the increasing resistance for SiNW FET with small dimensions.

In this work, we assumed that the upper-corners have no influence on each other because w_{TOP} is approximately 15 nm and therefore sufficiently large to consider them separable. This is also shown in the computer simulation results (cf. **figure 8)**. When w_{TOP} is further reduced, the high Q_{inv} regions approach each other and might merge. A SiNW FET with such a cross-section is out of the scope of this work and would require further experiments.

6. Conclusions

We have investigated the electric characteristics of the <100>-directed SiNW nFETs and pFETs with triangular, trapezoidal and rectangular cross-sections. Focusing on the corner angles of the cross-sections, we obtained a larger additional amount of inversion charge with the SiNW FETs with smaller upper corner angles of the SiNW channel cross-section. On the other hand, the effective carrier mobility μ_{eff} at V_{OV} = 1.0 V could have its optimized point at around θ of 100°. We interpret the results of Q_{inv} and μ_{eff} as follows: (*i*) an overly acute angle degrades the effective carrier mobility around the corners, and an enlargement of the cross-sectional dimensions has only a minor effect; (*ii*) the contribution of the upper-corner angle is larger than that of the lower-corner angles because of the semi gate-around structure. Furthermore, we examined the expectation of the on-current (I_{ON}) based on measured values of Q_{inv} and μ_{eff}. The on-current I_{ON} was normalized by the peripheral length of side channels and top channel of cross-sectional shapes. Although normalized inversion charge density was the largest, effective carrier mobility with acute upper-corner angle was severely degraded. Considering the intrinsic delay time (*CV/I*) of SiNW FET, SiNW FETs with rectangular cross-section with upper-corner angle of 100° is the most suitable in this work to achieve high electrical performance. We believe that these findings represent valuable guidelines for the design of a high performance SiNW FET. Our future work will focus on an analysis of SiNW FETs with channel cross-sections that have a smaller w_{WN} than those in this work, in which each corner might correlate with each other.

Acknowledgements

The authors thank all members of ASKA II line and the researchers in the front-end program in the R&D department 1, Selete, Tsukuba for device fabrication and fruitful discussions. This work was supported by the program 'Development of Nanoelectronic Device Technology' of the New Energy and Industrial Technology Development Organization (NEDO). The authors thank Dr. Daniel Berrar for proofreading.

References

[1] Li M., Yeo K. H., Suk S. D., Yeoh Y. Y., Kim D-W., Chung T. Y., Oh K. S., Lee W-S. Sub-10 nm gate-all-around CMOS nanowire transistors on bulk Si substrate. Tech. Dig. Symp. of VLSI Tech. 2009: 94-95.

[2] Singh N., Lim F. Y., Fang W. W., Rustagi S. C., Bera L. K., Agarwal A., Tung C. H., Hoe K. M., Omampuliyur S. R., Tripathi D., Adeyeye A. O., Lo G. Q., Balasubramanian N., Kwong D. L. Ultra-narrow silicon nanowire gate-all-around CMOS devices: impact of diameter, channel-orientation and low temperature on device performance. Tech. Dig. of Int'l Electron

Device Meet. 2006:1-4.

[3] Ma F.-J., Rustagi S. C., Samudra G. S., Zhao H., Singh N., Lo G-Q., Kwong D.-L. Modeling of stress-retarded thermal oxidation of nonplanar silicon structures for realization of nanoscale devices. IEEE Electron Device Lett. 2010;31(7):19-721.

[4] Moselund K. E., Dobrosz P., Olsen S., Pott V., De Michielis L., Tsamados D., Bouvet D., O'Neill A., Ionescu A. M. Bended Gate-All-Around Nanowire MOSFET: a device with enhanced carrier mobility due to oxidation-induced tensile stress. Tech. Dig. of Int'l Electron Device Meet. 2007:191-194.

[5] Kedzierski J., Bokor J., Kisielowski C. Fabrication of planar silicon nanowires on silicon-on-insulator using stress limited oxidation. J. Vac. Sci. Technol. B. 1997;15(6):2825-2828.

[6] Liu H. I., Biegelsen D. K., Ponce F. A., Johnson F. A., Pease R. F. W. Self-limited oxidation for fabricating sub-5nm silicon nanowire. Appl. Phys. Lett. 1994;64(11):1383-1385.

[7] Lee M. C. M., Wu M. C. Thermal annealing in hydrogen for 3-D profile transformation on silicon-on-insulator and sidewall roughness reduction. J. Microelectromech. Syst. 2006;15(2):338-343.

[8] Tezuka T., Toyoda E., Nakaharai S., Irisawa T., Hirashita N., Moriyama Y., Sugiyama N., Taoka N., Yamashita Y., Kiso O., Harada M., Yamamoto T., Takagi S. Observation of mobility enhancement in strained Si and SiGe tri-gate MOSFETs with multi-nanowire channels trimmed by hydrogen thermal etching. Tech. Dig. fo Int'l Electron Device Meet. 2007:887-890.

[9] Suk S. D., Yeoh Y. Y., Li M., Yeo H. Y., Kim S. H., Kim D. W., Park D., Lee W. S. TSNWFET for SRAM cell application: Performance variation and process dependency. Tech. Dig. Symp. of VLSI Tech. 2008:38-39.

[10] Bidal G., Boeuf F., Denorme S., Loubet N., Huguenin J. L., Perreau P., Fleury D., Leverd F., Lagrasta S., Barnola S., Salvetat T., Orlando B., Beneyton R., Clement L., Pantel R., Monfray S., Ghibaudo G., Skotnicki T. High velocity Si-nanodot: a candidate for SRAM applications at 16 nm node and below. Tech. Dig. Symp. of VLSI Symp. 2009:240-241.

[11] Wunnicke O. Gate capacitance of back-gated nanowire field-effect transistors. Appl. Phys. Lett. 2006;89(8):083102.

[12] Suk S. D., Li M., Yeoh Y. Y., Yeo K. H., Cho K. H., Ku I. K., Cho H., Jang W., Kim D. W., Park D., Lee W. S. Investigation of nanowire size dependency on TSNWFET. Tech Dig. of Int'l Electron Device Meet. 2007:891-894.

[13] Giacomini R., Martino J. A. Trapezoidal cross-section influence on FinFET threshold voltage and corner effects. J. Electrochem. Soc. 2008;155(4):213-217.

[14] Chen J., Saraya T., Miyaji K., Shimizu K., Hiramoto T. Electron mobility in silicon

gate-all-around [100]- and [110]- directed nanowire metal-oxide-semiconductor field-effect transistors on (100)-oriented silicon-on-insulator substrate extracted by improved split capacitance-voltage method. Jpn. J. Appl. Phys. 2009;48(1):011205.

[15] Cassé M., Tachi K., Thiele S., Ernst T. Spectroscopic charge pumping in Si nanowire transistors with ah high-k/metal gate. Appl. Phys. Lett. 2010;96(12):123506.

[16] Sato S., Kamimura H., Arai H., Kakushima K., Ahmet P., Ohmori K., Yamada K., Iwai H. Electrical characterization of Si nanowire field-effect transistors with semi gate-around structure suitable for integration. Solid-State Electron. 2010;54(9):925-928.

[17] Irie H., Toriumi A. Advanced split-CV technique for accurate extraction of inversion layer mobility in short channel MOSFETs. Extended Abstracts of International Conference on Solid State Devices and Materials. 2005:864-865.

[18] Kamimura H., Arai H., Sato S., Kakushima K., Ahmet P., Tsutsui K., Sugii N., Hattori T., Iwai H. Evaluation of lateral Ni diffusion in Si nanowire Schottky contact. ECS Trans. 2009;18(1):71-75.

[19] Arai H., Kamimura H., Sato S., Kakushima K., Ahmet P., Nishiyama A., Tsutsui K., Sugii N., Natori K., Hattori T., Iwai H. Annealing reaction for Ni silicidation of Si nanowire. ECS Trans. 2009;25(7):447-454.

[20] Sato S., Lee Y., Kakushima K., Ahmet P., Ohmori K., Natori K., Yamada K., Iwai H. Gate semi-around Si nanowire FET fabricated by conventional CMOS process with very high drivability. Proc. of the 40th European Solid-State Device Research Conference. 2010:361-364.

[21] French P. J., Sarro P. M., R. Mallée, Fakkeldij E.J. M., Wolffenbuttel R. F. Optimization of a low-stress silicon nitride process for surface-micromachining applications. Sensors and Actuators A. 1997;58(2):149-157.

[22] Ancona M. G., Tiersten H. F. Macroscopic physics of the silicon inversion layer. Phys. Rev. B. 1987;4(6):7959-7965.

[23] Paasch G., Übensee H. A modified local density approximation. Electron density in inversion layers. Phys. Stat. Sol. (b) 1982;133(1):165-178.

[24] Fossum J. G., Yang J. W., Trivedi V. P. Suppression of corner effects in triple-gate MOSFETs. IEEE Electron Device Lett. 2003;24(12):745-747.

[25] Moselund K. E., Bouvet D., Tschuor L., Pott V., Dainesi P., Ionescu A. M. Local volume inversion and corner effects in triangular gate-all-around MOSFETs. Proc. of the 36th European Solid-State Device Research Conference. 2006:359-362.

[26] Chern J. G. J., Chang P., Motta R. F., Godinho N. A new method to determine MOSFET channel length. IEEE Elecron Device Lett. 1980;1(9):170-173.

[27] Sekaric L., Gunawan O., Majumdar A., Liu X-H., Weinstein D., Sleight J-W. Size-dependent modulation of carrier mobility in top-down fabricated silicon nanowires. Appl. Phys. Lett. 2009;95(2):023113.

[28] Seike A., Tange T., Sano I., Sugiura Y., Kosemura D., Ogura A., Ohdomari I. Transconductance enhancement of nanowire field-effect transistors by built-up stress induced during thermal oxidation. Appl. Phys. Lett. 2007;91(6):062108.

[29] Sakina Y., Ohno T., Matsumoto S. Two-dimensional analysis of thermal oxidation of silicon. Jpn. J. Appl. Phys. 1983;22(8):L514-516.

[30] Ghibaudo G. New method for the extraction of MOSFET parameters. Electronics Lett. 1988;24(9):543-545.

[31] Tanaka T. Novel parameter extraction method for low field drain current of nano-scaled MOSFETs. Proc. IEEE Int. Conf. Microelectronic Test Structure. 2007;265–267.

Figure captions

Figure 1. Cross-sectional transmission electron microscope (TEM) images of the channels of the <100>-directed SiNW FETs with a semi gate-around structure fabricated on (100)-oriented silicon-on-insulator wafer.

Figure 2. Typical (a) transfer and (b) output characteristics of <100>-directed SiNW FETs with a gate length of 190 nm with the cross-section (a) in figure 1.

Figure 3. (a) Effective carrier mobility (μ_{eff}) at the inversion carrier density of 7×10^{12} cm^{-2} (b) inversion charge density (Q_{inv}) at the absolute overdrive voltage of 1.0 V of SiNW FETs.

Figure 4. An additional amount of inversion charge (Q_{add}) at the absolute overdrive voltage of 1.0 V dependence on the upper-corner angles θ of the SiNW pFETs.

Figure 5. Effective carrier mobility of (a) nFETs and (b) pFETs at the inversion charge density of 7×10^{12} cm^{-2} measured at 296, 213, 155, 112, 81, 59 and 43 K. The black and gray circles indicate the rectangular cross-section with the upper-corner angles θ of 121^{o} and 133^{o}, respectively. The white circles indicate the triangular cross-section with θ of 78^{o}. The white rectangles indicate the rectangular cross-section with θ of 100^{o}.

Figure 6. Surface-roughness-limited mobility of both SiNW nFETs and pFETs as a function of the upper corner angle. The surface-roughness-limited mobility was extracted at the inversion carrier

density (N_S) of 7×10^{12} cm^{-2} at the measurement temperature of 40K.

Figure 7. Normalized drain current of the SiNW pFET with a gate length of 490 and 56 nm and different upper-corner angles θ.

Figure 8. Two-dimensional inversion charge distribution of different Si nanowire cross-sections calculated with the Taurus-DAVINCI with triangular cross-sections with θ of (a) 60^o, (b) 70^o, and (c) 80^o and h_{NW} of 8 nm, and trapezoidal cross-sections with h_{NW} of 12 nm, w_{TOP} of 12 nm and θ of (c)90^o, (e) 110^o, (f) 130^o, and (g) 150^o.

Figure 9. A schematic illustration of an additional access resistance to total a source/drain series resistance of the SiNW FETs.

Table captions

Table 1. Inversion charge density at the absolute overdrive voltage of 1.0 V of devices (a), (d) and (e).

Table 2. Effective carrier mobility at the normalized inversion carrier density of 7×10^{12} cm^{-2} of device (a), (d) and (e).

Figure 1

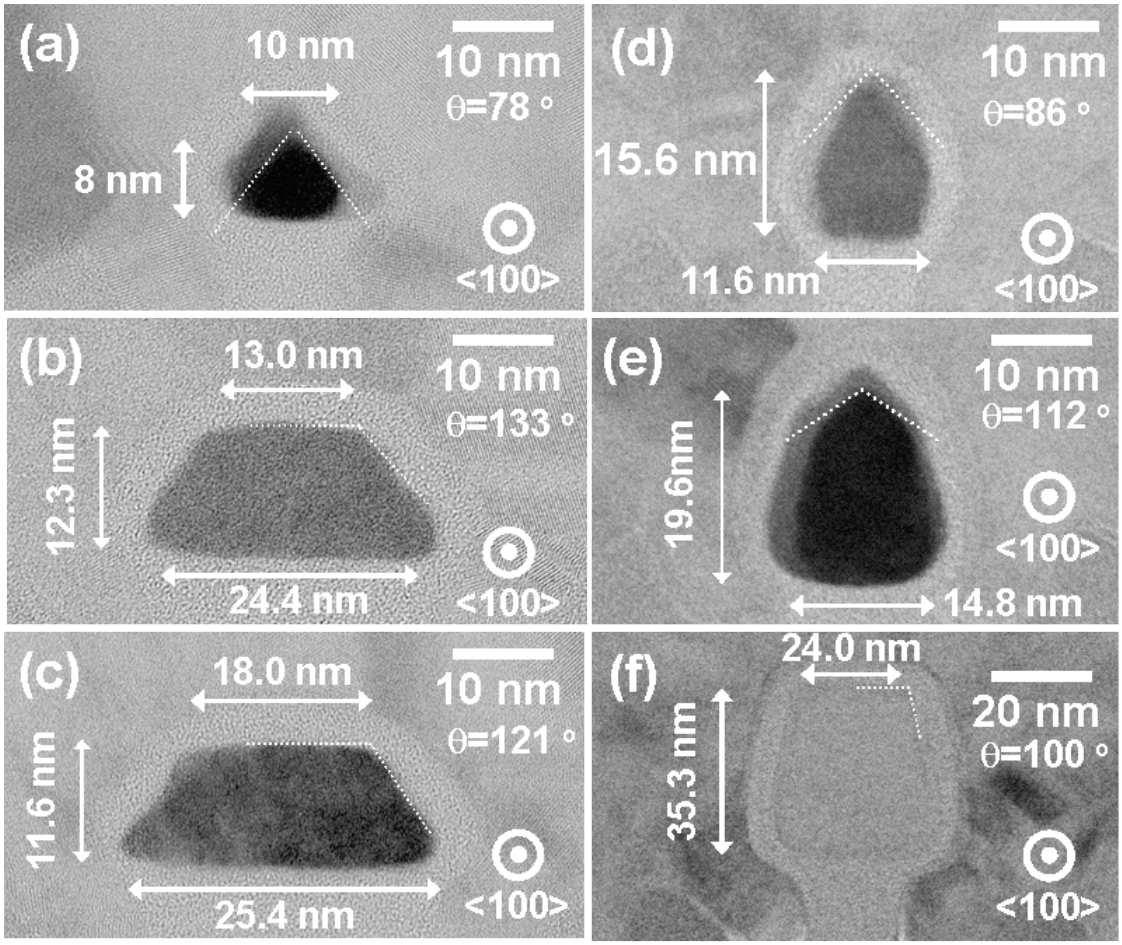
(a)
10 nm
8 nm
10 nm
θ=78 °
<100>
(d)
15.6 nm
11.6 nm
10 nm
θ=86 °
<100>
(b)
13.0 nm
12.3 nm
24.4 nm
10 nm
θ=133 °
<100>
(e)
19.6nm
14.8 nm
10 nm
θ=112 °
<100>
(c)
18.0 nm
11.6 nm
25.4 nm
10 nm
θ=121 °
<100>
(f)
24.0 nm
35.3 nm
20 nm
θ=100 °
<100>

Figure 2

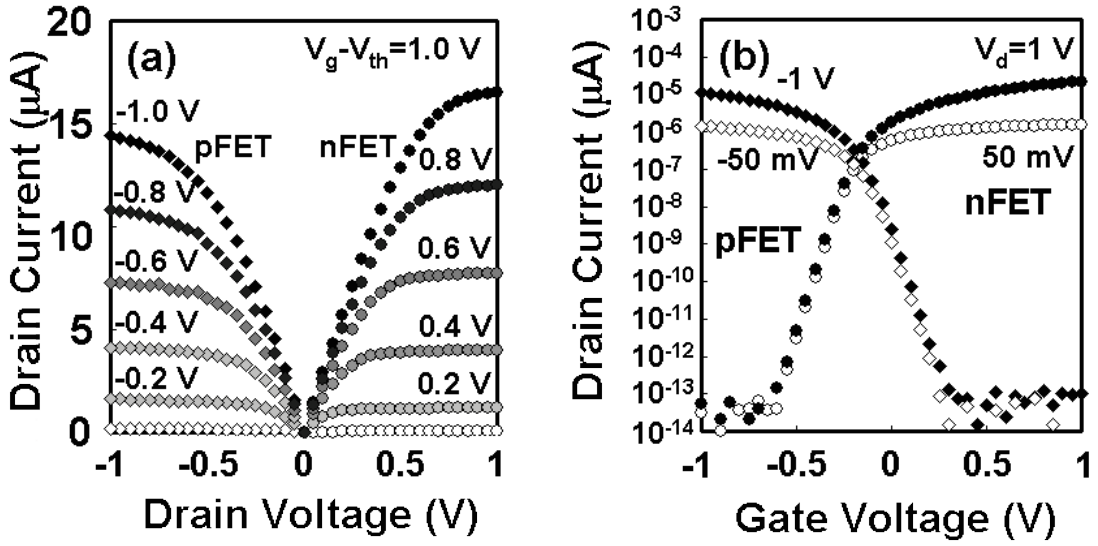
(a)
V_g-V_{th}=1.0 V
-1.0 V
pFET
nFET
0.8 V
-0.8 V
0.6 V
-0.6 V
0.4 V
-0.4 V
0.2 V
-0.2 V
Drain Current (μA)
Drain Voltage (V)
(b)
V_d=1 V
-1 V
-50 mV
50 mV
nFET
pFET
Drain Current (μA)
Gate Voltage (V)

Figure 3

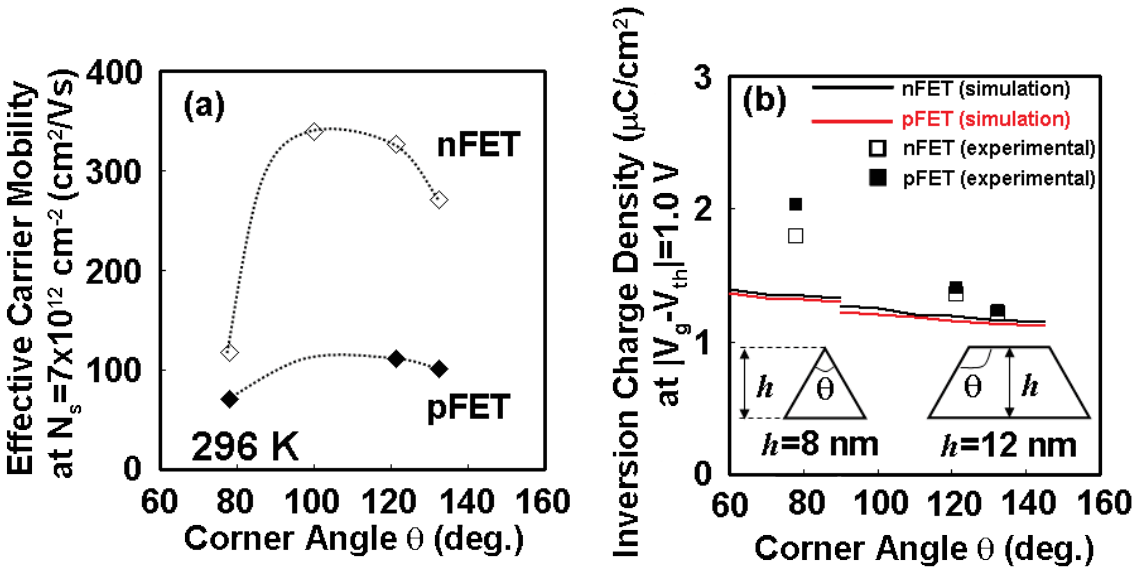
(a)
nFET
pFET
296 K
Effective Carrier Mobility at N_s=7x10^{12} cm^{-2} (cm^2/Vs)
Corner Angle θ (deg.)
(b)
nFET (simulation)
pFET (simulation)
nFET (experimental)
pFET (experimental)
h
θ
h=8 nm
h=12 nm
Inversion Charge Density (μC/cm^2) at |V_g-V_{th}|=1.0 V
Corner Angle θ (deg.)

Figure 4

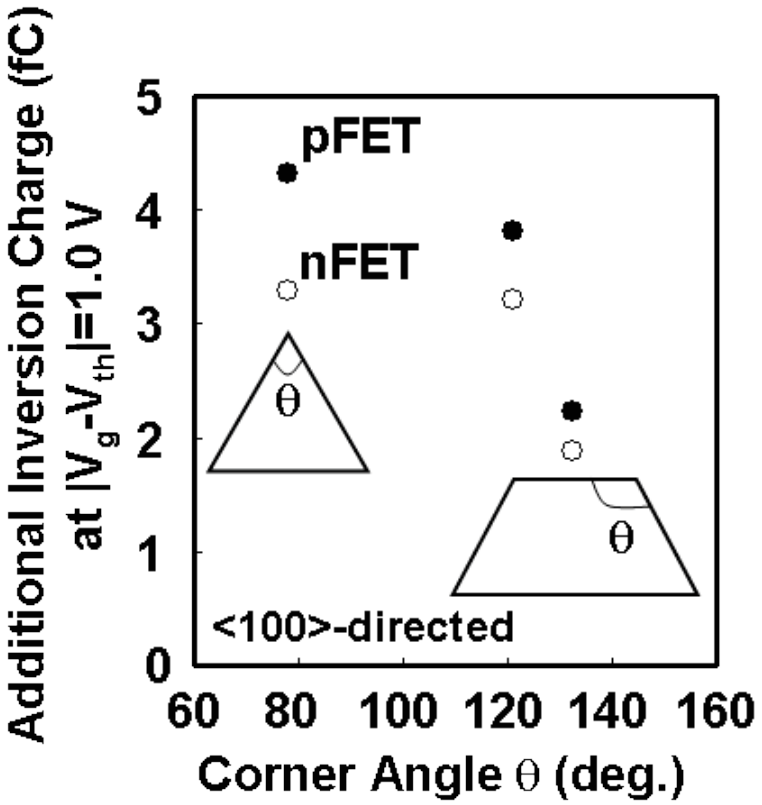
Additional Inversion Charge (fC)
at |Vg-Vth|=1.0 V
5
4
3
2
1
0
pFET
nFET
θ
θ
<100>-directed
60
80
100
120
140
160
Corner Angle θ (deg.)

Figure 5

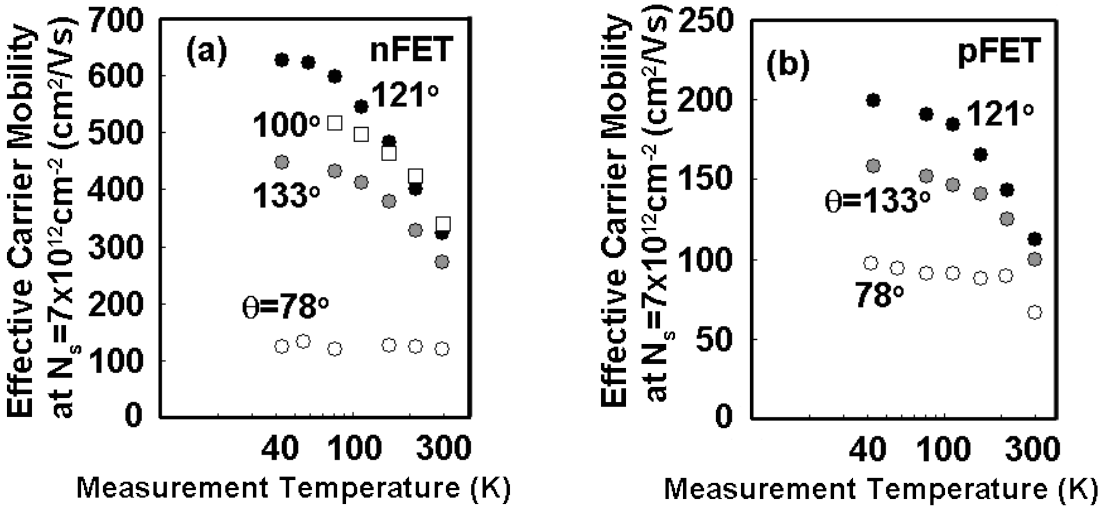
(a)
nFET
121°
100°
133°
θ=78°
Effective Carrier Mobility at N_s=7x10^{12}cm^{-2} (cm^2/Vs)
700
600
500
400
300
200
100
0
40
100
300
Measurement Temperature (K)
(b)
pFET
121°
θ=133°
78°
250
200
150
100
50
0
40
100
300
Measurement Temperature (K)

Figure 6

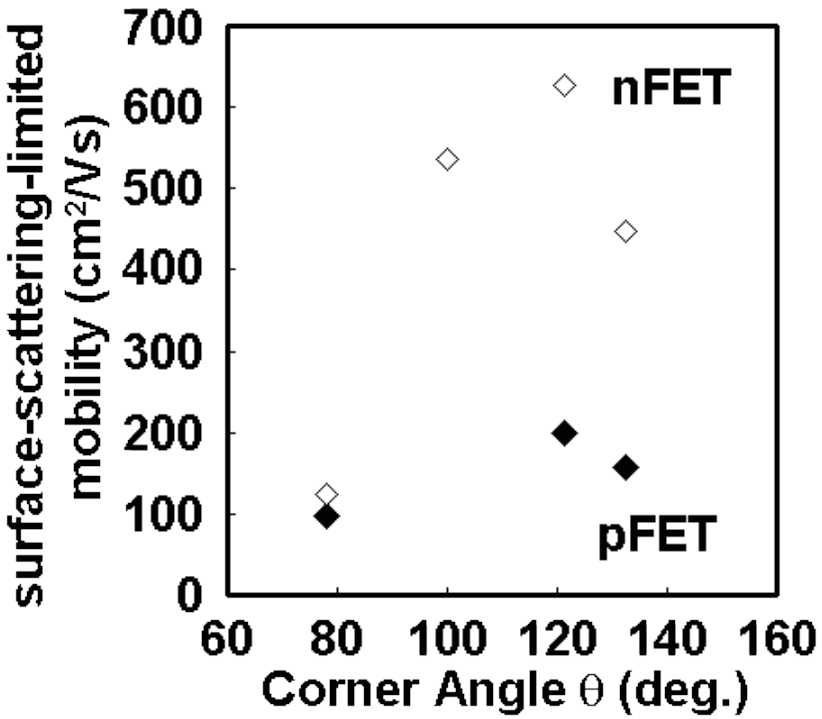
surface-scattering-limited mobility (cm²/Vs)
700
600
500
400
300
200
100
0
60
80
100
120
140
160
Corner Angle θ (deg.)
nFET
pFET

Figure 7

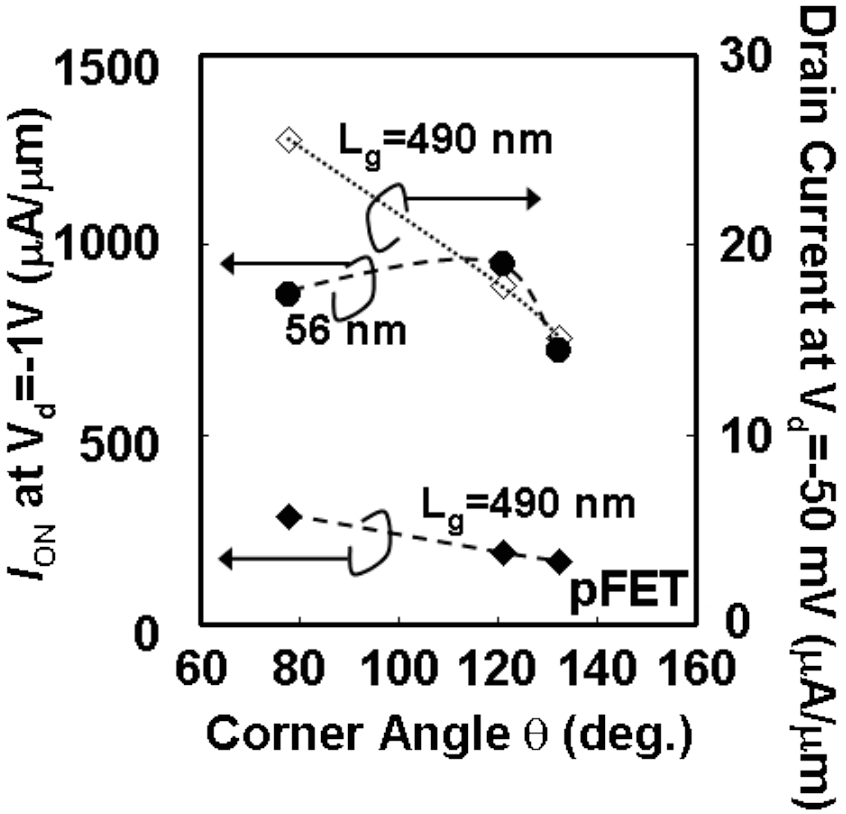
1500
1000
500
0
30
20
10
0
60
80
100
120
140
160
L_g=490 nm
56 nm
L_g=490 nm
pFET
I_{ON} at V_d=-1V (μA/μm)
Drain Current at V_d=-50 mV (μA/μm)
Corner Angle θ (deg.)

Figure 8

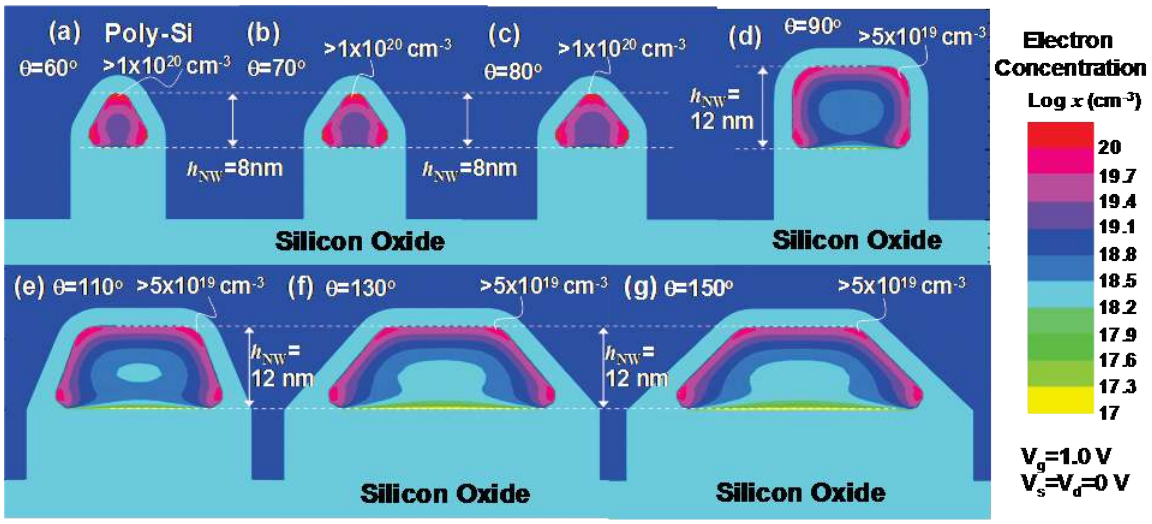
(a) Poly-Si
θ=60°
>1x10^20 cm^-3
(b)
θ=70°
>1x10^20 cm^-3
(c)
θ=80°
>1x10^20 cm^-3
(d)
θ=90°
>5x10^19 cm^-3
h_NW=8nm
h_NW=8nm
h_NW= 12 nm
Silicon Oxide
Silicon Oxide
(e) θ=110°
>5x10^19 cm^-3
(f) θ=130°
>5x10^19 cm^-3
(g) θ=150°
>5x10^19 cm^-3
h_NW= 12 nm
h_NW= 12 nm
Silicon Oxide
Silicon Oxide
Electron Concentration
Log x (cm^-3)
20
19.7
19.4
19.1
18.8
18.5
18.2
17.9
17.6
17.3
17
V_g=1.0 V
V_s=V_d=0 V

Figure 9

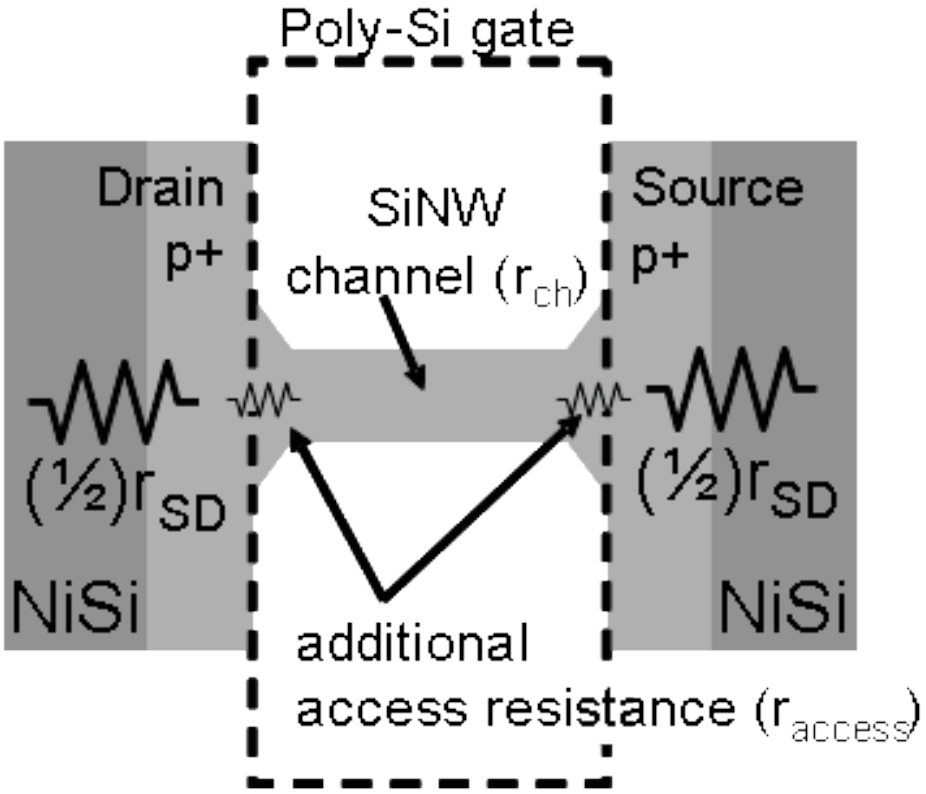
Poly-Si gate
Drain
p+
SiNW
channel (r_{ch})
Source
p+
($\frac{1}{2}$)r_{SD}
($\frac{1}{2}$)r_{SD}
NiSi
NiSi
additional
access resistance (r_{access})

Table 1

	nFET ($\mu C/cm^2$)	pFET ($\mu C/cm^2$)
(a)	1.79	2.03
(d)	1.24	1.28
(e)	1.15	1.26

Table 2

	nFET (cm^2/Vs)	pFET (cm^2/Vs)
(a)	110	69.3
(d)	124	38.5
(e)	123	64.3