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J. J. Gu
Birck Nanotechnology Center, Purdue University

Y. Q. Wu
Birck Nanotechnology Center, Purdue University

Peide D. Ye
Birck Nanotechnology Center, Purdue University, yep@purdue.edu

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J. J. Gu, Y. Q. Wu, and P. D. Ye

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Effects of gate-last and gate-first process on deep submicron inversion-mode InGaAs *n*-channel metal-oxide-semiconductor field effect transistors

J. J. Gu, Y. Q. Wu, and P. D. Ye[a)]
School of Electrical and Computer Engineering and Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana 47907, USA

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Recently, encouraging progress has been made on surface-channel inversion-mode In-rich InGaAs NMOSFETs with superior drive current, high transconductance and minuscule gate leakage, using atomic layer deposited (ALD) high-k dielectrics. Although gate-last process is favorable for high-*k*/III–V integration, high-speed logic devices require a self-aligned gate-first process for reducing the parasitic resistance and overlap capacitance. On the other hand, a gate-first process usually requires higher thermal budget and may degrade the III–V device performance. In this paper, we systematically investigate the thermal budget of gate-last and gate-first process for deep-submicron InGaAs MOSFETs. We conclude that the thermal instability of $(NH_4)_2S$ as the pretreatment before ALD gate dielectric formation leads to the potential failure of enhancement-mode operation and deteriorates interface quality in the gate-first process. We thus report on the detailed study of scaling metrics of deep-submicron self-aligned InGaAs MOSFET without sulfur passivation, featuring optimized threshold voltage and negligible off-state degradation. © *2011 American Institute of Physics*. [doi:10.1063/1.3553440]

I. INTRODUCTION

The continuous device scaling and performance improvements required by the International Technology Roadmap of Semiconductors (ITRS) are facing a grand challenge as conventional Si CMOS scaling is approaching its fundamental limits. As several new technologies such as high-*k* metal gate integration, silicon-on-insulator (SOI) devices, nonplanar Si transistors and strained channel materials have been developed to maintain the Moore's Law, tremendous efforts have been spent to look into those alternative channel materials "beyond Si" such as Germanium and III–V compound semiconductors. In particular, high indium content InGaAs is considered as the most promising n-channel material for future low-power high-performance CMOS applications, benefiting from its high electron mobility, saturation velocity and trap neutral level near conduction bandedge. In the quest for perfect dielectrics on III-V semiconductors, significant progress has been made recently on many promising dielectrics including atomic-layer-deposited (ALD) Al_2O_3,[1–4] HfO_2,[4–6] HfAlO,[4,7,8] ZrO_2 (Ref. 9) and *in situ* molecule-beam-epitaxial (MBE) $Ga_2O_3(Gd_2O_3)$.[10–12] Most recently, record-high inversion current[2,13] and transconductance[14,15] with good off-state performance[15] have been achieved for InGaAs MOSFETs with high-*k* gate dielectrics formed by ALD.

In our previous long-channel and deep-submicron InGaAs MOSFET fabrication, a gate-last nonself-aligned process was applied, which requires a low thermal budget after high-*k* dielectric and metal gate formation and is favorable for a simplified process. However, real high-speed logic devices require a gate-first self-aligned process by eliminating overlap capacitance and reducing the series resistance. Recently, self-aligned ALD high-*k*/$In_{0.53}Ga_{0.47}As$ MOSFETs with a TaN,[6,8] TiN,[12] TiW,[16] or W (Ref. 17) metal gate were demonstrated. The threshold voltage in Refs. 6, 8 and 12 is relatively low for enhancement-mode operation, resulting in an intolerable off current at zero gate voltage. It has also been reported that the gate-first process introduces a much larger interface trap density between the high-*k* and InGaAs interface.[18] It is worth pointing out that for the surface-channel InGaAs MOSFET gate stack formation, channel surface preparation such as HF/HCl, NH_4OH, and $(NH_4)_2S$ are usually applied before *ex situ* ALD high-*k* process, which provides a simple yet effective way to realize high-quality interface. However, the thermal stability of these surface pretreatments may cause some detrimental effects due to the higher thermal budget for gate-first self-aligned process. Moreover, all reported self-aligned InGaAs MOSFET processes use refractory metals as the gate metal. Dry etching of refractory metals is a more complicated process than lift-off of conventional metals and can potentially deteriorate the insulating high-*k* dielectric and the high-*k*/InGaAs interface.

In this paper, we report on a systematic study on the thermal budget for gate-last and gate-first InGaAs MOSFET fabrication. It is found that $(NH_4)_2S$ surface preparation is thermally unstable at processing temperatures higher than 400–500 °C and is incompatible with the gate-first self-aligned process. High temperature annealing of the sulfur-treated surface is harmful for the interface quality, resulting in significant threshold voltage shift and the deterioration in off-state performance. Furthermore, by optimizing the thermal budget of the gate-first process, a simple metal (Ni/Au) lift-off process is used in the fabrication of self-aligned inversion-mode InGaAs MOSFETs. A complete scaling metrics study is carried out for the self-aligned devices with gate

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[a)] Author to whom correspondence should be addressed. Electronic mail: yep@purdue.edu.

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lengths from 300 nm down to 100 nm. The thermal budget discussion of the gate-last nonself-aligned process and the thermal stability of sulfur passivation are discussed in Sec. II. The fabrication process, thermal budget and scaling metrics study of the gate-first self-aligned process are addressed in Sec. III.

II. GATE-LAST NON-SELF-ALIGNED PROCESS

A. *Experiment details*

Figure 1 shows the schematic cross section and fabrication process flow of gate-last nonself-aligned $In_{0.75}Ga_{0.25}As$ MOSFETs. The substrate material is similar to those reported before, in which a 500 nm p-doped 4×10^{17} cm^{-3} buffer layer, a 300 nm p-doped 1×10^{17} cm^{-3} $In_{0.53}Ga_{0.47}As$ and a 12 nm 1×10^{17} cm^{-3} $In_{0.75}Ga_{0.25}As$ channel layer were sequentially grown by MBE on a 2-inch InP p+substrate. After surface degreasing and ammonia-based native oxide etching, 10 nm thick Al_2O_3 encapsulation layer was deposited using an ASM F-120 ALD reactor at 300 °C. Source and drain regions were selectively implanted with a Si dose of 1×10^{14} cm^{-2} at 20keV. Here ∼200 nm thick electron beam resist PMMA A4 was used as hard mask to protect the channel region underneath from the ion implantation. Implantation activation was performed by rapid thermal anneal (RTA) at 600 °C for 15 s in N_2 ambient. Al_2O_3 gate dielectric (5 nm) was regrown by ALD after removing the encapsulation layer. $(NH_4)_2S$ was used to passivate the surface before the gate oxide growth. To study the thermal stability of sulfur treatment, the two post-deposition anneal (PDA) process was performed at 400 °C or 600 °C in N_2 ambient. The source and drain ohmic contacts were made by an electron beam evaporation of a combination of AuGe/Ni/Au and lift-off process followed by a RTA at 320 °C for 30 s also in N_2 ambient. Finally, the gate electrode was defined by electron beam evaporation of Ni/Au and lift-off process. All patterns were defined by a Vistec VB-6 UHR electron-beam lithography (EBL) system. In a gate-last non-self aligned process, the metal gate electrode has an overlap of ∼100 nm with the source and drain region to avoid the misalignment for the second EBL.

B. *Thermal budget*

In the gate-last process, because the ALD Al_2O_3 gate dielectric is regrown after the S/D activation, the thermal budget of the high-*k*/InGaAs is determined by the process following gate oxide regrowth. Therefore, the gate-last process usually requires a lower thermal budget and is considered beneficial for the high-*k* dielectric integration. In this study, the PDA process at either 400 °C or 600 °C is the dominant factor in terms of thermal budget consideration. A PDA process after the ALD dielectric growth condenses the film and decreases the hysteresis, which is considered helpful to the gate stack in most cases. On the other hand, it increases the thermal budget and may cause inter-diffusion at the oxide/III–V interface. In this experiment, we find that a PDA of 600 °C causes a negative threshold voltage shift and degrades the off-state performance. We ascribe this detrimental effect to the thermal instability of the sulfur pretreated interface. The details are addressed in the next section.

C. *Thermal instability of sulfur passivation*

Figure 2 shows the output and transfer characteristics of two 160-nm gate length gate-last $In_{0.75}Ga_{0.25}As$ MOSFETs with 400 °C or 600 °C PDA process after gate dielectric deposition. The EOT of these devices is around 2.4 nm. The on current improves by ∼5% for the device with 600 °C PDA. However, there is a clear shift of the I_{ds}-V_{gs} curve to the negative gate voltage. This is further confirmed by the split CV measurement result shown in Fig. 3. For the same 160-nm L_g device, the gate capacitance start to increase at around 0.3 V for 400 °C PDA devices, while this threshold shifts to around 0V for 600 °C annealed devices. A 10% increase in C_{gc} is also observed which may result from an increase in dielectric constant after 600 °C PDA. Moreover, the threshold voltage shift is present for all devices regardless of the gate length as illustrated in Fig. 4. Here the threshold voltage is obtained using conventional linear extrapolation at low drain bias for devices with L_g from 140 to 250 nm. A threshold voltage shift of approximately −0.3V is consistently observed for all devices annealed at 600 °C. Meanwhile, the subthreshold slope (SS) degrades by about 20% for 600 °C annealed devices, as shown in Fig. 5.

One origin for the negative V_T shift is that the sulfur layer at the interface diffuses into InGaAs and is partially activated at PDA temperatures higher than 400 °C. Previous XPS studies show that after ALD growth, monolayers of sulfur still exist at high-k/III-V interface.[19,20] More recently, monolayer doping (MLD) has been successfully realized on

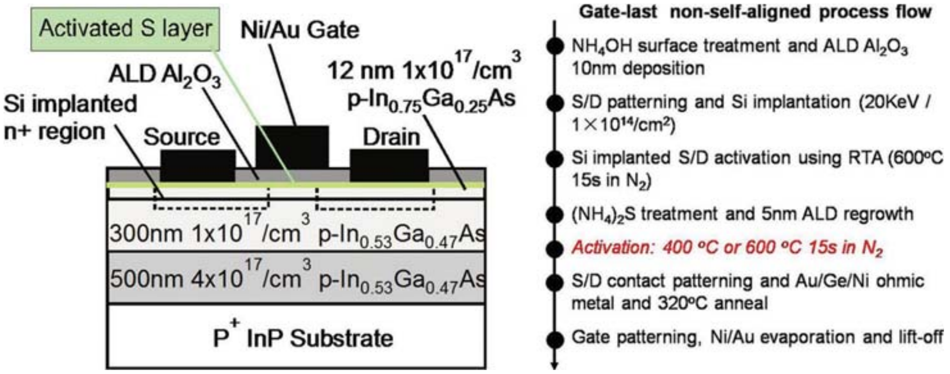
Activated S layer
Ni/Au Gate
ALD Al_2O_3
12 nm $1x10^{17}/cm^3$
p-$In_{0.75}Ga_{0.25}As$
Si implanted
n+ region
Source
Drain
300nm $1x10^{17}/cm^3$ p-$In_{0.53}Ga_{0.47}As$
500nm $4x10^{17}/cm^3$ p-$In_{0.53}Ga_{0.47}As$
P^+ InP Substrate
Gate-last non-self-aligned process flow
NH_4OH surface treatment and ALD Al_2O_3 10nm deposition
S/D patterning and Si implantation (20KeV / $1\times10^{14}/cm^2$)
Si implanted S/D activation using RTA (600°C 15s in N_2)
$(NH_4)_2S$ treatment and 5nm ALD regrowth
Activation: 400 °C or 600 °C 15s in N_2
S/D contact patterning and Au/Ge/Ni ohmic metal and 320°C anneal
Gate patterning, Ni/Au evaporation and lift-off

FIG. 1. (Color online) Schematic cross section and fabrication process of a non-self-aligned inversion-mode n-channel $In_{0.75}Ga_{0.25}As$ MOSFET with gate-last process. 400 or 600°C PDA process after gate dielectric regrowth is added to investigate the thermal stability of the $(NH_4)_2S$ treatment.

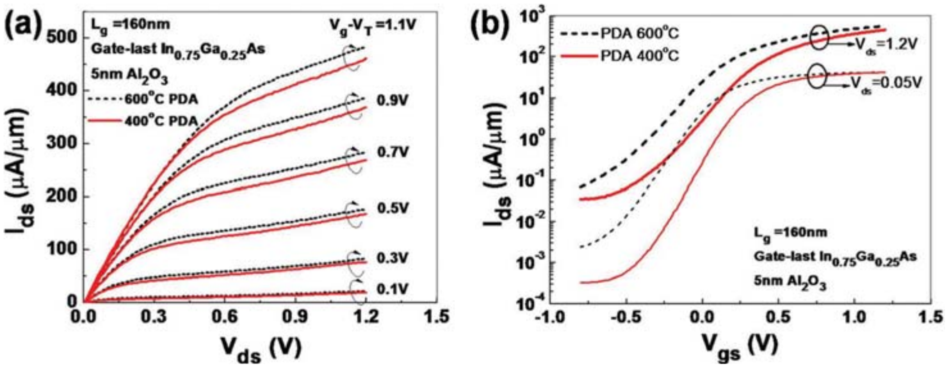

FIG. 2. (Color online) (a) output and (b) transfer characteristics of an $L_g = 160$ nm gate-last $In_{0.75}Ga_{0.25}As$ MOSFET with 400 or 600 °C PDA process after gate dielectric deposition.

InAs substrate with $(NH_4)_2S_x$ pretreated surface and thermal diffusion process.[21] Similarly to MLD, our results also suggest that the 600 °C PDA drives in the sulfur atoms at Al_2O_3/InGaAs interface, which serve as *n*-type dopants in the channel region. A simple calculation reveals that a $\Delta Q \approx -1.6 \times 10^{12}$ cm^{-2} additional negative charge has been induced by the S-doping. The S-induced negative sheet charge depletes the p-type channel region even at zero gate bias. This explains the negative V_T shift observed for devices with 600 °C PDA. The 20% degradation in SS indicates that more interfaced traps have been introduced after high temperature annealing: this also contributes to the negative V_T shift. The trap neutral level (TNL) in $In_{0.75}Ga_{0.25}As$ lies close to conduction band. Traps below the TNL are mainly donorlike. The increase in donor traps gives a larger positive interface charge at flatband condition, which tends to facilitate inversion. As a result, the measured threshold voltage for the 600 °C annealed devices shift to negative gate voltage. Note that negative threshold voltage shift is unfavorable for enhancement-mode operation because it dramatically increases the off-state current at $V_{gs} = 0$. This conclusion could be used to explain the low V_T of the gate-first self-aligned InGaAs devices reported before in Refs. 6, 8, 12.

Similar results have been reported in a recent $In_{0.53}Ga_{0.47}As$ MOS capacitor study.[18] In their experiment, the thermal budget for the sulfur passivated surface is 500 °C for the gate-last and 700 °C for the gate-first scheme. MOS capacitors with the gate-first process are found to have much larger interface trap density (D_{it}) than gate-last samples for both Al_2O_3 gated and HfO_2 gated capacitors. This suggests that the sulfur monolayer remains intact with thermal processing temperature up to 500 °C, consistent with our device-level results.

In summary, $(NH_4)_2S$ treated InGaAs surface is susceptible to thermal instability with process temperature higher than 400–500 °C, which could cause a significant negative V_T shift and degradation in off-state performance. This can be prevented in the gate-last process by lowering the thermal budget after ALD gate dielectric growth. In the gate-first configuration, however, the thermal budget is dominated by the relatively high source and drain activation temperature with a typical temperature of 600 °C or higher for In-rich InGaAs. Thus $(NH_4)_2S$ treatment is inapplicable to the gate-first self-aligned In-rich InGaAs enhancement-mode MOSFET process. Although the S-doping effect may cause integration problems with the gate-first process, it does offer a potential solution to ultra-shallow *n*-type source and drain junctions and simple V_T adjustment scheme for InGaAs MOSFET design. Further research on utilizing this S-doping concept is on-going.

III. GATE-FIRST SELF-ALIGNED PROCESS

A. *Experiment details*

Figure 6 shows the schematic cross section and the fabrication process flow of a gate-first self-aligned $In_{0.65}Ga_{0.35}As$ MOSFET using conventional Ni/Au as metal gate. A 500 nm

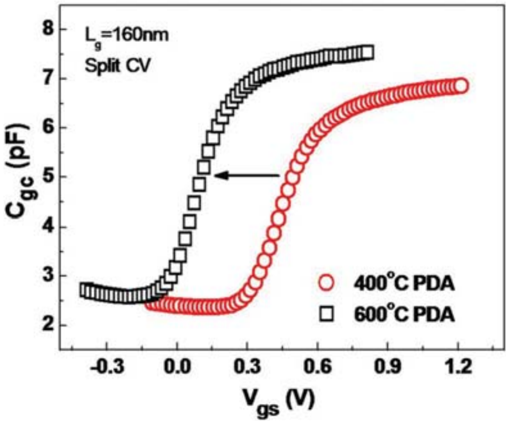

FIG. 3. (Color online) Split CV measurement of an $L_g = 160$ nm gate-last $In_{0.75}Ga_{0.25}As$ MOSFET. The inversion threshold shifts ~0.3 V to a negative gate voltage for 600°C PDA condition, with a ~10% increase in C_{gc}.

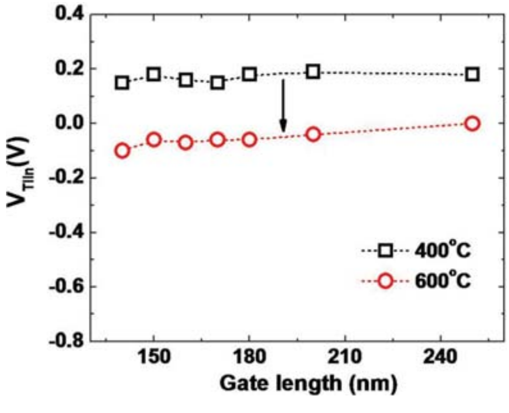

FIG. 4. (Color online) Linear extrapolated ($V_{ds} = 50$ mV) threshold voltage for a gate-last $In_{0.75}Ga_{0.25}As$ MOSFET with various gate lengths. A consistent −0.3 V V_T shift is observed for all devices after 600°C PDA.

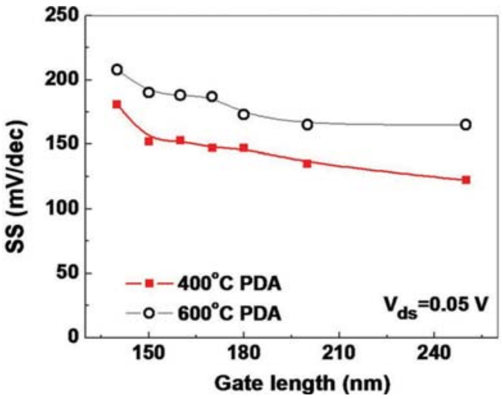

FIG. 5. (Color online) Subthreshold swing of a gate-last $In_{0.75}Ga_{0.25}As$ MOSFETs with 400 or 600°C PDA after gate oxide deposition, showing a ∼20% degradation at 600°C PDA condition.

p-doped 4×10^{17} cm^{-3} buffer layer, a 300 nm p-doped 1×10^{17} cm^{-3} $In_{0.53}Ga_{0.47}As$ and a 20 nm strained 1×10^{17} cm^{-3} $In_{0.65}Ga_{0.35}As$ channel layer were sequentially grown by MBE on a 2-inch InP p+substrate. After BOE and NH_4OH pregate treatment, a 5 nm ALD Al_2O_3 gate dielectric was deposited at a substrate temperature of 300 °C. Then 100nm thick Ni/Au gate electrode was defined through EBL, electron beam evaporation and lift-off process. The defined gate line has a width varying from 100 to 300 nm. After defining the source and drain active region, Si implantation was performed at an energy of 20 keV and a dose of 1×10^{14} cm^{-2}. Here the 100 nm thick metal gate was used to block the incoming implanted ions in a self-aligned fashion. The Si implanted source and drain was activated using RTA at 600 °C for 15 s in N_2 ambient. The key reason it is possible to use Ni/Au as the metal gate instead of refractory metals in gate-first self-aligned MOSFET fabrication is that the required activation temperature for the implanted source and drain in InGaAs is as low as 600 °C. Finally, the source and drain contact and testing pads were defined and AuGe/Ni/Au ohmic metal was annealed at 320 °C for 15 s. In the gate-first self-aligned process, there is no overlap between the gate electrode and the implanted source and drain region. The top view of a finished device and the scanning electron microscopic (SEM) image of a typical Ni/Au gate line with a gate length $L_g = 150$ nm is shown in the insets of Fig. 6.

B. *Thermal budget*

In the gate-first process, the thermal budget is primarily determined by the source and drain implant activation, which is 600 °C RTA in this work. Therefore, the source and drain dopant activation temperature is crucial in the gate-first process. In our previous work (Refs. 4, 13 and 21), we have been using an activation temperature up to 750 °C. In terms of on-state performance, a higher implant anneal temperature is believed to help increase the activation efficiency and boost the drive current. However, the effect on on-current (I_{on}) and transconductance (G_m) is found to be marginal. As for the off-state performance, we have found that an activation temperature over 600 °C dramatically increases the source and drain junction leakage current. Accordingly, off-state performance such as SS and drain-induced-barrier-lowering (DIBL) degrade significantly due to the reverse biased junction leakage current. As a result, we conclude that 600 °C RTA is the optimal activation temperature for gate-first In-rich InGaAs MOSFETs as the device scales into the deep-submicron regime. Due to the reduction of the thermal budget down to 600 °C for In-rich InGaAs, we use a simple metal (Ni/Au) lift-off process to form the self-aligned metal gate for gate-first InGaAs MOSFET fabrication in this work. It is found that the Ni/Au metal gate is able to sustain the highest processing temperature of 600 °C. Detailed device performance is discussed in the next section.

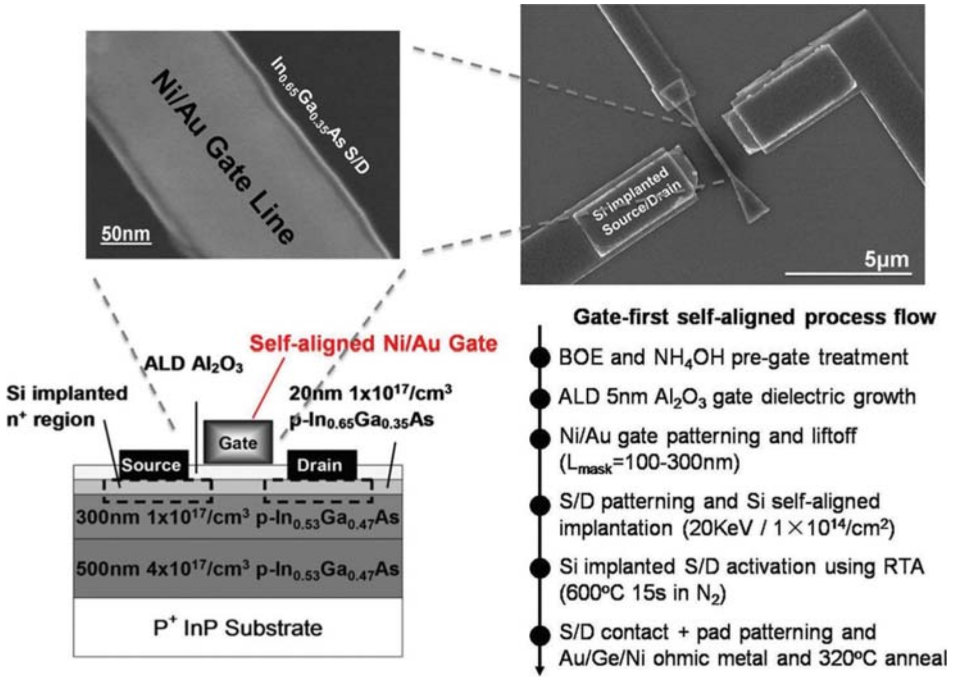
Ni/Au Gate Line
$In_{0.65}Ga_{0.35}As$ S/D
50nm
Si implanted Source/Drain
5μm
Self-aligned Ni/Au Gate
ALD Al_2O_3
Si implanted n^+ region
20nm $1x10^{17}/cm^3$ p-$In_{0.65}Ga_{0.35}As$
Gate
Source
Drain
300nm $1x10^{17}/cm^3$ p-$In_{0.53}Ga_{0.47}As$
500nm $4x10^{17}/cm^3$ p-$In_{0.53}Ga_{0.47}As$
P^+ InP Substrate
Gate-first self-aligned process flow
BOE and NH_4OH pre-gate treatment
ALD 5nm Al_2O_3 gate dielectric growth
Ni/Au gate patterning and liftoff (L_{mask}=100-300nm)
S/D patterning and Si self-aligned implantation (20KeV / $1\times10^{14}/cm^2$)
Si implanted S/D activation using RTA (600°C 15s in N_2)
S/D contact + pad patterning and Au/Ge/Ni ohmic metal and 320°C anneal

FIG. 6. (Color online) Schematic cross section and fabrication process of a self-aligned inversion-mode n-channel $In_{0.65}Ga_{0.35}As$ MOSFET with a gate-first process. Insets show the SEM images of Ni/Au gate line and top-view device structure of a typical $L_g = 150$ nm device.

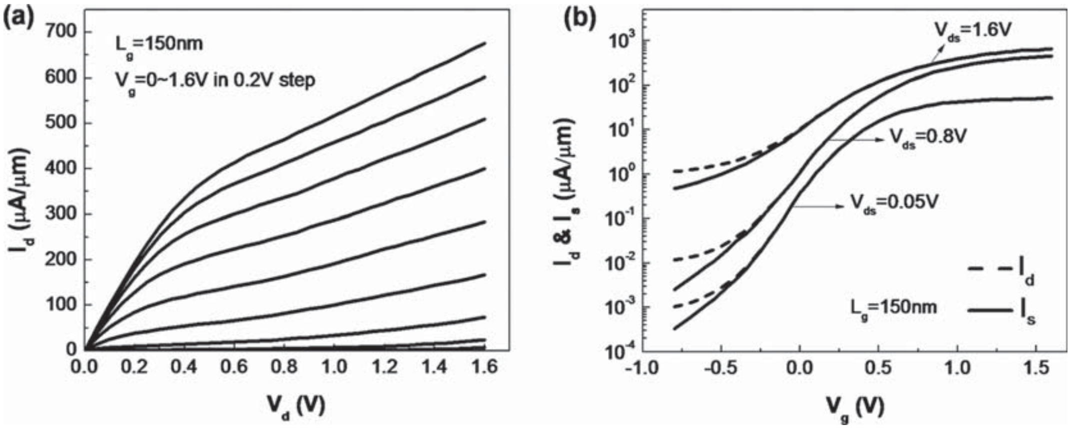

FIG. 7. (a) output and (b) subthreshold characteristics of an $L_g = 150$ nm gate-first self-aligned $In_{0.65}Ga_{0.35}As$ MOSFET with Ni/Au metal gate.

C. *Scaling metrics study of gate-first deep-submicron $In_{0.65}Ga_{0.35}As$ MOSFETs*

Figure 7(a) shows the output characteristic of a typical 150-nm gate-length self-aligned $In_{0.65}Ga_{0.35}As$ MOSFET. The maximum supply voltage V_{DD} is 1.6V. The on-current at a gate voltage of $V_{gs} = V_{ds} = 1.6$ V is 675 μA/μm. The same device exhibits a maximum extrinsic transconductance G_m of 620 μS/μm at $V_{ds} = 1.6$ V. The threshold voltage extracted using linear extrapolation at $V_{ds} = 50$mV is 0.33V for this particular device. Figure 7(b) shows the subthreshold characteristic of drain current I_d and the source current I_s vs V_{gs} for the same device. The discrepancy of I_d and I_s at negative gate bias is due to the reverse biased drain junction leakage current as discussed in the previous section. Devices with gate lengths smaller than 140 nm cannot be turned off due to the short-channel effect (SCE).[22] Thus the scaling metrics of gate-first $In_{0.65}Ga_{0.35}As$ MOSFETs with gate lengths varying only from 140 to 300 nm is summarized in Fig. 8, including I_{on}, G_m, V_T, SS, and DIBL. The on-state performance does not scale linearly in the deep-submicron regime due to the impact-ionization enhancement in I_{on} for shorter gate length devices. Devices with different gate lengths are all operated in enhancement-mode with the threshold voltage V_T of

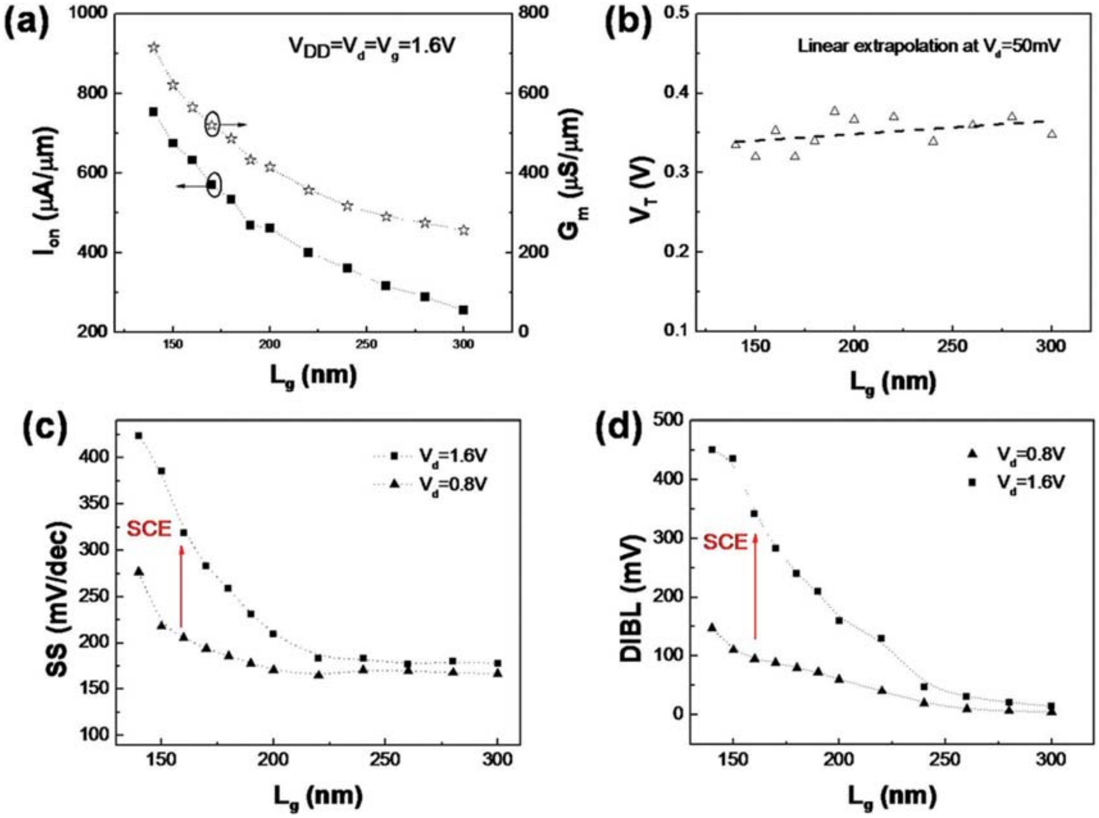

FIG. 8. (Color online) (a) on-current and peak transconductance at $V_{DD} = 1.6$V (b) linear extrapolated ($V_d = 50$mV) threshold voltage (c) subthreshold swing (SS) and (d) drain-induced barrier (DIBL) scaling metrics for gate-first self-aligned $In_{0.65}Ga_{0.35}As$ MOSFET with Ni/Au metal gate.

0.32–0.38 V, measured from the transfer characteristics in linear region at drain-source voltage $V_{\mathrm{ds}} = 50$ mV. To minimize the effect of process-induced threshold voltage variation, the V_{T} shown here is averaged from 10 devices in various dies for each gate length. For gate lengths larger than 200 nm, SS saturates at about 170 or 180 mV/dec when drain voltage is biased at 0.8 or 1.6 V, which is mainly limited by interface traps. These relatively large SS values induced by interface states significantly limit the off-current of the transistor. Greater efforts should be placed on developing new pre-gate and post-gate interface passivation techniques to meet the state-of-the-art Si industry standard. For gate lengths smaller than 200 nm, SS increases dramatically at a high drain bias ($V_{\mathrm{d}} = 1.6$ V), due to the enhanced SCE. This portion of the off-state degradation can be improved by decreasing interface traps, reducing the equivalent oxide thickness,[14] or introducing three-dimensional (3D) device structures, such as FinFETs,[23] to achieve better electrostatic control of the channel. On the other hand, devices with L_{g} greater than 250 nm have reasonable off-state performance without suffering from DIBL. The off-state performance for the gate-first InGaAs MOSFETs is comparable to our previous results using the gate-last process[14,22] with 5 nm Al_2O_3 gate oxide. No significant degradation of interface quality is introduced by the gate-first self-aligned process using conventional metal gate.

To continue the device scaling of InGaAs MOSFETs, the key challenge is how to form an aggressively scaled dielectric (EOT$\sim$1nm) that effectively passivates the interface states, which allows a steep subthreshold slope. Similar to Si MOSFETs, the continuous shrinking of the InGaAs device dimension requires that more sophisticated processing should be introduced, such as advanced doping profile, multi-gate, thin-body structure, etc., to ensure the electrostatic control of the channel and the ability to tune the threshold voltage. However, our study shows that particular attention needs to be paid on the thermal budget in fabricating InGaAs MOSFETs so as to fully benefit from the intrinsic high mobility of the channel material.

IV. CONCLUSION

In conclusion, the thermal budget of gate-last and -gate-first process in In-rich InGaAs MOSFET fabrication is systematically investigated. It is found that sulfur passivation technique is incompatible with the gate-first self-aligned process, which causes a significant negative V_{T} shift and degrades the off-state performance. We have demonstrated a gate-first self-aligned deep-submicron $In_{0.65}Ga_{0.35}As$ MOSFET process without $(NH_4)_2S$ treatment. A complete device scaling metrics study has been carried out with no significant interface quality degradation induced by the gate-first process. To further boost the device performance, a new passivation technique compatible with gate-first self-aligned process is needed, together with more aggressive gate-dielectric scaling and the implementation of 3D device structure to alleviate the SCE.

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[1] P. D. Ye, G. D. Wilk, J. Kwo, B. Yang, H.-J. L. Gossmann, M. Frei, S. N. G. Chu, J. P. Mannaerts, M. Sergent, M. Hong, K. Ng, and J. Bude, IEEE Electron Device Lett. **24**, 209 (2003).

[2] Y. Xuan, Y. Q. Wu, and P. D. Ye, IEEE Electron Device Lett. **29**, 296 (2008).

[3] J. P. de Souza, E. Kiewra, Y. Sun, A. Callegari, D. K. Sadana, G. Shahidi, D. J. Webb, J. Fompeyrine, R. Germann, C. Rossel, and C. Marchiori, Appl. Phys. Lett. **92**, 153508 (2008).

[4] Y. Xuan, Y. Q. Wu, T. Shen, T. Yang, and P. D. Ye, Tech. Dig. - Int. Electron Devices Meet. 637 (2007).

[5] D. Shahrjerdi, T. Rotter, G. Balakrishnan, D. Huffaker, E. Tutuc, and S. K. Banerjee, IEEE Electron Device Lett. **29**, 557 (2008).

[6] I. Ok, H. Kim, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao, D. Garcia, P. Majhi, N. Goel, W. Tsai, C. K. Gaspe, M. B. Santos, and J. C. Lee, Appl. Phys. Lett. **92**, 202903 (2008).

[7] H.-C. Chin, M. Zhu, C.-H. Tung, G. S. Samudra, and Y.-C. Yeo, IEEE Electron Device Lett. **29**, 553 (2008).

[8] J. Q. Lin, S. J. Lee, H. J. Oh, G. Q. Lo, D. L. Kwong, and D. Z. Chi, IEEE Electron Device Lett. **29**, 977 (2008).

[9] S. Koveshnikov, N. Goel, P. Majhi, H. Wen, M. B. Santos, S. Oktyabrsky, V. Tokranov, R. Kambhampati, R. Moore, F. Zhu, J. Lee, and W. Tsai, Appl. Phys. Lett. **92**, 222904 (2008).

[10] F. Ren, J. M. Kuo, M. Hong, W. S. Hobson, J. R. Lothian, J. Lin, H. S. Tsai, J. P. Mannaerts, J. Kwo, S. N. G. Chu, Y. K. Chen, and A. Y. Cho, IEEE Electron Device Lett. **19**, 309 (1998).

[11] R. J. W. Hill, D. A. J. Moran, X. Li, H. Zhou, D. Macintyre, S. Thoms, A. Asenov, P. Zurcher, K. Rajagopalan, J. Abrokwah, R. Droopad, M. Passlack, and I. G. Thayne, IEEE Electron Device Lett. **28**, 1080 (2007).

[12] T. D. Lin, H. C. Chiu, P. Chang, L. T. Tung, C. P. Chen, M. Hong, J. Kwo, W. Tsai, and Y. C. Wang, Appl. Phys. Lett. **93**, 033516 (2008).

[13] Y. Xuan, T. Shen, M. Xu, Y. Q. Wu, and P. D. Ye, Tech. Dig. - Int. Electron Devices Meet. 371 (2008).

[14] Y. Q. Wu, M. Xu, R. S. Wang, O. Koybasi, and P. D. Ye, Tech. Dig. - Int. Electron Devices Meet. 323 (2009).

[15] M. Radosvljevic, B. Chu-Kung, S. Corcoran, G. Dewey, M. K. Hudait, J. M. Fastenau, J. Kavalieros, W. K. Liu, D. Lubyshev, M. Metz, K. Millard, N. Mukherjee, W. Rachmady, U. Shah, and Robert Chau, Tech. Dig. - Int. Electron Devices Meet. 319 (2009).

[16] D. Lin, G. Brammertz, S. Sioncke, C. Fleischmann, A. Delabie, K. Martens, H. Bender, T. Conard, W. H. Tseng, J. C. Lin W. E. Wang, K. Temst, A. Vatomme, J. Mitard, M. Caymax, M. Meuris, M. Heyns, and T. Hoffmann, Tech. Dig. - Int. Electron Devices Meet. 327 (2009).

[17] U. Singisetti, M. A. Wistey, G. J. Burek, A. K. Baraskar, B. J. Thibeault, A. C. Gossard, M. J. W. Rodwell, B. Shin, E. J. Kim, P. C. McIntyre, B. Yu, Y. Yuan, D. Wang, Y. Taur, P. Asbeck, and Y.-J. Lee, IEEE Electron Device Lett. **30**, 1128 (2009).

[18] H. Zhao, J. Huang, Y.-T. Chen, J. H. Yum, Y. Wang, F. Zhou, F. Xue, and J. C. Lee, Appl. Phys. Lett. **95**, 253501 (2009).

[19] M. Milojevic, C. L. Hinkle, F. S. Aguirre-Tostado, H. C. Kim, E. M. Vogel, J. Kim, and R. M. Wallace, Appl. Phys. Lett. **93**, 252905 (2008).

[20] P. T. Chen, Y. Sun, E. Kim, P. C. McIntyre, W. Tsai, M. Garner, P. Pianetta, Y. Nishi, and C. O. Chui, J. Appl. Phys. **103**, 034106 (2008).

[21] J. C. Ho, A. C. Ford, Y.-L. Chueh, P. W. Leu, O. Ergen, K. Takei, G. Smith, P. Majhi, J. Bennett, and A. Javey, Appl. Phys. Lett. **95**, 072108 (2009).

[22] Y. Q. Wu, W. K. Wang, O. Koybasi, D. N. Zakharov, E. A. Stach, S. Nakahara, J. C. M. Hwang, and P. D. Ye, IEEE Electron Device Lett. **30**, 700 (2009).

[23] Y. Q. Wu, R. S. Wang, T. Shen, J. J. Gu, and P. D. Ye, Tech. Dig. - Int. Electron Devices Meet. 331 (2009).