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Effects of temperature variation (300–600 K) in MOSFET modeling in 6H–silicon carbide

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Abstract

Silicon carbide (SiC) based devices perform very well in severe environments and show excellent device characteristics at very high temperatures and in high radiation environments. An analytical model for a lateral MOSFET that includes the effects of temperature variation in 6H–SiC poly-type has been developed. The effects of elevated ambient and substrate temperatures (300–600 K) on the electrical characteristics as well as the variation of large and small signal parameters of the lateral MOSFET have been studied. The model includes the effects of temperature on the threshold voltage, carrier mobility, the body leakage current, and the drain and source contact region resistances. The MOSFET output characteristics and parameter values have been compared with previously measured experimental data. A good agreement between the analytical model and the experimental data has been observed.
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Keywords: High temperature MOSFET; Silicon carbide; Temperature variation effect

1. Introduction

The theoretical as well as the practical limitations of silicon for high temperature electronics have lead to the search for suitable materials that operate reliably at high temperatures. A systematic investigation of silicon devices for high temperature electronics (MOSFETs as well as CMOS technology) was reported by Shoucair and co-workers [1–5]. The fundamental (intrinsic) requirements of semiconductor materials for high power and high temperature applications can be summarized as: large breakdown voltage, large saturated electron drift velocity, small dielectric constant, reasonably high electron mobility, small on-resistance, and high thermal conductivity. All these requirements cannot be fulfilled by silicon. The maximum tolerable operating temperature for silicon devices is 150 °C. Therefore, there is a need to develop a reliable technology for severe environment, high temperature and radiation tolerant analog and digital circuits. The hybrid electric vehicles (HEV), aircraft industries, the geothermal and mining explorations, industrial process controls, and space exploration industries can benefit from this technology.

The wide band gap materials possess characteristics that are suitable for high temperature electronics. Among the wide band gap materials, silicon carbide (SiC) has received increased attention because of its potential for a wide variety of high power applications [6–9]. SiC has a high electric breakdown field (3.5×10^6 V/cm), high electron saturated drift velocity (2×10^7 cm/s), high melting point (2830 °C), and high thermal conductivity (4.9 W/cm K) that give it a great potential for high temperature and high power device applications. A summary of SiC material parameters is shown in Table 1. These features of SiC make it an attractive material not only for high power and high temperature applications but also lead to significant savings in cost and space in packaging and cooling systems for many aircraft, shipboard, and hybrid vehicle applications.

MOSFETs are widely used in amplifier design, analog ICs, digital CMOS design, power electronics and

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Table 1
Comparison of Si and SiC material properties [9]

Properties	Si	6H–SiC	4H–SiC
Band gap (eV)	1.11	2.9	3.2
Dielectric constant	11.8	9.7	9.7
Breakdown field (V/cm)	6×10^5	35×10^5	35×10^5
Saturated velocity (cm/s)	1×10^7	2×10^7	2×10^7
Electron mobility (in bulk) (cm^2/V s)	1350	380	800
Hole mobility (in bulk) (cm^2/V s)	450	95	120
Thermal conductivity (W/cm K)	1.5	4.9	4.9
Melting point (°C)	1420	2830	2830

switching devices. Diodes and MOSFETs are used as switching devices in dc–dc converters and ac drives that are extensively used in power electronics, power systems, traction drives, and HEV applications. A model for a vertical MOSFET, which is a suitable structure for a power MOSFET, has been developed and its impact on the system level benefits of SiC MOSFET has been studied and reported [10–12]. The performance of the Si-based switches is approaching the theoretical limits in high power applications due to its intrinsic material properties. SiC is an alternate material system that can be used to overcome the limitations of the Si-based switching devices and can be used in extreme environments.

The MOSFET device characteristics and circuit behavior that changes with the increase in temperature can be predicted and simulated with a suitable model. Unfortunately, no reliable MOSFET device model has been reported that includes the effects of change in temperature. Temperature dependency of model parameters of 6H–SiC MOSFET was explained from measured data [13]. Some empirical relations for MOSFET parameters i.e. threshold voltage, mobility etc. have also been extracted from experimental data [13]. A CMOS process has been developed, fabricated and tested in 6H–SiC [14]. The measured data for NMOS and PMOS output characteristics, transfer characteristics, threshold voltage, and sheet resistances were reported in [14]. This paper presents an analytical model for lateral MOSFET in 6H–SiC that includes the effects of temperature. The aim of this model is to establish a relationship between the MOSFET's output characteristics and temperature while explaining the factors affecting it at high temperature. The model includes the effects of temperature on the threshold voltage, carrier mobility, the body leakage current, and the drain and source contact region resistances. Output characteristics and temperature dependent parameters have been evaluated using the proposed model with the device dimensions described in [14]. Preliminary results from the analytical model and measured data presented in [14] demonstrate the feasibility of the developed model.

2. Proposed model

A detailed and intensive study has been made on different MOSFET device parameters and device behaviors, and the temperature dependent terms were determined from the study. Changes in material properties with temperature as well as the contribution to the output current due to the physical structure of MOSFET have been taken into consideration. A large-signal model for a lateral MOSFET with temperature compensation has been proposed (Fig. 1). The temperature dependent compensating current elements are considered to be in parallel with the MOSFET channel between the drain and the source. These currents contribute to the total current at high temperature. The three compensating current elements are (i) the body leakage current, I_R; (ii) current change due to the threshold voltage change, I_{TH}; (iii) current change due to the change of drain and source contact region resistance, I_{RDS}. Room temperature (300 K) has been taken as the reference temperature. MOSFET channel current, I_D has been calculated at room temperature using Eqs. (1) and (2) which are obtained from MOSFET charge sheet model [15]. Channel current, I_D is kept constant for all temperature. The compensating currents incorporate the change in MOSFETs current.

$$I_D = \frac{W}{L}\mu_n C_{ox}[(V_{GS} - V_{TH}) - V_{DS}/2]V_{DS}, \tag{1}$$

$$I_{D\,sat} = \frac{W}{2L}\mu_n C_{ox}(V_{GS} - V_{TH})^2, \tag{2}$$

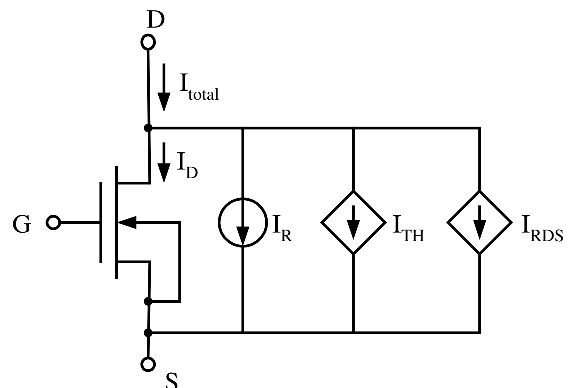

Fig. 1. MOSFET model with temperature compensation.

Table 2
List of abbreviations used in equations

I_D	Drain current in linear region operation
$I_{D\,sat}$	Drain current in saturation region operation
I_R	Body leakage current
I_{TH}	Current due to threshold voltage change
I_{RDS}	Current due to drain and source contact resistance change
V_{GS}	Gate to source voltage
V_{DS}	Drain to source voltage
V_{TH}	Threshold voltage at room temperature
$V_{TH'}$	Threshold voltage at elevated temperature
V_{fbo}	Flat band voltage
V_0	Constant
R_{DS}	Drain and source contact resistance at room temperature
$R_{DS'}$	Drain and source contact resistance at elevated temperature
W	MOSFET channel width
L	MOSFET channel length
N_A	Doping concentration of the acceptor atoms
μ_n	Electron mobility
C_{ox}	Oxide capacitance
α	Proportionality constant
β	Multiplying factor
n_i	Intrinsic carrier concentration
N_c	Density of states in the conduction band
N_v	Density of states in the valance band
E_g	Band gap
E_f	Fermi energy level
E_i	Intrinsic energy level
Φ_f	Surface potential
Φ_m	Band bending on metal side
Φ_s	Band bending on semiconductor side
Φ_{ms}	Difference between metal and semiconductor band bending
k	Boltzmann constant
T	Temperature
ΔQ_{it}	Interface state density
χ_{SiC}	Work function for SiC
D_n	Diffusion coefficient
L_n	Diffusion length
q	Electron charge
A	Cross-sectional area of *pn* junction
N	Doping density
Q_f	Fixed oxide charge
Q_{it}	Charge trapped in interface states

where symbols have their usual meaning. Eq. (1) is used in the linear region operation and Eq. (2) is used in the saturation region operation of the MOSFET. A list of symbol abbreviations is shown in Table 2.

The total drain current can be expressed by Eq. (3) as

$$I_{total} = I_D + I_R + I_{TH} + I_{RDS}, \tag{3}$$

where

$$I_R = qA\frac{D_n n_i^2}{L_n N_A}\alpha A T^3 \exp\left\{-\frac{E_g}{kT}\right\}, \tag{4}$$

$$I_{TH} = \frac{W}{L}\mu_n C_{ox}[V'_{TH} - V_{TH}]V_{DS}, \tag{5}$$

$$I_{TH_{sat}} = \frac{W}{2L}\mu_n C_{ox}\left[(V_{GS} - V'_{TH})^2 - (V_{GS} - V_{TH})^2\right], \tag{6}$$

$$I_{RDS} = \beta\left(\frac{1}{R'_{DS}} - \frac{1}{R_{DS}}\right)V_{DS}. \tag{7}$$

The change in current due to the change in threshold voltage is evaluated by Eq. (5) for linear region operation and by Eq. (6) for saturation region operation. At room temperature, I_R is negligible; I_{TH} and I_{RDS} become zero. However, with the increase in temperature, compensating terms contribute to the total current. The major factors of the compensating currents are discussed in the following sections.

2.1. Leakage currents

Body leakage current is proportional to intrinsic carrier concentration, n_i. At room temperature, n_i of SiC is very low. Thus, the contribution of the leakage current is negligible. However, with the increase in temperature, n_i increases exponentially. Therefore, leakage current contributes to the total current at high temperature. Let us consider the large-signal model of the lateral MOSFET as shown in Fig. 2 with the effect of leakage currents. The drain to body leakage current is invariably found to be due to the diffusion across the reverse biased *pn* junction under consideration. For an n-channel MOSFET device, the temperature dependence of the leakage current can be expressed by Eq. (4), which is basically the reverse saturation current of a diode [3]. The term $1/T$ inside the exponent bracket is the dominant temperature factor compared to the T^3 outside the bracket. Here, q is the electron charge, A is the area of the *pn* junction, and α is the proportionality factor. The existence of the leakage current can be shown in the large-signal MOSFET model by placing a diode between the drain and the body terminal. The electrical large-signal model is thus equivalent to adding a temperature dependent current source between the drain and the source terminals.

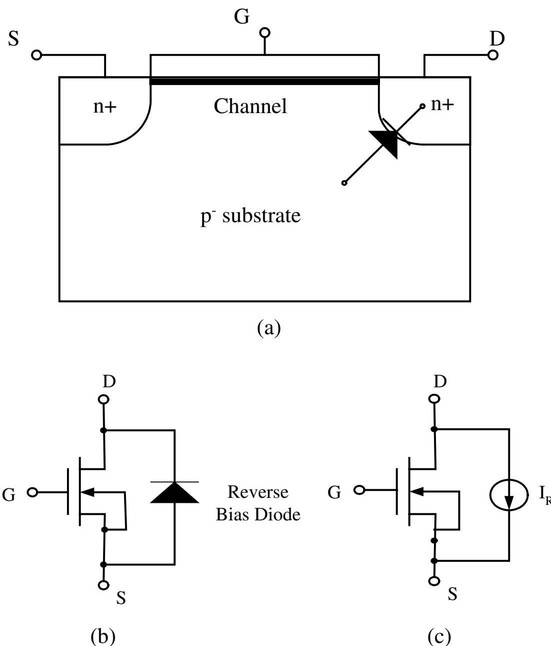

Fig. 2. Large signal model of n-channel MOSFET including the effect of leakage currents: (a) physical structure, (b) equivalent transistor, (c) electrical model.

2.2. Threshold voltage

Threshold voltage is the most significant parameter in the study of temperature dependence of MOSFET characteristics. MOSFET current–voltage characteristics are proportional to the square of the difference of gate voltage and threshold voltage. Thus, a small change in threshold voltage causes a large change in the output current. Therefore, it is very important to calculate the threshold voltage accurately with temperature changes. There are many material parameters that are related to the calculation of threshold voltage, and a number of empirical relationships have been obtained from experimental data [16]. Let us consider the simple band diagram of metal oxide semiconductor as shown in Fig. 3. Threshold voltage of MOSFET can be calculated using Eq. (8):

$$V_{TH} = V_{fbo} - \frac{\Delta Q_{it}}{C_{ox}} \pm 2\Phi_f \pm \sqrt{2V_0(2|\Phi_f|)}, \tag{8}$$

where Φ_f is the surface potential, which is given by Eq. (9):

$$\Phi_f = \frac{kT}{q} \ln\left(\frac{n}{n_i}\right). \tag{9}$$

The variation of the intrinsic carrier concentration n_i with temperature is given by Eq. (10):

$$n_i = (N_c N_v)^{1/2} \exp\left(-\frac{E_g}{2kT}\right). \tag{10}$$

The density of states in the conduction band, N_c, the valence band, N_v and the bang gap energy, E_g can be obtained by Eqs. (11)–(13), respectively:

$$N_c \cong 1.73 \times 10^{16} T^{3/2}, \tag{11}$$

$$N_v \cong 4.8 \times 10^{15} T^{3/2}, \tag{12}$$

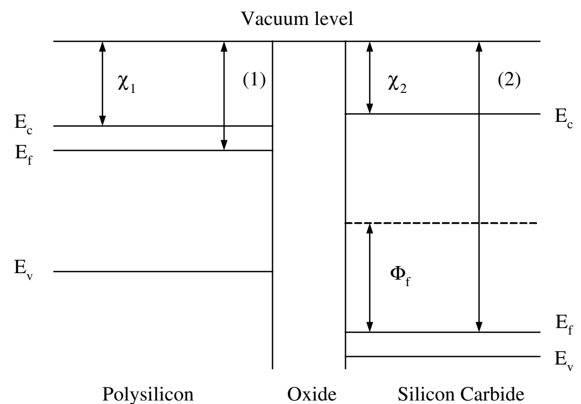

Fig. 3. Band diagram of metal–oxide semiconductor.

$$E_g \cong E_g(0) - 6.5 \times 10^{-4} \times \frac{T^2}{T+200}. \quad (13)$$

The flat band voltage also changes with temperature and can be calculated by Eq. (14), where $\Phi_{ms} = (1) - (2)$ (Fig. 3) is the difference between metal and semiconductor band bending:

$$V_{fbo} = \Phi_{ms} - \frac{Q_f}{C_{ox}} - \frac{Q_{it}(\Phi_s = 0)}{C_{ox}} = \Phi_m - \left[\chi_{SiC} + \frac{E_g}{2} + (E_f - E_i)\right] - \frac{Q_f + Q_{it}(\Phi_s = 0)}{C_{ox}}. \quad (14)$$

The interface state density, ΔQ_{it} and V_0 (Eq. (16)) are the only temperature independent parameters, which can be calculated by Eqs. (15) and (16), respectively:

$$\Delta Q_{it} = Q_{it}(2\Phi_f) - Q_{it}(0), \quad (15)$$

$$V_0 = \frac{q\varepsilon_{SiC}N}{C_{ox}^2}. \quad (16)$$

A high interface state density for SiO_2/SiC interface has been reported in [17]. The reasons for high interface state density are discussed in Section 3.

2.3. Mobility

Electrons and holes mobilities in a doped semiconductor decrease due to the increase of phonon effects with the temperature. A model for electron mobility of SiC material is shown in [18]. The model includes only the bulk mobility. However, the inversion layer mobility of SiC is much smaller than the bulk mobility. High interface state density plays an important role in inversion layer mobility. Experimentally measured mobility values in the inversion layer have been reported in [13,14]. The reported mobility values show an interesting trend in mobility. Initially, the mobility increases (which is opposite to the expected nature of mobility) for a working temperature range of 300–500 K. This may be due to the early movement of Fermi level towards the band gap with increased temperature. However, the mobility decreases at very high temperature where lattice scattering dominates and begins to release the interface trap charges. Therefore, the inversion layer mobility is almost constant over the temperature range (300–600 K) considered in the model. A constant value of mobility (21 $cm^2/V\,s$) has been used in the simulations.

2.4. Contact region resistances

The drain and the source metal contact resistances and $n+$ region sheet resistance of the MOSFET also change with temperature. It is shown in [14] that the value of sheet resistance at 600 K becomes almost half of the value at 300 K. Therefore, less voltage drop occurs at the drain and source contacts, and the channel has more drain to source voltage, which ultimately causes the drain current to increase. Fig. 4 shows the measured sheet resistance of the $n+$ contact regions of the 6H–SiC lateral MOSFET. The resistance values decrease almost linearly. Therefore, a linear approximation has been made in the calculation of the resistances. The change of resistance can be calculated by Eq. (17):

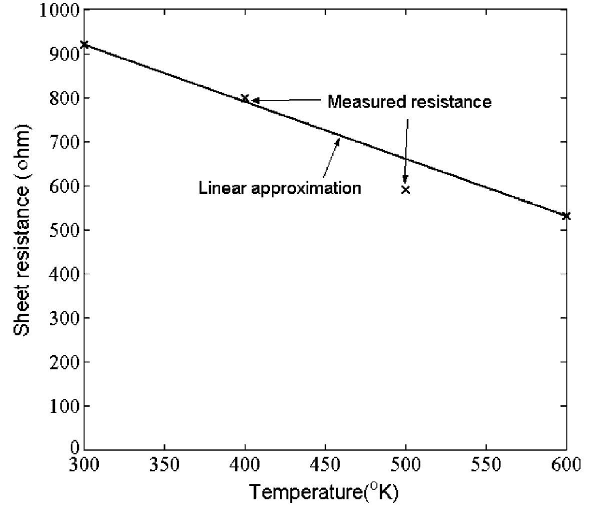

Fig. 4. Variation of sheet resistance with temperature.

$$R'_{DS} = 920 - \frac{4}{3}(T - 300). \quad (17)$$

The resistance of the metallic contact is negligible due to larger contact area. Therefore, only the change of the sheet resistance has been considered into the resistance calculation. The change in the drain and source resistances has been modeled as a change in conductance, and the effective increase in current, I_{RDS} is expressed by Eq. (7) where β is a fitting parameter to match the total current, R_{DS} is the total drain and source contact region resistance at room temperature and R'_{DS} is the total drain and source contact region resistance at elevated temperature.

3. Results and discussion

The aim of the present work is to develop an analytical model to explain and interpret the change of output characteristics with temperature for the measured data shown in [14]. The model has been evaluated in 6H–SiC material system and the same device dimensions as those of [14] are used for simulations. The output characteristics have been simulated at 300, 400, 500 and 600 K. Figs. 5 and 7 show the output characteristics for

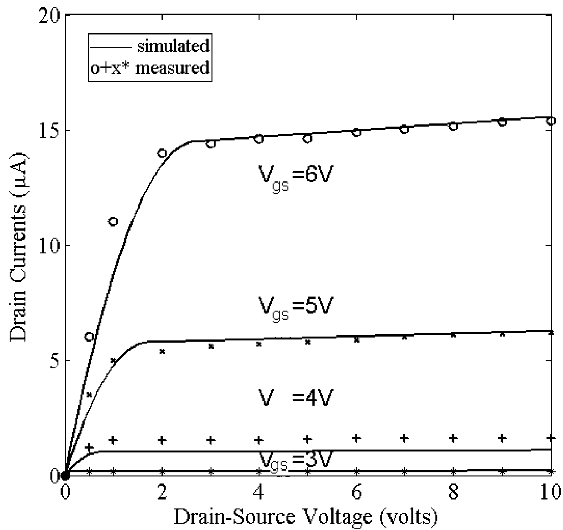

Fig. 5. Output characteristics for simulated and measured data at 300 K.

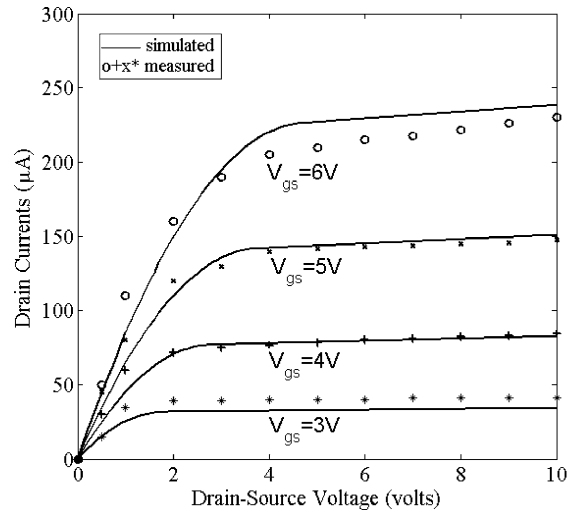

Fig. 7. Output characteristics for simulated and measured data at 600 K.

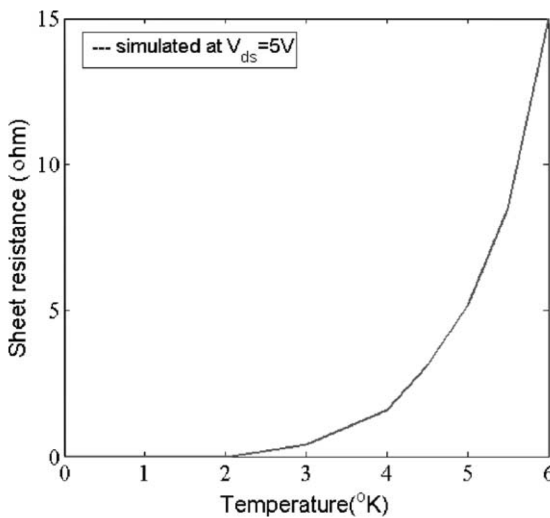

Fig. 6. Transfer characteristics simulated at drain–source voltage $V_{DS} = 5$ V, temperature 300 K.

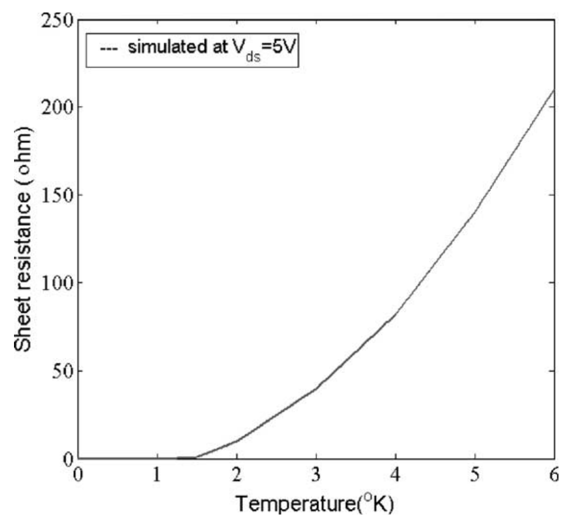

Fig. 8. Transfer characteristics simulated at drain–source voltage $V_{DS} = 5$ V, temperature 600 K.

simulated and measured data at 300 and 600 K, respectively. The simulation results match perfectly with the measured data at 300 K as compared to the results at 600 K where there are minor discrepancies. At 300 K, the drain current is 15 μA whereas it rises to 235 μA at 600 K for a gate voltage $V_{GS} = 6$ V. At room temperature, the current starts conducting through the channel at high gate voltage, $V_{GS} = 3.2$ V, whereas it starts at $V_{GS} = 1.2$ V at 600 K. The transfer characteristics are also simulated at a drain–source voltage $V_{DS} = 5$ V and are shown in Figs 6 and 8 at 300 and 600 K, respectively.

The changes in threshold voltage with temperature are also simulated and compared with measured data as shown in Fig. 9. The SiC lateral MOSFET has a very high threshold voltage i.e. 3.2 V at room temperature and 1.2 V at 600 K [14]. The large variation of the threshold voltage causes a huge change in the drain currents of the MOSFET. There are very good agreements between the results of simulated and measured threshold voltages. The contributions of the compensating currents to the total current change are evaluated at different temperatures. Table 3 shows the relative percentage of the current of the compensating terms. It

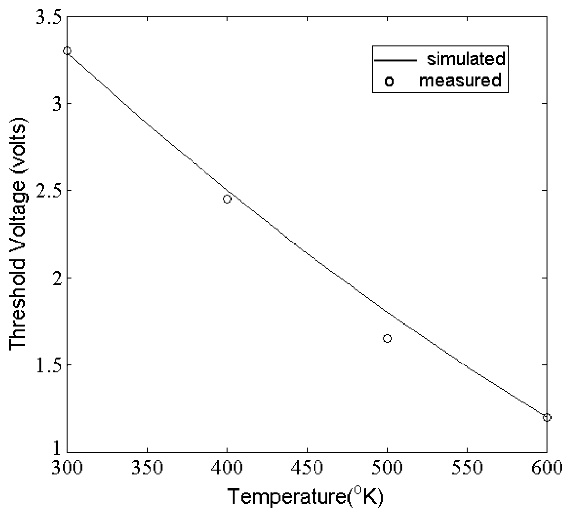

Fig. 9. Threshold voltages obtained from simulation and measurement for different temperature.

Table 3
Contribution of the compensating currents to the total current change

Temperature (K)	Total current change (μA)	% of current change due to threshold voltage	% of current change due to body leakage	% of current change due to drain source resistance
400	45	90	2	8
500	116	85	6	9
600	220	78	15	7

has been observed that most of the current change (about 85% on an average) is obtained by threshold voltage change i.e. threshold voltage mostly characterizes the device behavior. At lower temperature, contribution of the leakage current is negligible. However, at high temperature it plays a major role. Drain and source resistances change monotonously with temperature.

The high interface state density results in a high threshold voltage. The reasons for such high interface state density is expected due to the damage caused by ion implantation and high concentration of Boron atoms at the SiO_2/SiC interface. Due to low electrical activation rate, higher implantation doses are required to obtain the desired acceptor concentrations for p-well, which consequently degrades the SiO_2/SiC interface. Low activation rate for Boron implants is also the reasons for relatively low value of effective channel mobility. A large surface density and high concentration of Boron atoms at the SiO_2/SiC interface introduce more scattering of the electron in the inversion layer, lowering the effective channel mobility.

4. Conclusions

An analytical model has been developed to explain the behavior of the MOSFET output characteristics at different temperatures. The model has been evaluated for 6H–SiC material system. It includes the change in the threshold voltages, carrier mobility, the body leakage current, and the drain and source contact resistances. The MOSFET output characteristics and parameter values are compared with previously measured experimental data. There is a good agreement between the model outputs and the experimental data. The model can be used to predict the MOSFET characteristics with change of temperature.

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