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Effects of the physical parameter on gate all around FET

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Abstract. As the devices are getting compact, the size of transistors reduces day by day; however, with certain limitations. Due to miniaturization, the characteristics of the transistor change due to quantum mechanical effects and the present scenario, analytically modeled surface potential-based gate all around (GAA) FET model by solving 1-D Poisson's equation, approximation method and using necessary boundary condition. Here, the change in channel material (Si, InP, GaAs, InAs and Ge), channel radius (varied from 6 nm to 10 nm), oxide thickness (changed from 2 nm to 5 nm), drain to source voltage (varied from −0.5 V to 0.5 V), Source/Drain doping (varied from 10^{17} to $10^{22}/cm^3$) and temperature (from 0 to 300 K) of the transistor, surface potential changes from −1.6 V to 1.3 V approx. respectively, considered as the GAA FET parameters. The proposed novel model exhibits better control over hot carrier effect, Drain Induced Barrier Lowering (DIBL), reduced threshold voltage and other such short channel effects in the GAA FET. Moreover, the I–V characteristics of the GAA FET were analyzed. The MATLAB code is used for modeling of the GAA FET nanowire transistor.

Keywords. Gate all around (GAA) MOSFET; nanowire; cylindrical channel; short channel effects (SCEs).

1. Introduction

To govern Moore's law reality [1], the transistor must be scaled down from classical dimension to quantum scale by reducing the channel length, replacing low k dielectric to high k dielectrics and a new structural approach from planar MOSFET to 3D FinFET which leads to increase in the speed and reduces cost. However, with deep scaling, unwanted effects come into play; these effects are termed as short channel effects (SCEs) [2]. In SCEs, the channel length is in the order of depletion layer width of the drain and source. Due to these SCEs, the performance of the transistor is affected [3] which leads to various drawbacks like drain induced barrier lowering (DIBL), velocity saturation, hot carrier effect, threshold voltage roll-off, surface scattering and rise in leakage current [4]. Due to the DIBL effect, the gate is ineffective as there is an electrostatic decoupling between drain and source. With the decrease in on/off ratio, completely turning OFF transistor is difficult. This effect is due to the lowering of the threshold voltage. As the gate length is decreased, the electric field between source and drain increases and becomes larger. With this high value of the electric field, the proportionate relationship is violated, which leads to velocity saturation eventually leading to a decrease in the current drive. With the reduction of channel length, there is a lowering of threshold voltage, there is an increase in sub-threshold leakage current which increases power dissipation. Due to miniaturization of channel length, the surface to volume ratio increases, this is a major cause for surface effect and increases the mean free path of electrons. Hence, with an increase in surface scattering, the mobility of charge carriers degrades. The above key factor reduces the performance of the planar structure. Therefore, electrostatic veracity is improved with the increase in the number of gates for channel width and height below 10 nm. Some of the major key steps to reduce SCEs are to (a) implicate strained channel, and (b) modified the gate structures, i.e. PD-SOI-FET, and FD-SOI-FET, double gate, Fin-FET, triple gate, Pi gate, omega gate, square gate (G4) all around and cylindrical gate all around MOSFET. In double-gate MOSFET [5], there are two gates (one above the channel and the other below the channel) which shows better electrostatic potential control over the channel as compared to single gate FET. The Fin FET structure resembles a set of fins [6], which have better electrical control over the channel to reduce the leakage current and overcome other SCEs. The effective channel length of the device is determined by the thickness of the fin [7]. Triple gate FET having three gates, surrounding the three sides of the channel [8], shows the high current driving capability and better gate control over the channel up to 10 nm channel

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[9]. In Pi gate MOSFET, the gate is grown into a buried oxide and enhances electrostatic potential control in the channel and thus protecting it from the electric-field lines which are originating from the drain [10]. Omega-FET exhibits better scaling down characteristics where the gate is almost wrapped around the channel. Omega-FET is almost like GAA concerning electrical performance, but it suffers from severe corner effects [11]. The square gate has four gates (square shape) all around the channel of FET [12] and surrounds the entire channel which can reduce SCEs to some extent, but there exists another problem, i.e. corner effect. These corner effects can be reduced by using a cylindrical channel. In cylindrical gate all around MOSFET, the channel is entirely wrapped and is cylindrical. Gate all around (GAA) transistor outperforms all other multi-gate transistors due to gate wrapped all over the channel which has better electrostatic control over the channel and reduces SCEs. This shows that GAA MOSFET is the future prominent candidate for scaling down of the MOSFET and governs Moore's law [13]. In GAA MOSFET there are four gates i.e. top gate, bottom gate, and two side gates. In comparison to the double gate MOSFET, there are two additional gates so there are two additional inversion channels created which leads to allowing further scale down of FET.

In this paper, we have modeled GAA MOSFET using Poisson's equation with varying physical parameters such as channel material 'ε_t' (i.e. Si, InP, GaAs, InAs and Ge), channel radius 'r', oxide thickness 't_{ox}', gate to source voltage 'V_{GS}', drain to source voltage 'V_{DS}', Source/Drain doping 'N_D' and temperature 'T'. With these changes in the physical parameters, we have found variations in the surface potential of the transistor. Also, we have plotted the I–V characteristics curve for GAA FET.

2. Analytical modeling of gate all around nanowire transistor

The front and side views of the cylindrical GAA nanowire MOSFET structure are shown in figure 1. The structure modeled is cylindrical in shape with a nanowire channel at the center. This channel is completely wrapped with an insulator and finally with the gate.

Analytical modeling of GAA MOSFET is done by solving cylindrical Poisson's equation, parabolic approximation method, and necessary boundary conditions [14–19].

The 2-D Poisson's equation for cylindrical GAA MOSFET is given by

$$\frac{1}{r}\cdot\frac{\partial}{\partial r}\left(r.\frac{\partial}{\partial r}\varphi(r,z)\right)+\frac{\partial}{\partial z}\cdot\left(\frac{\partial}{\partial z}\varphi\right)=\frac{q.N_A}{\varepsilon_t} \tag{1}$$

where φ is the channel potential as a function of radius 'r' and channel length 'z'.

Considering the parabolic approximation, we obtain

$$\varphi(r,z)=g_0(z)+g_1(z)r+g_2(z)r^2 \tag{2}$$

where $g_0(z), g_1(z), g_2(z)$ are the coefficients as a function of 'z'.

Coefficient $g_0(z), g_1(z), g_2(z)$ in Eq. 2 can be obtained by considering the following boundary condition:

i) Electric flux at the interface of SiO_2/Si is given by

$$\frac{\partial}{\partial r}\varphi(r,z)=\frac{\varepsilon_{ox}}{\varepsilon_t}\cdot\frac{V_{GS}-V_{fb}-\varphi_s}{t_{ox}} \tag{3}$$

where V_{fb}, φ_s are flat band voltage and surface potential, respectively.

ii) The electric field at the center of the channel is zero.

$$E(r,z)|_{\cdot r=0}=0 \tag{4}$$

iii) The potential at the interfaces of the drain channel and source channel is

$$\varphi(r,0)=V_{built-in} \tag{5}$$

and

$$\varphi(r,L)=V_{built-in}+V_{DS} \tag{6}$$

where $V_{built-in}$ is built-in voltage, V_{DS} is a drain to source voltage.

By applying the above boundary condition, the surface potential for n channel is obtained as

$$\varphi_s=Ce^{kz}+De^{-kz}+\phi \tag{7}$$

where ϕ is given by

$$\phi=V_{GS}-V_{fb}-\frac{q.N_A}{\varepsilon_t.k^2} \tag{8}$$

where k is the natural length and is given by

$$k^2=\frac{2.\varepsilon_{ox}}{\varepsilon_t.R^2.\ln\left(1+\frac{t_{ox}}{R}\right)} \tag{9}$$

The coefficient C and D is given by

$$C=\frac{(V_{bi}+\phi).\left(1-e^{-kL}\right)+V_{DS}}{2\sin(kL)} \tag{10}$$

and

$$D=\frac{(V_{bi}+\phi).\left(e^{kL}-1\right)-V_{DS}}{2\sin(kL)} \tag{11}$$

The complete 2-D potential can be written as

$$\varphi(r,z)=\varphi_s+\frac{C_{ox}}{2.\varepsilon_t.R}\cdot\left(V_{GS}-V_{fb}-\varphi_s\right).\left(r^2-R^2\right) \tag{12}$$

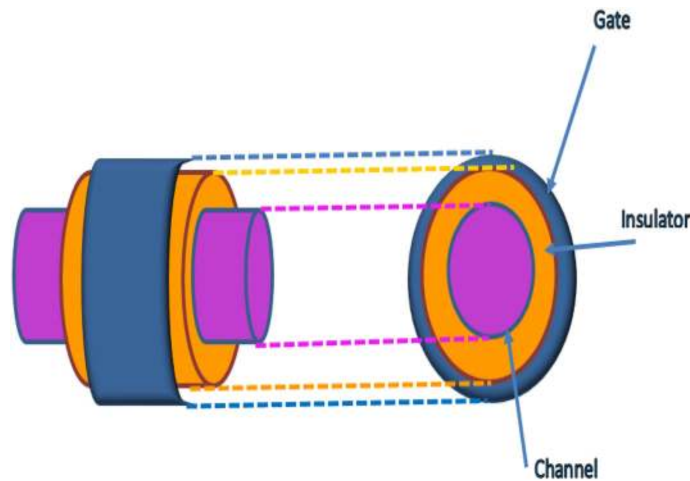

Figure 1. Schematic of gate all around nanowire transistor.

3. Results and discussion

We have considered these parameters, i.e. radius dimension R = 5 nm, oxide thickness t_{ox} = 2 nm, channel length L = 15 nm, V_{DS} = −0.1 V and V_{GS} = 1 V for simulation of the GAA nanowire MOSFET.

Figure 2 shows the plot between surface potential and channel material of GAA MOSFET with different channel

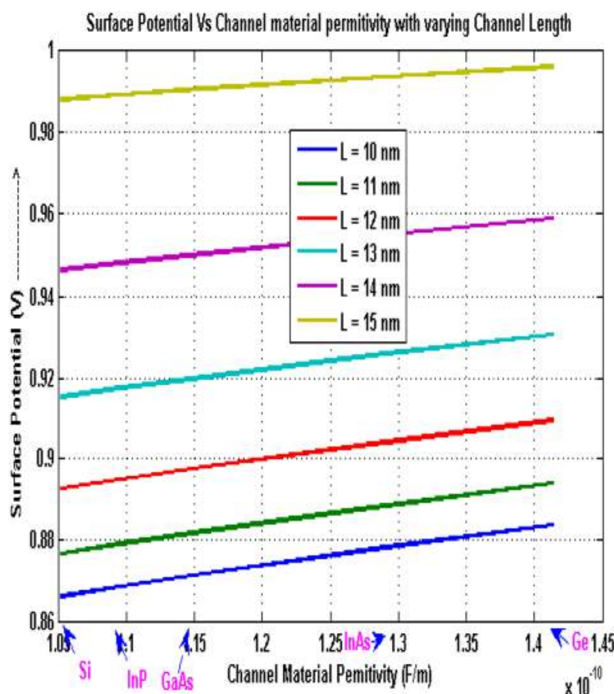

Figure 2. Surface potential vs channel material varying with channel length. Device parameter: radius R = 5 nm, oxide thickness t_{ox} = 2 nm, V_{DS} = −0.1 V and V_{GS} = 1 V, T = 300 K, channel length L varied from 10 to 15 nm and channel material Si, InP, GaAs, InAs, Ge was used. With increase of channel material permittivity, surface potential of the channel increases.

lengths. The voltage difference between the body and the gate of the device generates an electric field that controls the conductivity between source and drain. As the valence 'E_V' and conduction 'E_C' band are modified in the channel material. Due to this, there is a change in energy gap 'E_{gap}' of the material which leads to change in built-in potential 'V_{bi}' and further change in surface potential 'φ_s' of the device (given by $\varphi_s = (E_{Fi})_{surface} - (E_{Fi})_{Bulk}$ and $V_{fb} = \emptyset - \chi_m - E_c + E_F$). From Eq. 7 and Eq. 8, we find the proportional relationship between surface potential, natural length and channel permittivity. From figure 2, we analyze that, when we use Ge as channel material with permittivity 16 ε_0(F/m), the surface potential is approx. 0.89 V and with Si with permittivity 11.9 ε_0 (F/m), the surface potential is 0.86 (for a channel length of 10 nm) which shows a deviation of 0.03 V. So, with the increase of channel material permittivity, surface potential increases.

Figure 3 shows the plot between surface potential and donor concentration 'N_d' of GAA MOSFET with different channel length 'L'. With the change in doping, built-in potential (V_{bi}) changes (as given by relationship $V_{bi} = \frac{kT}{q} ln\left(\frac{N_A N_D}{n_i^2}\right)$) and as per Eq. 7 to Eq. 11, there is a change in surface potential 'φ_s'. From this figure, we investigate that with the increase of donor concentration 'N_d' the surface potential increases. When donor concentration is of 10^{17} cm^{-3} at 10 nm channel length, the surface potential is approx. 0.90 V and with donor concentration of 10^{22} cm^{-3}, the surface potential is approx. 0.93 V. The maximum of sub-threshold swing, minimum threshold voltage, and maximum leakage are observed at the same doping level. There is a deviation of 0.03 V in the surface potential to change of donor concentration. Also, with the change in channel length from 10 nm to 15 nm, the surface potential changes from 0.90 V to 1.1 V.

Figure 4 shows the plot between surface potential and channel radius of GAA MOSFET with different channel

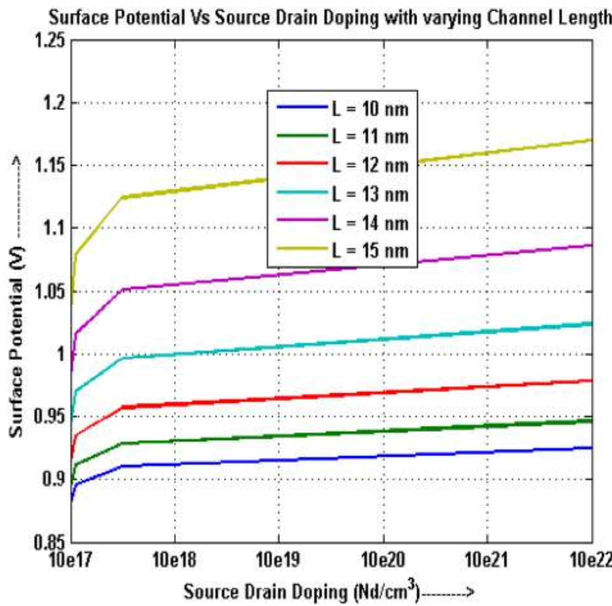

Figure 3. Surface potential vs channel length varying with N_d doping. Device parameter: radius R = 5 nm, oxide thickness t_{ox} = 2 nm, V_{DS} = −0.1 V and V_{GS} = 1 V, T = 300 K, channel length L varied from 10 to 15 nm and source/drain doping N_d varied from 10^{17} to $10^{22}/cm^3$. With the increase of source/drain doping N_d, surface potential increases.

lengths. The movement of the carriers from source to drain takes place through the channel, with the change in the physical size of the channel, i.e. length 'L' and radius 'R' in the deep sub-micron region, the characteristics of the device changes. Also, with the change in channel radius 'R', natural length changes as per the relationship $k^2 = \frac{2.\varepsilon_{ox}}{\varepsilon_t.R^2.\ln\left(1+\frac{t_{ox}}{R}\right)}$. So, with the increase in the dimension of the channel, the surface potential should also increase. From figure 4, we investigated that surface potential increases 'φ_s' with the increase of channel radius 'R' from 5 to 10 nm. The surface potential with radius 5 nm is approx. 0.87 V at 10 nm channel length and when the channel radius is 10 nm, the surface potential is approx. 0.91 V, so there is a deviation of approx. 0.04 V in surface potential. When the thin film thickness is reduced, the controllability of the gate over the channel becomes stronger in comparison with the influence exerted by the source/drain. Also, with the change in channel length from 10 to 15 nm, the surface potential changes from 0.87 V to 0.99 V, with a deviation of 0.12 V.

Figure 5 shows the surface potential of GAA MOSFET with the oxide thickness with different channel lengths. The gate oxide thickness 't_{ox}' determines the good control of the FET depending upon the oxide capacitance 'C_{ox}' of the given film. As the thickness of the oxide scales below few nanometers, leakage current '$I_{leakage}$' increases due to tunneling, leading to high power consumption and reduced device reliability. Gate capacitance 'C_{gate}' increases with the increase of oxide thickness 't_{ox}' given by $C_{ox} = \frac{\varepsilon_{ox}}{T_{ox}}A * \varepsilon_0$ and leads to further change in natural length 'k' given as $k^2 = \frac{2.\varepsilon_{ox}}{\varepsilon_t.R^2.\ln\left(1+\frac{t_{ox}}{R}\right)}$, which affects the surface potential 'φ_s'.

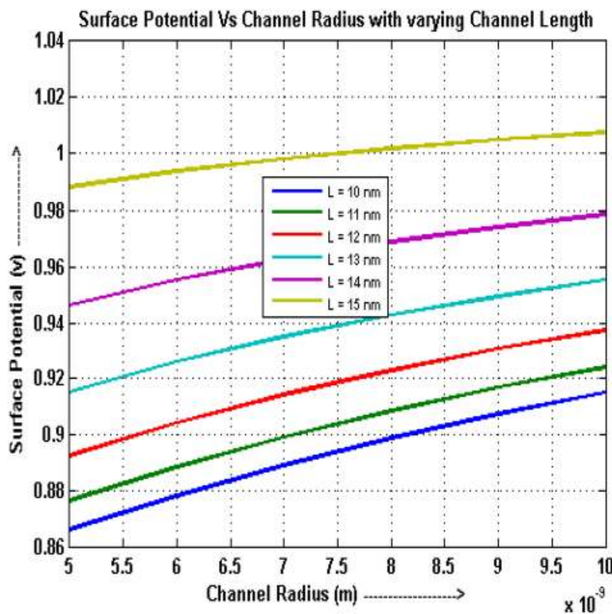

Figure 4. Surface potential vs channel radius with varying channel length. Device parameter: oxide thickness t_{ox} = 2 nm, V_{DS} = −0.1 V, V_{GS}= 1 V, T = 300 K, channel length L varied from 10 nm to 15 nm and radius R varied from 5 nm to 10 nm. With the increase of channel radius R, the surface potential of the channel increases.

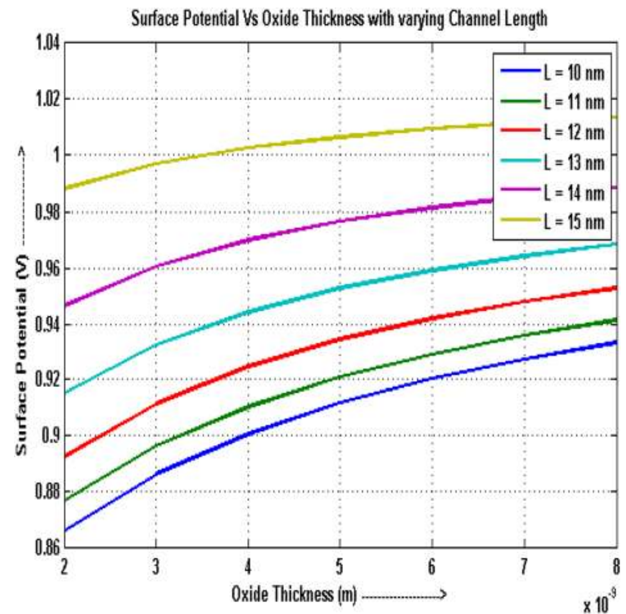

Figure 5. Surface potential vs oxide thickness varying with channel length. Device parameter: radius R = 5 nm, V_{DS} = −0.1 V, V_{GS} = 1 V, T = 300 K, channel length L varied from 10 to 15 nm and oxide thickness t_{ox} varied from 2 to 8 nm. With the increase of oxide thickness t_{ox}, the surface potential of the channel increases.

From figure 5 we observe that, when the oxide thickness is 2 nm with channel lengths 'L' of 10 nm, the surface potential is approx. 0.87 V however, when the oxide thickness is 8 nm and the surface potential is approx. 0.93 V, which shows a deviation of 0.06 V in surface potential. With the increase of oxide thickness, the surface potential also increases. Thicker oxide can be used to improve gate dielectric reliability and reduce leakage current flowing through the structure. Also, when the channel length is changed from 10 to 15 nm, the surface potential changes from 0.87 V to 0.99 V.

Figure 6 shows the surface potential varies with gate to source voltage 'V_{DS}' of GAA MOSFET with different channel length 'L' varying from 10 to 15 nm. The gate to source voltage 'V_{DS}' is an important factor for turning ON/OFF transistor. The surface potential 'φ_s' increases rapidly from −1.6 to 0.1 V as the gate to source voltage 'V_{GS}' increases from −0.5 to 0.5 V.

Figure 7 shows a plot between surface potential vs. temperature with varying channel lengths from 10 to 15 nm. With changes in temperature 'T' built-in potential (V_{bi}) changes (as given by the relationship $V_{bi} = \frac{kT}{q} ln\left(\frac{N_A N_D}{n_i^2}\right)$) and as per Eq. 7 to Eq. 11, there is a change in surface potential. The surface potential decreases from 1.27 to 0.9 V with an increase of temperature from 0 to 300 K (for 15 nm channel length) which shows a deviation of 0.37 V in surface potential. This decreasing surface potential 'φ_s' is due to the decrease of built-in potential, V_{bi} increasing with temperature. Also, we analyze that, with the change of channel length from 10 to 15 nm the surface potential changes from 0.87 to 1.27 V at 0 K, but at 300 K the surface potential changes from 0.84 to 0.9 V. So, there is a much higher change in surface potential at a temperature of 0 K than that of 300 K.

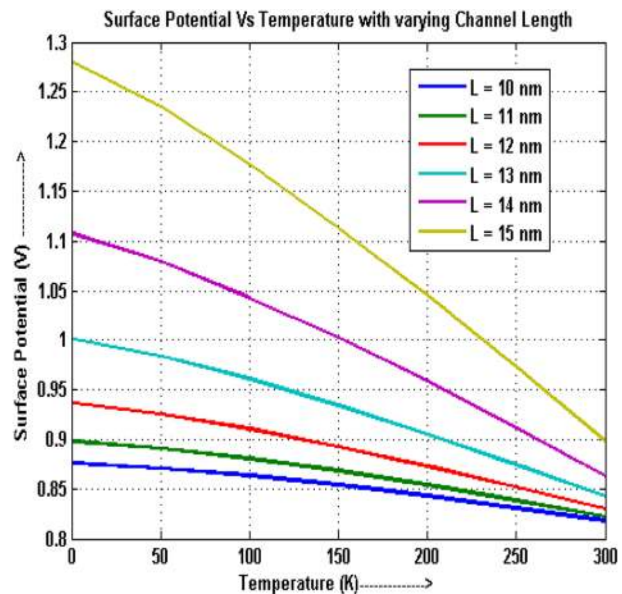

Figure 7. Surface potential vs Temperature varying with channel length. Device parameter: radius R = 5 nm, V_{DS} = −0.1 V, V_{GS} = 1 V, oxide thickness t_{ox} = 2 nm, channel length L varied from 10 to 15 nm and temperature varied from 0 to 300 K. With the increase of temperature T, the surface potential of the channel decreases.

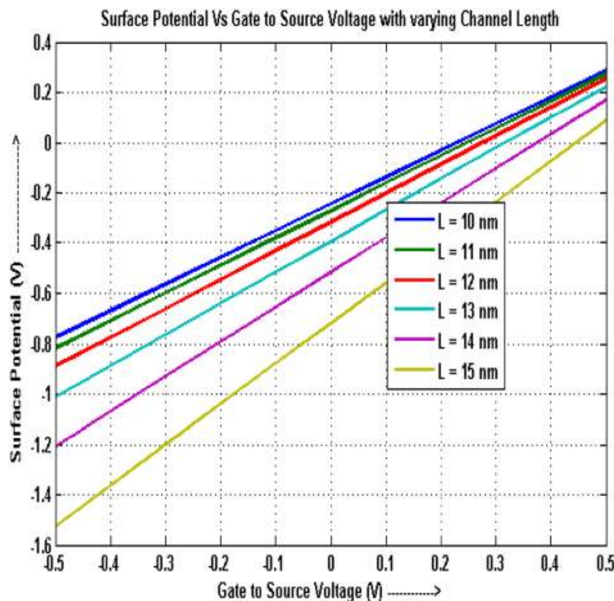

Figure 6. Surface potential vs. channel length varying with gate to source voltage. Device parameter: radius R = 5 nm, V_{DS} = −0.1 V, T = 300 K, oxide thickness t_{ox} = 2 nm, channel length L varied from 10 to 15 nm and V_{GS} varied from −0.5 V to 0.5 V. With the increase of gate to source voltage V_{GS}, the surface potential of the channel increases.

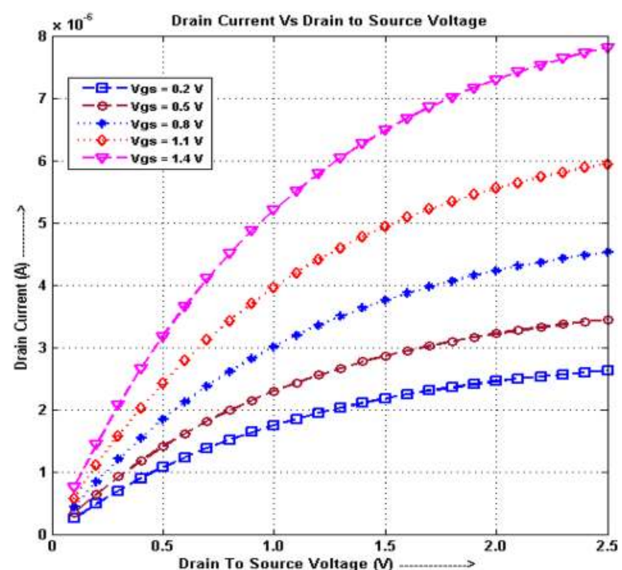

Figure 8. Drain current vs drain to source voltage varying with gate to source voltage. Device parameter: radius R = 5 nm, oxide thickness t_{ox} = 2 nm, channel length L = 10 nm and temperature = 300 K. With the increase of drain to source voltage and gate to source voltage drain current increases.

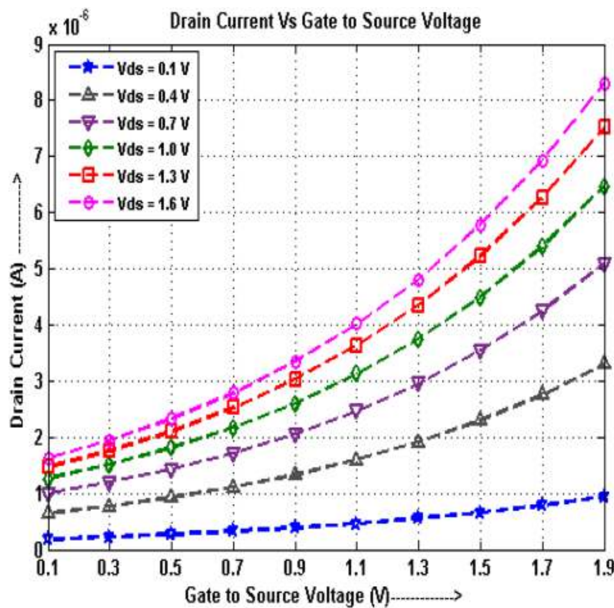

Figure 9. Drain current vs gate to source voltage varying with drain to source voltage. Device parameter: radius R = 5 nm, oxide thickness t_{ox} = 2 nm, channel length L = 10 nm and temperature = 300 K. With the increase of drain to source voltage and gate to source voltage drain current increases.

Figures 8 and 9 show output (I_D–V_{DS}) and transfer characteristics (I_D–V_{GS}) for a cylindrical gate all around FET. These figures show that with the increase of drain to source voltage and gate to source voltage drain current increases. When the gate voltage is 0.2 V and 1.4 V, drain current changes from 2.5 to 8 μA at a drain voltage of 2.5 V. When drain voltage is 0.1 V to 1.6 V, the drain current changes from 1 to 8.5 μA. From these I–V curves, we find that GAA FET shows good control over the channel.

4. Conclusion

Modeling of n-channel GAA MOSFET has been done using Poisson's equation and simulated using MATLAB code. The changes in the channel radius from 5 nm to 10 nm and 10 nm channel length, surface potential changes from 0.87 V to 0.91 V and 0.86 to 0.89 V respectively, for the channel material permittivity 11.9 ε_0 (F/m) (Si) to 16 ε_0 (F/m) (Ge). The surface potential varied from 0.87 V to 0.83 V, with a change of gate to source voltage from −0.5 to 0.5 V and the surface potential also increases −1.6 to 0.1 V at the temperature changes from 0 K to 300 K. With the analyses of change in surface potential with the variation in different physical parameters of the device, best device configuration can be accomplished, and SCEs can be reduced. Also, we have shown the output (I_D–V_{DS}) and transfer (I_D–V_{GS}) characteristics of GAA FET from which we find that with the increase of drain to source voltage and gate to source voltage, drain current increases.

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