Efficiency and Conducted EMI evaluation of a single-phase power factor correction boost converter using state-of-the-art SiC MOSFET and SiC diode

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***Abstract*—SiC-based diodes and MOSFETs switch extremely quickly with low conduction losses. Thus, from the perspective of efficiency, such devices are ideal for a continuous conduction mode (CCM) boost power factor correction (PFC) converter. However, the circuit parasitic becomes alive while switching with high dv/dt and di/dt values, which necessitates the need for EMC compliance measurements. Employing the best available low-loss SiC MOSFET and SiC diode, in this study, a 1 kW PFC boost converter prototype was designed, developed, and evaluated with the objective of quantifying the efficiency and electromagnetic compatibility signature. The efficiency is evaluated through two approaches, namely, a circuit simulation and a laboratory measurement. With the first approach, the switching losses are obtained using a widely accepted double-pulse test methodology, and the conduction losses are taken from the data sheet, whereas with the second approach, the current and voltage are recorded at the input and output of the PFC converter using power analyzer. The electromagnetic interference (EMI) is monitored using LISN and EMC analyzer. To maximize the efficiency, a fast, clean switching of the SiC is necessary. Utilizing a low-parasitic printed circuit board design approach and switching the selected low-loss SiC devices with a 0 Ω external gate drive resistance, this PFC boost yields a peak efficiency of 97.2% at full rated power when switched at 250 kHz. Furthermore, the EMI noise was measured at 66 and 250 kHz. It was found that the same EMI filter size satisfies the CISPR 11 Class B conducted EMI limit at both switching frequencies with a noise of approximately 10 dB higher at 250 kHz. As the main contribution of the present study, the best case efficiency and worst case EMI are evaluated in this study.**

***Index Terms*—AC-DC power converters, circuit simulation, electromagnetic interference, energy efficiency, power MOSFET, printed circuit board layout, Schottky diodes, silicon carbide, switching loss, wide-bandgap semiconductors.**

I. Introduction

Rectifiers for AC-DC conversion are widely used in many applications, such as switched-mode power supplies (SMPSs), pulse width modulated (PWM) motor drives, and uninterrupted power supplies (UPSs), which result in non-sinusoidal input currents with large harmonic components leading to a poor power factor [1]–[3]. This eventually entails myriad problems, for instance, interference with the communication circuits and other equipment; losses and heating of the capacitors, motors, and transformers; and an accelerated ageing of their insulation [4]–[6]. To improve the power quality, line harmonic regulations, namely, EN 61000-3-2 [7] and IEEE Std. 519-2014 [8], are established. As an example, for the bus voltage of ≤ 1 kV at the point of common coupling (PCC), the IEEE Std. 519-2014 recommends that the individual and total harmonic distortion be $\leq 5\%$ and $\leq 8\%$, respectively [8]. To comply with these standards, an active power factor correction (PFC) circuit must be used [2], [3]. However, this solution leads to an increased pollution within the 20 kHz to 1 GHz range because it involves a power electronic converter [9]. Therefore, this active PFC must also satisfy the standard for a high-frequency range; i.e., conducted (150 kHz to 30 MHz) and radiated (30 MHz to 1 GHz) noises must meet the IEC CISPR 16-1-2 regulation [10].

Aside from meeting the mandatory line harmonic requirements, as mentioned above, AC-DC power converters also require satisfying efficiency-related needs, which are enforced owing to economic and environmental concerns by various programs and organizations, such as the 80 PLUS incentive program [11], the U.S. Environmental Protection Agency's (EPA) Energy Star [12], and the Climate Saver Computing Initiative (CSCI) [13]. As an example, the 80 PLUS certification requires an efficiency of $\geq 80\%$ at 20%, 50%, and 100% of the rated load [11].

Comprehensive research into an electromagnetic interference (EMI) analysis has been carried out [14]–[20]. In [14], two separate heat sinks are proposed to achieve a better EMC performance of SiC JFET-based motor drives. Oswald *et al.* [15] compared the spectra of SiC MOSFET/SiC, SiC MOSFET/Si, and Si IGBT/Si diodes based on switching waveforms obtained from a double-pulse tester, which revealed that SiC MOSFETs generate higher EMI noise than Si IGBTs within a frequency range of 2–50 MHz. Furthermore, the reverse-recovery effect of silicon carbide (SiC) versus silicon (Si) diodes was studied in [16], in which it was concluded that parasitic oscillation during switching transients magnifies the EMI noise within the corresponding ringing frequency range in the spectra. In addition, the CM choke sizing for 20 kHz versus 200 kHz drives [17], the suppression of EMI using random modulation techniques [18], and optimal EMI filter designs [19], [20] have been reported.

To minimize the conduction loss of the diode bridge, various PFC topologies, such as a boost bridgeless PFC, totem-pole bridgeless PFC, and numerous control strategies have been proposed and analyzed [21]–[27]. Since the commercialization of an SiC Schottky barrier diode (SBD) in 2001, many authors have compared the efficiency gain brought about by SiC SBD over a Si ultra-fast boost diode, primarily focusing on minimizing the reverse-recovery loss associated with it [28]–[34]. A Si super junction MOSFET and SiC SBD were long considered ideal solid-state devices [35]–[39] until the commercialization of an SiC MOSFET in 2010. For this application, many publications have reported the use of an

SiC SBD and SiC MOSFET [40]–[46]. As the best example, a 1 kW SiC-based PFC was reported, which resulted in an efficiency of 97% when switched at 100 kHz [42]. However, in this study, a 1 kW SiC-based PFC converter is designed, developed, and evaluated using the best available low-loss SiC MOSFET and SiC diode. With the goal of fully exploiting a high switching speed and low-loss capability of SiC devices, a low inductive and capacitive printed circuit board (PCB), along with an external gate drive resistance of 0 Ω, is employed. Initially, through low-inductive measurement connections, a clean, fast switching of the chosen state-of-the-art SiC devices is accomplished. An efficiency of 97.2% is demonstrated when switched at 250 kHz. Moreover, EMC compliance was investigated for two different switching frequencies, namely, 66 and 250 kHz, the results of which revealed that the same filter size satisfies the CISPR Class B conducted EMI regulations with excellent margins. Overall, to minimize the EMI at the source, a clean switching approach of an SiC is required; to obtain the highest efficiency, a clean, fast switching of an SiC is indispensable; and to evaluate the converter EMI, a fast and high-frequency switching of SiC is the most interesting condition (the EMI is significantly aggravated using fast- and high-frequency switching). In the present study, a PFC rectifier was evaluated under such conditions, thus extending the research in this regard.

The remainder of this paper is organized as follows. A description of the converter and its specifications are presented in Section II. The hardware setup for a double-pulse test (DPT) and circuit simulation is then described in Section III, which covers the loss measurement using the DPT methodology with high-bandwidth measurement equipment and low-inductance connections. In addition, a converter loss breakdown is shown in this section. Section IV focuses on the circuit design considerations for the clean switching of SiC devices through the design and measurement of a conventional PFC converter prototype. The experiment results are presented in Section V. Finally, Section VI highlights the major conclusions of the present study.

II. Converter Description and Specifications

A conventional or classical PFC circuit consists of an input EMI filter, diode bridge, and boost converter, as shown in Fig. 1. The primary objective of this circuit is the active shaping of the input current (i_s), allowing it to be in phase with the input AC voltage (v_s), thus minimizing the harmonic distortion. The current paths when the PFC operates in a continuous conduction mode (CCM) are also illustrated in Fig. 1, which shows that the reverse current resulting from parasitic capacitance within the diode contributes to the turn-on switching loss in the MOSFET apart from the switching loss in itself.

Table I shows the specifications of the converter. The input voltage (v_s) has a range ($v_{s,min}$–$v_{s,max}$) of 85–265 V. The line frequency (f_{line}) is 50/60 Hz, the output voltage (v_{out}) is 400 V, and the output power (P_{out}) is 1 kW. The boost inductor (L_B) is specified such that the ripple current (Δi_L) is 30% at a low-line voltage (85 V) through a circuit

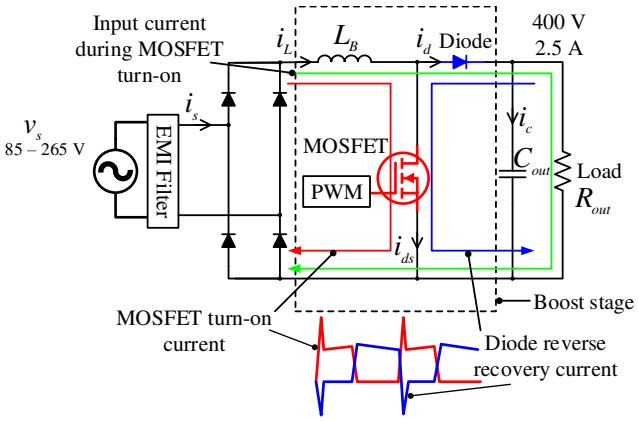


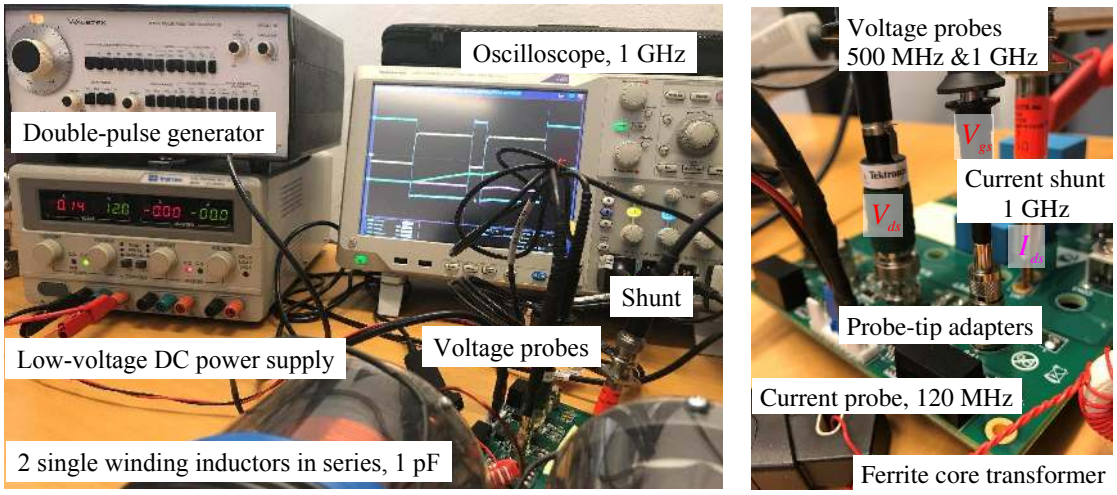
Fig. 1. Schematic diagram of an active PFC boost converter, illustrating the current paths for the MOSFET and diode in a CCM operation. During the boost diode turn-off and boost MOSFET turn-on, the reverse-recovery current in the diode not only contributes to the switching loss in itself but also to the turn-on switching loss in the MOSFET, which demands larger die devices to meet the efficiency and thermal specifications when using a diode with a large recovery charge.

simulation in MATLAB. Alternatively, the simulated value of L_B is assured through an analytical expression given in (1) [see Appendix]. The output capacitor (C_{out}) was designed to handle the double-line frequency ripple voltage (Δv_{out} = 10 V_{pp}) and meet the hold-up time requirement (t_{hold} = 16.6 ms at the minimum output voltage, $v_{out,min}$ = 350 V). Both the simulation and analytical approaches are used to guarantee the designed size. See the analytical expression used for C_{out} in (2) [Appendix]. Furthermore, the switching frequency was detected by the maximum possible value that a commercially available analog controller IC could offer. The controller IC, UCC28180, could operate in CCM mode with user programmable switching frequency of 250 kHz.

Table II shows the part number and specifications of the components, particularly chosen with the goal of maximizing the efficiency in a prototype PFC converter. The bridge diodes are based on Si technology, with the lowest V_F of the commercially available devices. Using an off-the-shelf single sendust core [47] with 85 turns of the copper wire, a boost inductor is produced that provides an inductance of approximately 424 μH at zero bias and a DC resistance (DCR)

TABLE I
Specifications of PFC Boost Converter.

Parameters	Specifications
Input voltage ($v_{s,min}$)–($v_{s,max}$)	85–265 V
Line frequency (f_{line})	50/60 Hz
Output voltage (v_{out})	400 V
Output power (P_{out})	1 kW
Switching frequency (f_{sw})	250 kHz
Boost inductor current (Δi_L)	30% @85 V, 1 kW, 250 kHz
Output voltage ripple (Δv_{out})	10 V_{pp}
Hold-up time (t_{hold})	16.6 ms @ $v_{out,min}$ = 350 V
EMI standards	CISPR 11 Class B
Efficiency regulations	80 PLUS



(a) Hardware setup. (b) Measurement arrangements.

Fig. 2. Laboratory setup showing the arrangement for current and voltage measurements of the DUT. Double-pulses are generated using a function generator. The DUT current is measured using a high-bandwidth, low-inductive-current shunt. The voltage is measured using a high-bandwidth single-ended probe, mounted to the PCB using a probe-tip adaptor for a reduction of the ground-lead inductance.

TABLE II
CHOSEN COMPONENTS WITH THEIR PART NUMBERS AND SPECIFICATIONS. THE ON-STATE PARAMETERS ASSOCIATED WITH THE DIODE, V_{FO} AND R_d, AND MOSFET, $R_{DS,on}$, ARE TAKEN AT 125 °C [48], [49].

Components	Part number	Specification
Bridge diode	GSIB2580	V_{FO} = 0.98 V, R_d = 22 mΩ
L_B	CS330060	sendust, DCR = 80 mΩ
MOSFET	C3M0065090D	$R_{DS,on}$ = 82 mΩ
Boost diode	SCS220AE2	V_{FO} = 0.8 V, R_d = 34 mΩ
C_{out}	B43508A5567M062	ESR = 220 mΩ @100 Hz

of 80 mΩ. A single-layer winding approach with multiple parallel wires is used for reducing the AC losses. The boost MOSFET and diode are based on SiC and chosen based on state-of-the-art low-loss devices. An effective series resistance (ESR) of C_{out} is 220 mΩ. The on-state parameters associated with the diode, namely, the forward voltage drop (V_{FO}) and on-state resistance (R_d), and with the MOSFET, namely, on-state resistance ($R_{DS,on}$), are taken at 125 °C, whereas those related to the inductor and capacitor are provided for 25 °C in Table II, which are the inputs for the loss calculation of the converter.

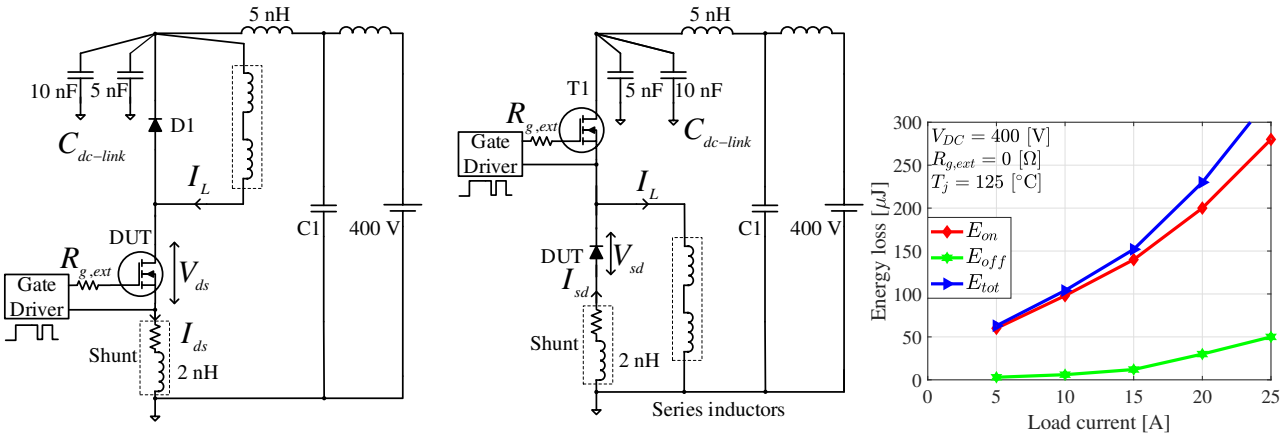
III. HARDWARE SETUP FOR DOUBLE-PULSE TEST OF SIC DEVICES AND CONVERTER LOSS BREAKDOWN

In this section, a hardware setup designed for the clean switching of an SiC MOSFET and diode is discussed. Furthermore, the connections of the measurement probes in the PCB are illustrated, which is crucial for accurately tracking the fast rising and falling transients. The switching energy loss is then quantified through DPT measurements. Finally, a circuit simulation for evaluating the converter loss breakdown is presented.

A. Hardware setup and measurement considerations

An image of the laboratory setup used for DPT measurements of the chosen devices is shown in Fig. 2. To maximize the high performance achieved by an SiC device, some of the design techniques implemented in this DPT setup are as follows. First, slits are made in the PCB between the gate, drain, and source to avoid a coupling capacitance. Second, gate and drain traces are routed either perpendicular or anti-parallel to each other to avoid inserting an external stray capacitance through the PCB. Third, a transmission-line like structure in which the negative trace runs just below the positive trace is employed in the PCB design to reduce the stray magnetic flux and EMI that occurs from leakage or stray inductance. Furthermore, the positive and negative planes are designed as polygon fills whenever possible in the PCB layout because this technique increases the size of the area. Moreover, the main power trace and switching device are placed on the bottom layer; simultaneously, the gate driver parts and the signal traces are placed on the top side of the PCB board. This arrangement minimizes the impact of high dv/dt and di/dt noises from the switching node to the gate side. In addition, small film capacitors (5–10 nF), as indicated in Fig. 3, are placed close to the SiC devices to provide a low impedance path to the fast switching signals, and the gate driver is kept as close as possible to the SiC MOSFET. In a previous study, the authors used an Ansys Q3D extractor (3D FEM simulations) to evaluate a similar low-parasitic busbar layout for SiC modules [50], the knowledge of which is implemented herein.

Fig. 2 (b) shows a detailed view of low-inductive connections used for the measurements, in which a PCB probe-tip adapter is used to minimize the ground-lead inductance associated with the return probe of a typical voltage probe. A high bandwidth voltage (P5100A, 500 MHz) and current probes (coaxial shunt, SDN-25, 1 GHz), together with a high-bandwidth oscilloscope (DPO5104B, 1 GHz), are used for capturing the fast rising and falling transients of an SiC MOS-



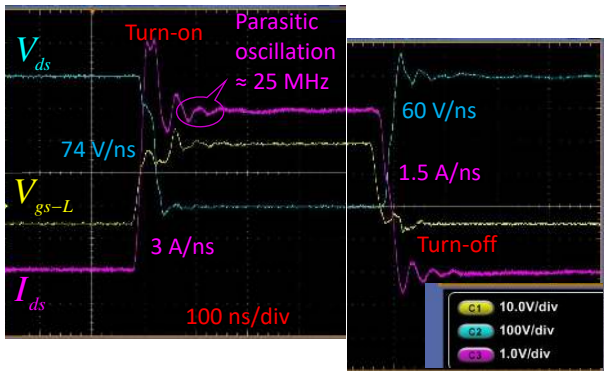
(a) DPT circuit for MOSFET. (b) DPT circuit for diode. (c) Switching energy loss of SiC MOSFET.

Fig. 3. An inductive load circuit for a hard switching test of the (a) SiC MOSFET and (b) SiC Schottky diode. Double-pulses are applied to the device under test (DUT) in (a); in contrast, they are applied to the control device (upper transistor T1) in (b). An external gate resistor ($R_{g,ext}$) is used to regulate the dv/dt and di/dt of the DUT. (c) Switching energy loss versus load current of the chosen SiC MOSFET at a V_{DC} of 400 V and a T_j of 125 °C.

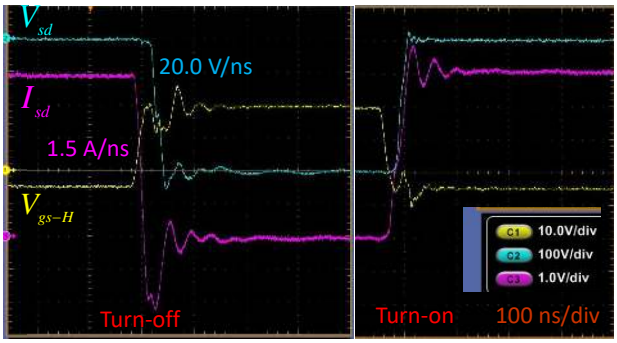
FET and SiC diode. Note that the shunt introduces a parasitic inductance of 2 nH into the circuit. After compensating for the probe delays, the recorded switching waveforms are multiplied and integrated over the defined switching time to compute the associated energy loss.

B. Switching loss measurement using DPT methodology

The dynamic performance of an SiC MOSFET was assessed using DPT methodology, in which two pulses were sent to the device under test (DUT) in a clamped inductive load circuit, as shown in Fig. 3 a). Double-pulses were generated using a function generator. By regulating the width of the first pulse and the DC-link voltage, the desired load current was achieved. Only two pulses were applied to the DUT each time; consequently, the DUT junction temperature increase from the switching loss was negligible. Fig. 3 (b) shows a schematic diagram of the DPT measurements of the SiC diode. Here, the double-pulses are fed to the upper transistor. The measured turn-on, turn-off, and total switching energy losses, namely, E_{on}, E_{off}, and E_{tot}, respectively, at a junction temperature, T_j, of 125 °C are shown in Fig. 3 (c). To monitor the junction temperature, a small hole was made in the heat sink where the device was mounted. This hole was made as close to the chip as possible to estimate the junction temperature. Moreover, such measurements were taken for a temperature range of 25–150 °C, and it was found that the influence on the losses was extremely trivial. Thus, it was concluded that the method used for the temperature measurements is sufficient for this case. A sample of the switching events for the chosen SiC MOSFET and SiC diode are depicted in Fig. 4 at a $R_{g,ext}$ of 0 Ω. These devices switch extremely quickly with very little ringing, substantiating the low inductive design described in Section III-A. Here, dv/dt within the range of 60–75 V/ns and di/dt within the range of 1.5–3 A/ns are achieved at a DC-link voltage of 400 V and a load current of 20 A. As can be seen, a parasitic oscillation of 25 MHz is observed during the switching transients.

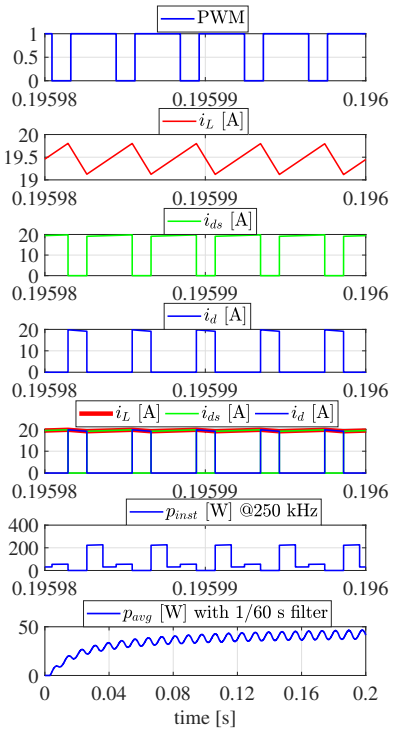


(a) Turn-on and turn-off switching transients of SiC MOSFET.

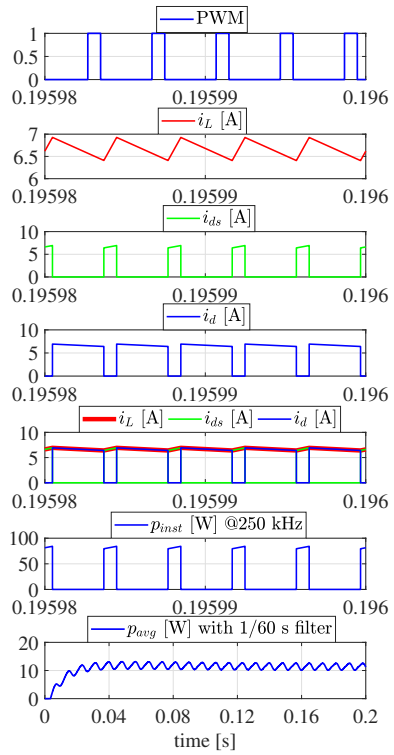


(b) Turn-on and turn-off switching transients of SiC diode.

Fig. 4. Sample of switching events of SiC MOSFET and SiC diode at a DC-link voltage of 400 V and a load current of 20 A with an external gate resistance of 0 Ω. Clearly, the overshoot and oscillations are slight in the switching signals, indicating that the stray inductances of the switching and gate loops are fairly low. Voltage probes are connected (using a PCB probe-tip adapter) directly across the drain-source and gate-source terminals while measuring the associated voltages. The highest achievable dv/dt during a turn-off is 60 and 20 V/ns for an SiC MOSFET and SiC diode, respectively. Likewise, the highest achievable di/dt is 3 A/ns during a turn-on of an SiC MOSFET and 1.5 A/ns during turn-off of an SiC diode. A parasitic oscillation of approximately 25 MHz was observed during these transients.



(a) A sample with a 85 V line input.



(b) A sample with a 230 V line input.

Fig. 5. Sample plots at different locations in the circuit (Fig. 1) at two different values of v_s, namely, 85 and 230 V, when switched at a f_{sw} of 250 kHz. At a low input voltage (85 V), the diode has a shorter duty cycle than the MOSFET compared to that at a high input voltage, and thus a diode with a low V_F is desired for achieving a low loss, particularly at 85 V. In a 1 kW PFC boost converter, the total MOSFET loss reaches approximately 40 W at 85 V and 9 W at 230 V when switched at 250 kHz. It should be noted that the time scale of the last sub-plot differs (0–0.2 s) compared to those of the other sub-plots, and thus the pattern of p_{avg} can be seen over the full simulation time.

C. PFC converter loss evaluation using circuit simulation

Using MATLAB Simulink, the total converter loss is simulated, the inputs for which are the switching losses obtained from the laboratory measurement and the conduction losses from the data sheet. These data are used as look-up tables or polynomial functions based on a curve fitting. To compute the losses associated with the rectifier bridge, the on-state loss of the Si diodes, the output capacitor ESR, and the boost inductor copper loss are used as input into the simulation model. As a cross-check, conduction losses are calculated using the simple analytical expressions provided in the Appendix in (3), and are found to be in accordance with the simulations. Regarding the switching loss, the look-up table method implemented in this study calculates the switching power loss by counting the number of switching events during the fundamental cycle of the input.

Fig. 5 (a), (b) illustrates the simulated waveforms of the PFC converter, such as the PWM input into the MOSFET, the current through the boost inductor (i_L), the switching current in the boost MOSFET (i_{ds}), the switching current in the boost diode (i_d), the instantaneous power loss of the MOSFET (p_{inst}), and the average power loss of the MOSFET (p_{avg}) with a filter of 0.01 s (1/60, with 60 Hz being the fundamental frequency). The sample plots are given for a switching frequency of 250 kHz. Apparently, when the MOSFET is in an on-state, i_L increases, and when the MOSFET is in an off-state (namely, when the diode conducts), i_L decreases. At a low input voltage (85 V), the diode has a shorter duty cycle than the MOSFET, whereas the opposite holds true at a high input voltage, which is why the diode with a low V_F is desired for achieving a low loss, particularly at a low line voltage. The last signal in the sub-plot is the average power loss over the SiC MOSFET, which includes the conduction and switching loss. Note that this particular sub-plot has a different time range (0–0.2 s) than the other sub-plots, which has deliberately been chosen to observe the average power loss characteristics of the SiC MOSFET over a longer time frame.

The detailed conduction loss breakdown for different line inputs, namely, 85, 115, and 230 V, is shown in Fig. 6, and the

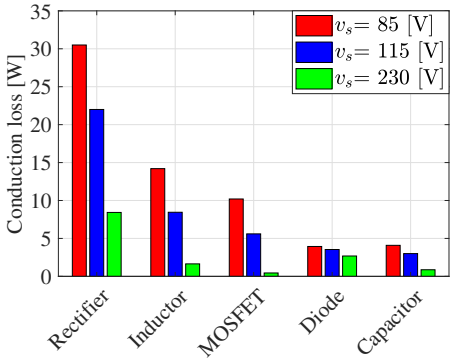


Fig. 6. Illustration of conduction loss breakdown at different input voltages, namely, 85, 115, and 230 V, at a 100% output power. The bridge rectifier has the largest part of the conduction losses compared to the other components in the circuit. Simultaneously, the conduction losses are more pronounced at lower line voltages compared to those at higher line voltages.

switching losses of the boost diode and MOSFET at these line inputs are shown in Fig. 7. For the same output power (1 kW), higher losses are incurred at a low line voltage compared to a high voltage, the primary reason for which is the higher current at the low line compared to that at the high line.

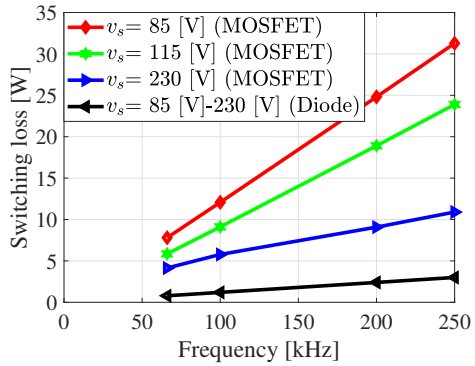


Fig. 7. Illustration of switching loss breakdown at different input voltages, namely, 85, 115, and 230 V, at a 100% output power. The switching losses imposed by the SiC MOSFET are larger compared to those imposed by the SiC diode. Of special note is that the switching losses of the SiC diode are independent of the load current, hence giving the same results at different line voltages, but the losses increase with the increase in voltage in the SiC MOSFET under similar circumstances.

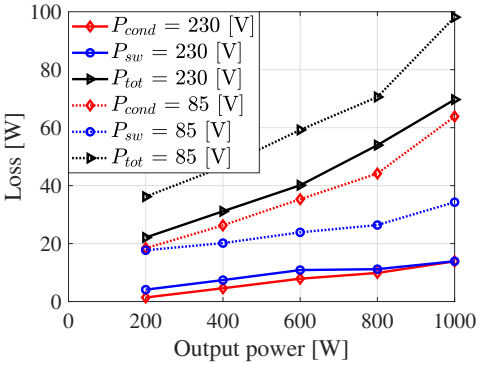


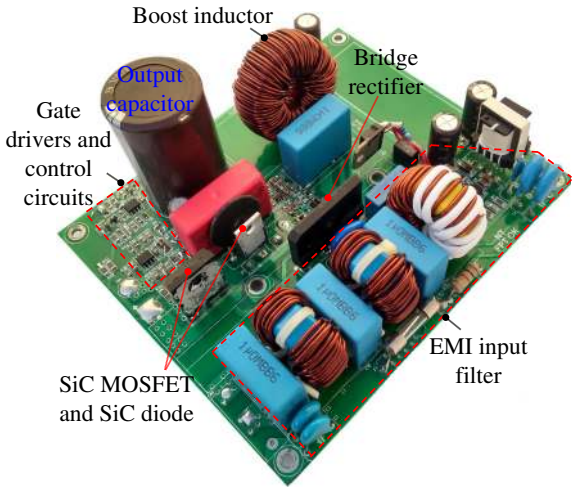
Fig. 8. Plots illustrating the conduction loss (P_{cond}), switching loss (P_{sw}), and total loss (P_{tot}) at 250 kHz. Clearly, P_{cond} is lower throughout the entire load for a v_s of 230 V, whereas the opposite is true for a v_s of 85 V.

The capacitive charge is low for the SiC diode and almost independent of di/dt, the forward current, and the temperature. Hence, the switching loss of the SiC Schottky diode is taken as a constant for a given output voltage of 400 V. Fig. 8 illustrates the total conduction, total switching, and their summation, P_{cond}, P_{sw}, and P_{tot}, respectively, over the entire load range at 250 kHz for two different line voltages. As shown, P_{cond} is lower over the entire load range for a v_s of 230 V, whereas the opposite is true for a v_s of 85 V.

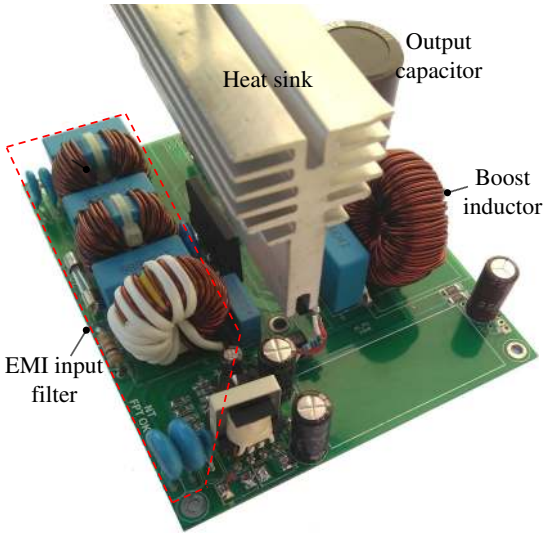
IV. Circuit Design and Layout Considerations in a Prototype PFC Converter

This section describes the circuit design and layout considerations in a PFC rectifier prototype for achieving the clean switching of an SiC MOSFET and SiC diode. In addition, brief descriptions of the input EMI filter, boost inductor, gate driver, and PFC controller are included. A full schematic diagram of the prototype is shown in Fig. 16 in the Appendix, and a complete component layout along with PCB routing is shown in Fig. 17.

With the objective of reducing the oscillations in the switching transients, the electric and magnetic field generations are minimized for controlling the generation of the EMI at the source. High-voltage switching traces are kept as small as possible to minimize the electric fields. The heat sink is connected to the return such that it does not act as a voltage-driven antenna. The gate drive track inductance is minimized. The switching current conductors are balanced and run opposite to each other to minimize stray inductance. Guard rings are used for the current sense signals. A ground plane was used for the control circuits. In addition, decoupling capacitors are used as closely as possible to the switching nodes. An image of the implemented hardware prototype with two different side views delineating the placement of different components is provided in Fig. 9.



(a) Illustration of component placement in PFC rectifier.



(b) Illustration of components along with heat sink.

Fig. 9. Photographs of the prototype PFC converter with two different side views showing the placement of different components.

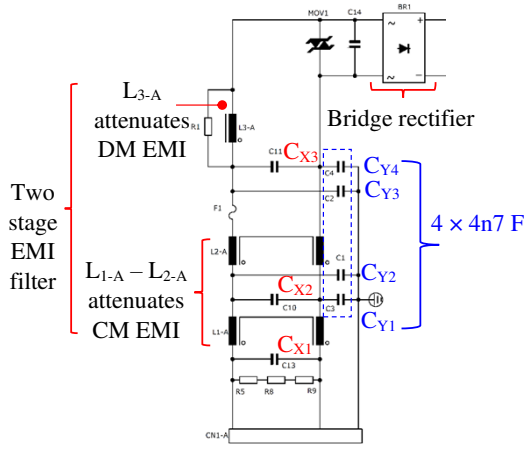


Fig. 10. Schematic diagram showing the two-stage EMI filter, the first stage consisting of inductors, L_{1-A} and L_{2-A}, attenuating the CM EMI, and the second stage with L_{3-A} attenuating DM EMI. Capacitances C_{Y1}–C_{Y4} (nF range) primarily serve as a CM filter; and C_{X1}–C_{X3} (μF range), as a DM filter.

A two-stage EMI filter, as shown in Fig. 10, was designed and implemented. The first stage consisting of the inductance, L_{1-A}, L_{2-A}, and the capacitances, C_{Y1}–C_{Y4}, attenuates a common-mode (CM) EMI. The second stage incorporating the inductance, L_{3-A}, and capacitances, C_{X1}–C_{X3}, attenuates a differential-mode (DM) EMI. Table III shows the designed EMI filter components for the prototype. The procedure followed in the design of the CM and DM filter is enumerated below.

1) Because the switching transients are the sources of the EMI, the measured DPT waveforms (time domain) are taken as an input to plot the corresponding frequency domain equivalent to a Fourier transform in MATLAB. This measured original noise is compared with the CISPR limits. Selecting the filter topology, as shown in Fig. 10, the corner frequency is calculated such that the attenuation satisfies the limit with an extra 6 dB safety margin.
2) First, the CM capacitances, C_{Y1}–C_{Y4}, are limited based on regulations indicating that the current-to-ground must not exceed 3 mA at 50/60 Hz. Accordingly, CM inductances are calculated using the resonance principle at the computed corner frequency. Then, the CM filter is tested in the MATLAB Simulink model of the PFC converter to check the defined 3 mA leakage current limit.
3) Because the leakage inductance of the CM choke, as well as the boost inductance of the PFC stage, help minimize the DM noise, a fairly low DM inductance is selected, namely, 1–4% of the CM inductance. Again, using the resonance equation, the CM capacitance is computed.
4) The designed filter was simulated in LTSpice employing realistic spice models of the circuit components, including SiC MOSFET, SiC diode, and EMI filters to check the EMC compliance before building the EMI filter in a laboratory.

A PFC controller UCC28180D from Texas Instruments is used with the switching frequency set to 250 kHz. Given the high switching speed capabilities of SiC devices, a higher switching frequency was possible without compromising the efficiency and achieving a dramatic size and cost reduction of the PFC boost inductor. A photograph showing the size difference in an inductor when switched at 66 kHz versus 250 kHz is provided in Fig. 11. The SiC MOSFET was driven by a +2.5/-5 A driver that can generate an approximately +18/-5 V drive voltage.

TABLE III
EMI FILTER SPECIFICATIONS.

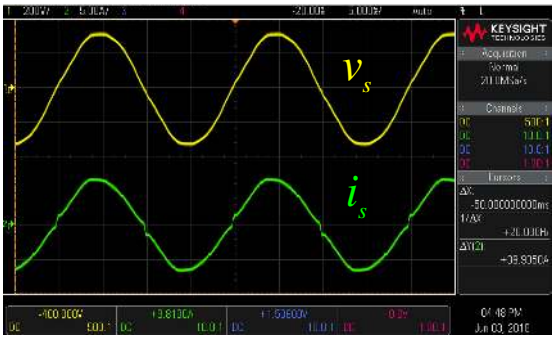
C_{Y1}–C_{Y4}, CM capacitances, Ceramic, Class X1/Y2 4 × 4n7F, P10 mm
L_{1-A}, L_{2-A}, CM chokes, EPCOS-TDK, R25 Ring core T38 material, 19 turns per coil, wire diameter 1.219 mm 2 × 3.6 mH ± 25% @ 1 kHz
L_{3-A}, DM chokes, Micrometal, T106-26 core, 36 turns wire diameter 1.422 mm, 1 × 120 μH ± 10% @ 1 kHz
C_{X1}–C_{X3}, DM capacitances, MKR, EPCOS, × 2 Class 3 × 1μF, 305 V, P22.5 mm

(a) f_{sw} = 66 kHz. (b) f_{sw} = 250 kHz.

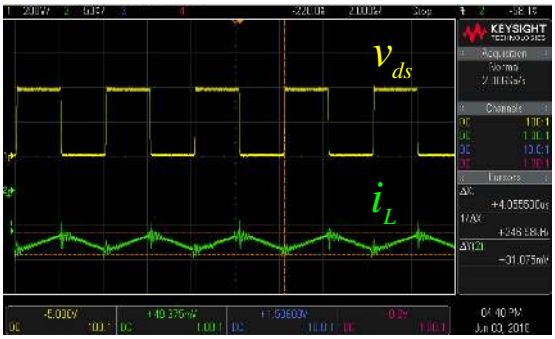
Fig. 11. Switching at 66 kHz requires 2× stacked sendust core, CS358060, with 70 turns giving 565 μH, whereas at 250 kHz, only a 1× stacked sendust core, CS330060, is sufficient, leading to a dramatic reduction in the size of the inductor.

V. Measurement Results

In this section, the efficiency and EMI evaluation of the prototype PFC converter are presented. The higher the ripple current in the boost inductance, the higher the AC losses in it. As a consequence, higher is the EMI because of the potential higher radiations of magnetic field. In this work, the SiC devices are switched with 0 Ω gate resistance together with the low parasitic design approach (the highest possible dv/dt and di/dt) with the aim of maximizing the efficiency and measuring the worst case EMI. However, slowing the SiC MOSFETs would potentially minimize EMI noises with the penalty of higher switching losses. Fig. 12 (a) shows the measured ac mains voltage and current. Clearly, i_s shapes v_s as expected. Fig. 12 (b) shows the MOSFET drain-source voltage and inductor current when switched at approximately 250 kHz. The discontinuity at zero-crossing of i_s is clearly seen because the dead-time comprises a major part with f_{sw} of 250 kHz compared with f_{sw} of 66 kHz. Fig. 13 (a) and (b) show the drain- and gate-source voltages during the turn-off and turn-on transients, respectively, illustrating the clean switching of an SiC MOSFET.

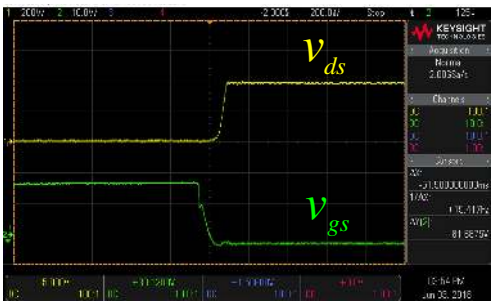


(a) Measured ac mains voltage, v_s, and current, i_s.

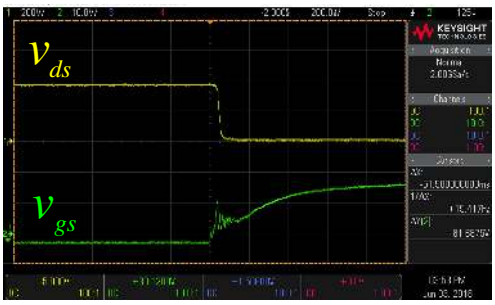


(b) MOSFET drain-source voltage, v_{ds}, and inductor current, i_L.

Fig. 12. Oscilloscope graphs at a switching frequency of roughly 250 kHz. (a) Illustration of i_s shaping v_s. (b) With f_{sw} of 250 kHz, boost inductor current, Δi_L, is 0.7 A, while it was 1.5 A with f_{sw} of 66 kHz. Influence of dead-time is seen as the discontinuity at zero-crossing of i_s.



(a) Measured v_{ds} and v_{gs} during turn-off.



(b) Measured v_{ds} and v_{gs} during turn-on.

Fig. 13. Measured drain-source voltage, v_{ds}, and gate-source voltage, v_{gs}, illustrating the clean switching of an SiC MOSFET. The gate oscillations are within the region where the device is beginning to partly turn on and transiting through the Miller plateau. This initial ringing is due to the input gate capacitance and the circuit parasitic inductance. Thereafter, the change in drain current is minor, resulting in insignificant ringing in v_{ds} during a turn on.

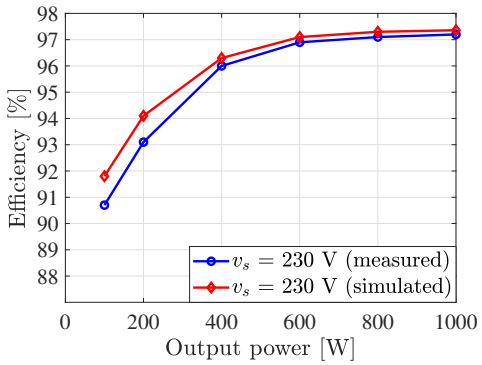


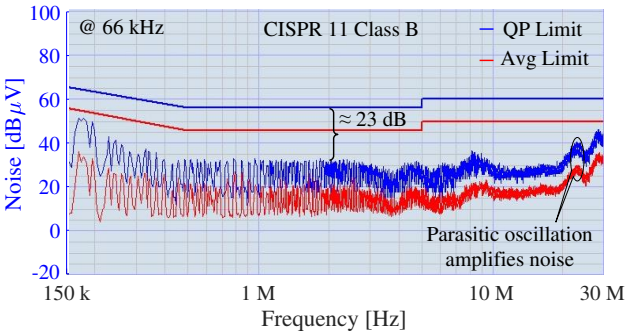
Fig. 14. Illustration of the simulated and measured efficiency of the PFC rectifier as a function of the output power, indicating that the converter achieves an efficiency of above 97% for a rated load of $>$ 60% with a peak efficiency of 97.2%. The measurements were taken using a prototype converter with a Yokogawa WT3000 power analyzer.

A. *Efficiency evaluation*

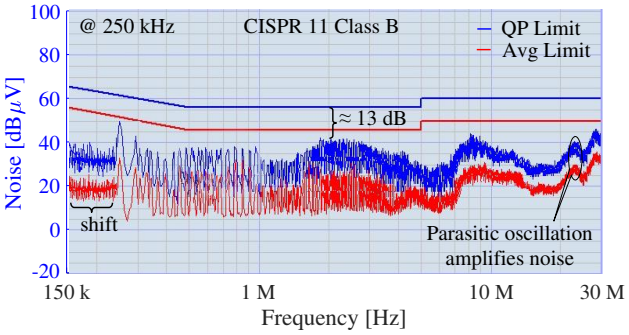
The simulated efficiency of the rectifier as a function of the output power for v_s = 230 V is shown in Fig. 14, together with the measurement results taken using a Yokogawa WT3000 power analyzer. As can be seen, the simulated results of the converter follow a similar pattern as the measured efficiency over a wide range of output power, and the discrepancy between the two is primarily due to two reasons. First, the simulated case does not consider the core losses in the boost inductor or the input EMI filter losses, whereas the measured case includes the overall losses in the PFC rectifier. Second, to measure such a high efficiency, an error introduced when using a power analyzer is also critical. Nonetheless, the converter achieves an efficiency of above 97% for $>$ 60% of the rated load with a peak efficiency of 97.2%, and is well above the 80 PLUS efficiency required over the entire load range.

B. *EMI evaluation*

A standard line impedance stabilizing network (LISN) and an EMC analyzer (Agilent E7401A) were used for measuring the EMI. Fig. 15 shows the measured conducted EMI emission (within the frequency range of 150 kHz–30 MHz) of the prototype PFC rectifier at an input voltage of 230 V and an output power of 1 kW at two different switching frequencies, 66 and 250 kHz. Compared to 66 kHz switching, at 250 kHz, the EMI noise shifts toward the right slightly, and then increases by approximately 10 dB (23-13 = 10 dB) over the entire spectra applied, given the same EMI filter size. Alternatively, it can be stated that, as the switching frequency increases, the filter size increases if the same noise level needs to be maintained. In Section III-B, it was stated that the DPT-measured parasitic oscillations (labelled in Fig. 4) are within the range of 25 MHz. Interestingly, the EMI noises in the corresponding frequency range are augmented, which is clearly shown in Fig. 15. This was also corroborated through a simulation conducted in LTSpice by varying the switching loop inductance and observing the noise within the frequency domain plot.



(a) Conducted EMI at a switching frequency of 66 kHz.



(b) Conducted EMI at a switching frequency of 250 kHz.

Fig. 15. Conducted maximum peak and average EMI noise emissions of the prototype PFC rectifier at an input voltage of 230 V and an output power of 1 kW at two different switching frequencies, namely, 66 and 250 kHz. All measurements are below the quasi peak (QP) and average (Avg) limits, and thus meet the CISPR 11 regulation for Class B equipment. Compared to 66 kHz, a 250 kHz switching incurs a higher noise provided an identical EMI filter.

VI. Conclusion

The main conclusions from this work are described below.

- Employing low-loss SiC power devices in the boost stage, the efficiency was evaluated in a classic boost PFC topology, the results of which revealed that the major converter loss is comprised of a diode rectifier part, which is particularly pronounced at a low-line as compared to a high-line voltage.
- A comparison between the efficiencies evaluated using a simple look-up table input from a double-pulse test follows the pattern measured using a power analyzer meeting the 80 PLUS efficiency regulation over the entire load range with an excellent margin.
- The conducted EMI in the prototype converter was found to comply with the CISPR 11 standard. It was also concluded that, owing to the increase in switching frequency from 66 to 250 kHz, the emissions are increased by roughly 10 dB throughout the entire frequency range (150 kHz to 30 MHz). Moreover, it was revealed that EMI noise is augmented at the corresponding ringing frequency given by the parasitic in the commutation loop.
- Increasing the switching frequency drastically minimizes the boost inductor size; however, the increase in the input EMI filter size might offset the high-power density target, and thus an optimal switching frequency should be chosen.
- Clean switching of the state-of-the-art SiC devices was illustrated to substantiate the design of a low-parasitic layout.

Thus, with a proper design and circuit layout, the clean switching of SiC devices can be achieved without sacrificing their high-speed switching potential, leading to negligible switching losses in these devices and an improved EMI signature. Furthermore, a reduction in the switching speed can also be utilized to optimize the circuit design, such as increasing the efficiency and reducing the cooling requirements, and by increasing the switching frequency, the size of the magnetic components can be minimized.

VII. Appendix

Equations for passive component sizing

$$L_B = \frac{1}{\Delta i_L} \cdot \frac{v_{s,min}^2}{P_{out}} \cdot \left(1 - \frac{\sqrt{2} \cdot v_{s,min}}{v_{out}}\right) \cdot \frac{1}{f_{sw}} \tag{1}$$

$$C_{out} = \frac{2 \cdot P_{out} \cdot t_{hold}}{v_{s,min}^2 - v_{out,min}^2}, = \frac{P_{out}}{2 \cdot \pi \cdot f_{line} \cdot \Delta v_{out} \cdot v_{out}} \tag{2}$$

The higher value of C_d is considered to be the output capacitor size for the design.

Equations for conduction loss calculation

$$\begin{aligned} P_{cond}(rectifier) &= 2 \times (I_{L,rms}^2 \times R_d + I_{L,avg} \times V_{FO}) \\ P_{cond}(inductor) &= I_{L,rms}^2 \times DCR \\ P_{cond}(capacitor) &= I_{c,rms}^2 \times ESR \\ P_{cond}(MOSFET) &= I_{ds,rms}^2 \times R_{DS,on} \\ P_{cond}(diode) &= I_{d,rms}^2 \times R_d + I_{d,avg} \times V_{FO} \end{aligned} \tag{3}$$

where, $I_{L,rms}$, $I_{L,avg}$, $I_{d,rms}$, $I_{d,avg}$, $I_{ds,rms}$ and $I_{c,rms}$ are the currents through rectifier, boost diode, MOSFET and output capacitor. Diodes have average (avg) and RMS values.

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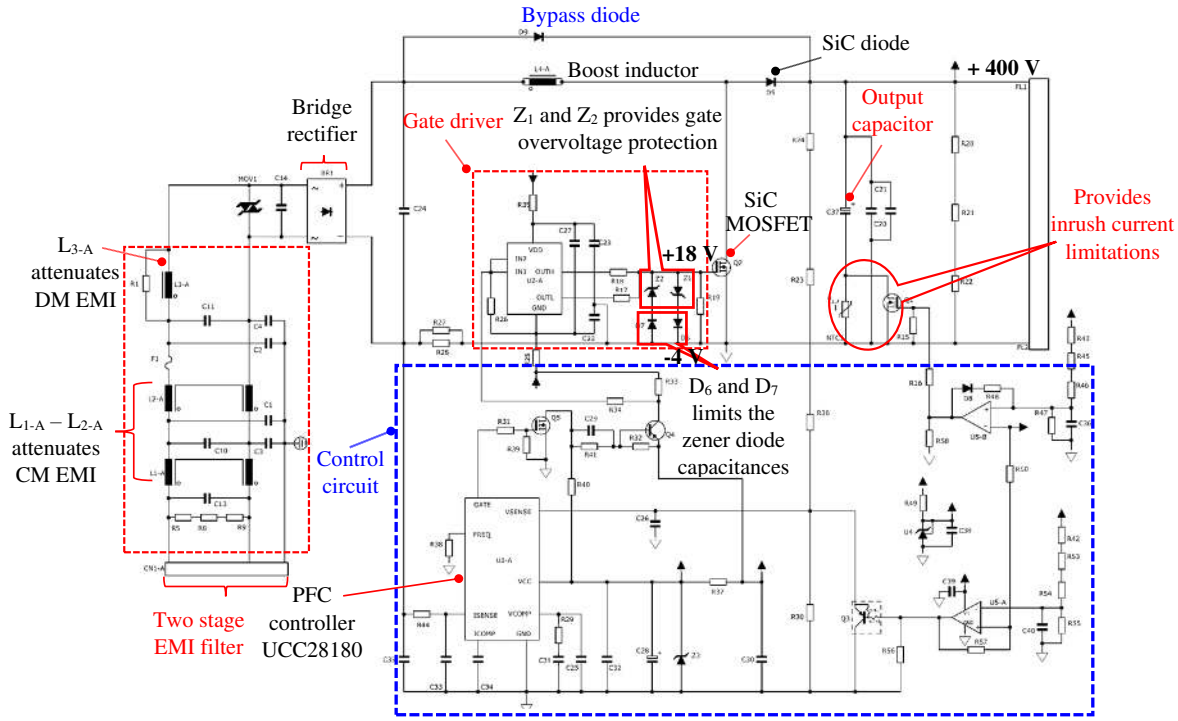

Fig. 16. A complete schematic diagram of the PFC rectifier prototype board.

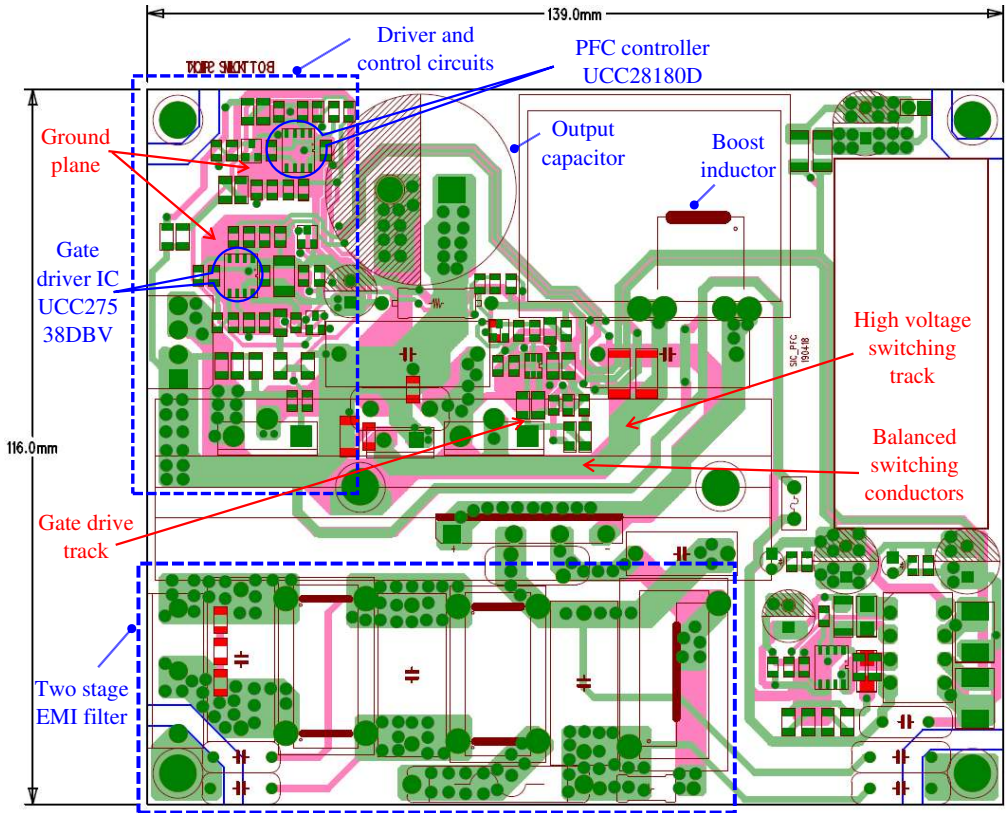

Fig. 17. A complete component layout and routing of the PFC rectifier prototype board (two-layer board).

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