Efficiency Improvement in Charge Pump Circuits

Chi-Chang Wang and Jiin-chuan Wu

***Abstract*— Conventional charge pump circuits use a fixed switching frequency that leads to power efficiency degradation for loading less than the rated loading. This paper proposes a level shifter design that also functions as a frequency converter to automatically vary the switching frequency of a dual charge pump circuit according to the loading. The switching frequency is designed to be 25 kHz with 12 mA loading on both inverting and noninverting outputs. The switching frequency is automatically reduced when loading is lighter to improve the power efficiency. The frequency tuning range of this circuit is designed to be from 100 Hz to 25 kHz. A start-up circuit is included to ensure proper pumping action and avoid latch-up during power-up. A slow turn-on, fast turn-off driving scheme is used in the clock buffer to reduce power dissipation. The new dual charge pump circuit was fabricated in a 3-μm p-well double-poly single-metal CMOS technology with breakdown voltage of 18 V, the die size is 4.7 $\times$ 4.5 mm^2. For comparison, a charge pump circuit with conventional level shifter and clock buffer was also fabricated. The measured results show that the new charge pump has two advantages: 1) the power dissipation of the charge pump is improved by a factor of 32 at no load and by 2% at rated loading of 500 Ω and 2) the breakdown voltage requirement is reduced from 19.2 to 17 V.**

***Index Terms*—Charge pump, CMOS analog integrated circuit, latch-up.**

I. Introduction

THE charge pump [1]–[5] and switching regulator [6] are two popular dc–dc converting circuits which are used to obtain a dc voltage higher than the supply voltage or a dc voltage with reverse polarity. Both circuits use a high frequency switching action to achieve voltage conversion. The major difference between these two types of circuits is the elements used to store energy during switching action. Charge pump circuits use capacitors as energy storage devices. Switching regulators use inductors or transformers as energy storage devices. When the power required is small, the capacitors needed by the charge pump circuit could be small enough that the entire charge pump can be integrated on an integrated circuit to reduce system cost. Therefore, on-chip charge pump converters are widely used in nonvolatile memory circuits [1], dynamic random access memory circuits [2], low voltage circuits [3], continuous time filters [4], and RS-232C transceivers [5].

Unlike the switching regulators, the output voltage of the charge pump circuits are usually not regulated. The conventional charge pump circuits are designed to operate at a fixed switching frequency with a rated output load current and voltage. For a CMOS charge pump circuit with a given switching frequency, load current, and output voltage, to obtain the best power efficiency, there exists an optimal value for the widths of the MOS transistor switches used in the charge pump. In this paper, the optimal width of the transistor switches in the charge pump is shown to be proportional to the load current. When the loading is less than the rated loading, either a smaller transistor width or a lower switching frequency should be used. Otherwise, the output voltage increases, and the power efficiency becomes worse. Because with transistor width and switching frequency fixed, the dynamic power to charge and discharge the gate of these switches is fixed. However, when load current is less than the rated loading, the power loss in these switches and the power delivered to the load decrease proportionally. Thus, the overall power efficiency decreases. Unfortunately, for most applications, the output load current is usually varying, depending on the mode of operation. Since it is difficult to dynamically change the widths of the on-chip transistor switches, a large enough transistor width and high enough switching frequency are chosen to guarantee the output voltage levels at the maximum loading. As a result, the power efficiency degrades as load current decreases, especially at no load. For applications that operate most of the time at no load, this is a great waste of power. Two methods can be used to reduce the power loss, one is to regulate the output; the other is to vary the switching frequency according to the loading.

Since the output of the charge pump is used to operate the transistor switches in the charge pump, the charging and discharging of the gate capacitance of these switches consume a certain amount of dynamic power. Regulating the output to a fixed level keeps the dynamic power from increasing at light loading. However, precise voltage regulation usually requires an operational amplifier and bandgap reference. The dc currents in these circuits offset most of the power saving. Rough voltage regulation, e.g., in DRAM applications [7], does not requires an operational amplifier and bandgap reference, but still requires dc current. Varying the switching frequency according to the loading is a more attractive method. When the switching frequency is changed from high switching frequency at maximum loading to low switching frequency at no load, the dynamic power will be greatly reduced and the output level is also regulated somewhat. One obvious scheme to adjust frequency is to use the output voltages to control the frequency of a V_{CO}. However, to oscillate as low as tens of Hertz, the chip area needed to implement the effective RC constant would be too large to be practical in an IC. We

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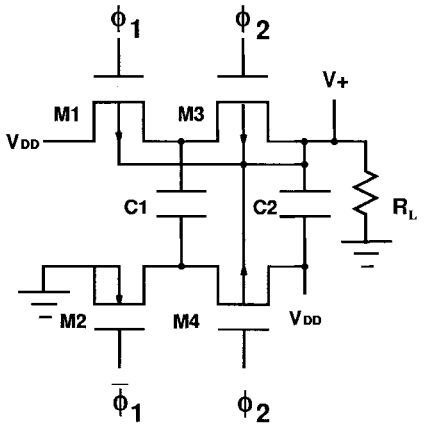


Fig. 1. A CMOS voltage doubling charge pump circuit.

proposed a new scheme to vary the switching frequency by modifying the design of the level shifter circuit. Section II describes the design of the charge pump circuit. Section III discusses the basic operation of a new CMOS dual charge pump utilizing a novel level shifter/frequency converter, two-phase nonoverlapping clock generator and buffer, and start-up circuit. Measurement results from test chips are described in Section IV.

II. Charge Pump Circuit Design

The schematic diagram of a CMOS charge pump circuit [5], which roughly doubles the supply voltage, is shown in Fig. 1. If a p-well process is used, then the substrates of all the PMOS are connected together. Since the substrate of PMOS must be connected to the highest voltage in the circuit, it must be connected to V_+ instead of V_{DD}. The power loss of this charge pump consists of two parts: one is the resistive power loss; the second is the dynamic power dissipated. The former depends on the on-resistance of the transistor switches and the load currents. The latter depends on the switching frequency, gate size, and the output voltage.

A. Conduction Power Loss

In Fig. 1, the transistor switches, used to connect and disconnect capacitors C_1 and C_2, are controlled by the two-phase nonoverlapping clock, ϕ_1 and ϕ_2. When ϕ_1 is low and ϕ_2 is high, the transistors M_1 and M_2 are turned on, and M_3 and M_4 are turned off. The voltage across capacitor C_1 is charged to V_{DD}. When ϕ_1 is high and ϕ_2 is low, the transistors M_1 and M_2 are turned off, and M_3 and M_4 are turned on. Capacitor C_1 is connected in parallel with capacitor C_2. The charge stored on C_1 is shared with capacitor C_2, thus pumping the voltage on V_+ node higher than the supply voltage V_{DD}. Note that when C_1 and C_2 are connected, the current not only flows through the channel of M_3, it can also flow through the P_+/N_{sub} source junction diode if the voltage on the source of M_3 is larger than $V_+ + 0.6$ V. The two-phase nonoverlapping clock must guarantee that the switches are operated in a break-before-make fashion to eliminate short-circuit current during switching. At steady state, these transistors are operated in the linear region, i.e., $|V_{GS} - V_T| > |V_{DS}|$ and the second-order V_{DS} term in the current-voltage equation of the MOSFET can be neglected. The on-resistance R of transistor switches is

$$R = \frac{L}{\mu C_{ox} W (V_{GS} - V_T)} \tag{1}$$

where μ is the surface mobility of the electron or hole, C_{ox} is the capacitance per unit area of the gate oxide, W is the channel width, L is the channel length, V_{GS} is the voltage of between gate and source, and V_T is the threshold voltage.

For two-phase nonoverlapping clock, the duty cycle should be less than 50%, for simplicity in analysis, the clock is assumed to have 50% duty. At steady state, within a clock cycle, the charges delivered to the load must equal the charges supplied by the power supply. Since load current is always on, the charges delivered to the load in one clock cycle are $Q_T = I_L * T$, where I_L is the load current and T is the clock period. However, these charges can only be supplied to C2 and the load in half of the clock cycle. Thus, when transistors M3 and M4 are turned on, the average current through them must be $2I_L$. Because these charges are supplied from capacitor C_1, when transistors M_1 and M_2 are turned on to charge C_1, the average current through them must also be $2I_L$, i.e., exactly Q_T amount of charges are delivered to C_1 during this half clock cycle. Assume the output ripple voltage of charge pump is small compared with the output voltage, i.e., $V_+ \gg \Delta V_+$, and the voltages across the capacitors C_1 and C_2 can be considered as constant. Assume the on-resistance R of all the transistors are the same, then the operation of charge pump circuit can be expressed as following.

i) When ϕ_1 is high and ϕ_2 is low, transistors M_1 and M_2 are off, M_3 and M_4 are on

$$V_+ = V_{DD} - 2I_L R + V_{C_1} - 2I_L R \tag{2}$$

and

$$I_L = \frac{V_+}{R_L} \tag{3}$$

where V_+ is the output voltage, V_{DD} is the power supply voltage, R_L is the load resistance, and V_{C_1} is the voltage across capacitor C_1. Note that in this half clock period, the circuit is an RC discharge circuit. When the clock period is sufficiently small compared with the RC time constant, then V_+ and V_{C_1} can be considered as constant during this half clock period.

ii) When ϕ_1 is low and ϕ_2 is high, transistors M_1 and M_2 are on, M_3 and M_4 are off,

$$V_+ = V_{DD} + V_{C_2} \tag{4}$$

and

$$V_{DD} = 2I_L R + V_{C_1} + 2I_L R \tag{5}$$

where V_{C_2} is the voltage across capacitor C_2.

Substituting (5) into (2), the output voltage can be written as

$$V_+ = 2V_{DD} - 8I_L R. \tag{6}$$

It is noted that the second term on the right-hand side of (6) is the total voltage drop across all the transistor switches in

the charge pump circuit. Thus, conduction loss in the charge pump circuit is given by

$$\begin{aligned} P_C &= 8I_L R \times I_L \\ &= 8I_L^2 R \\ &= \frac{8I_L^2 L}{\mu C_o W(V_{GS} - V_T)}. \end{aligned} \tag{7}$$

Based on (7), the conduction loss of the charge pump is inversely proportional to the transistor width W and proportional to the square of the load current I_L and the channel length L.

B. Dynamic Power Loss

The dynamic power loss during charge pump operation consists of two components, one is the charging and discharging of the gates of the MOS switches, the other is the charging and discharging of the MOS switches' source/drain junctions that are connected to capacitor C_1.

1) MOSFET Gate Power Loss: If the sizes of transistors in Fig. 1 are the same, then the total gate power loss of charge pump circuit is

$$P_g = 4C_g f V_g^2 \tag{8}$$

where $C_g = WLC_{ox}$ is the gate capacitance of a MOSFET, f is the frequency of clock ϕ, and $V_g = V_+$ is the maximum control voltage of the gate. Since the charge pump has to deliver a current, the output ripple voltage ΔV_+ is

$$\Delta V_+ = \frac{I_L}{2fC_L}. \tag{9}$$

The operating frequency must be higher than that given by (9) to guarantee the output ripple voltage is less than the specification which may vary depending on the applications. Thus, the gate power loss is given by

$$P_g = \frac{2WLC_{ox}I_L V_x^2}{C_L \Delta V_x}. \tag{10}$$

It is noted that the gate power loss is proportional to the transistor width W, load current I_L, and the channel length L.

2) MOSFET Drain/Source Power Loss: In the 3-μm CMOS process that we used, the drain/source capacitance of a MOSFET is proportional to the channel width. Let $C'_{D/S}$ be the drain/source capacitance per unit channel width. The total source/drain power loss is

$$\frac{PD}{S} = 4C_{D/S} f V_{DB/SB}^2 \tag{11}$$

where $C_{D/S} = WC'_{D/S}$ is the drain/source capacitance of a MOSFET and $V_{DB/SB} = V_+/2$ is the voltage swing of the drain or source. Note that only the four source/drain junctions connecting to capacitor C_1 have dynamic power dissipation, because the voltages on the other four source/drain junctions are constant. Similar to the gate power loss shown in (10), the source/drain power can be written as

$$P_{D/S} = \frac{WI_L V_+^2 C'_{D/S}}{2C_L \Delta V_+}. \tag{12}$$

Note that the drain/source power loss is proportional to the transistor width W and load current I_L, but independent of the channel length L.

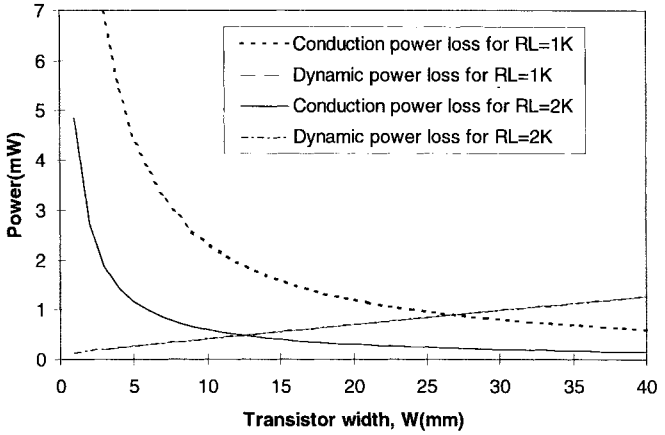
From the discussion above, the conduction loss of the charge pump is inversely proportional to the gate width. But the dynamic power loss is proportional to the gate width. Thus, the minimum total power loss of charge pump occurs when the conduction loss is equal to the dynamic power loss. Therefore, the optimal transistor switches width can be expressed as

$$W_{\text{opt}} = \left\{ \frac{4I_L C_L \Delta V_+}{\mu C_{ox}(V_{GS} - V_T)V_+^2} \left[1 + \frac{C'_{D/S}}{4LC_{ox}} \right]^{-1} \right\}^{1/2}. \tag{13}$$

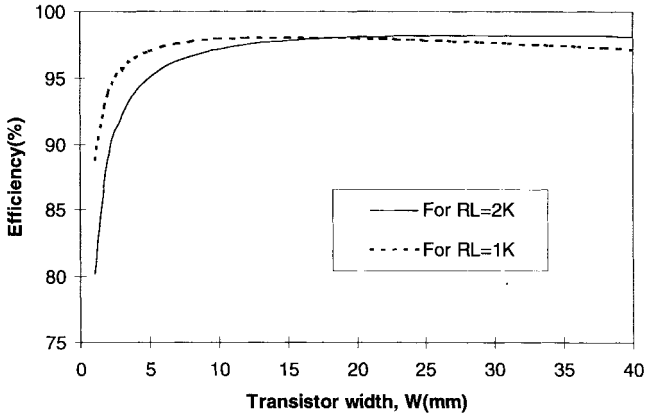
It can be seen from (13) that the optimal width is proportional to the square root of the load current I_L. However, the output load current usually varies during normal operation. In a typical design, in order to guarantee the output voltage levels at maximum loading, a high enough switching frequency is chosen first. Then, the optimal transistor switches width for the rated loading and the chosen switching frequency are used. With these parameters, the power efficiency is maximized for the rated load current. When the load current is less than the rated current, the power efficiency decreases, with the worst case occurring at no load. The conduction and dynamic power losses versus transistor width for $R_L = 1$ and 2 kΩ are shown in Fig. 2(a), with $V_{DD} = 5$ V, $f = 25$ kHz, and $C_L = 1$ μF. As expected, the conduction power decreases rapidly for transistor widths less than 10 mm. The dynamic power increases linearly with the transistor width. The conduction power decreases when R_L is increased, but the dynamic power does not depend on R_L. The optimal transistor widths for $R_L = 1$ and 2 kΩ are 12 and 27 mm, respectively. The power efficiency versus transistor width for $R_L = 1$ and 2 kΩ are shown in Fig. 2(b). For $R_L = 2$ kΩ, the maximum efficiency (98.0%) occurs at $W = 12$ mm. However, for W ranging from 6 to 44 mm, the efficiency is always above 97%. Similarly, for $R_L = 1$ kΩ, the maximum efficiency (98.2%) occurs at $W = 27$ mm. However, for W ranging from 9 to 50 mm, the efficiency is always above 97%. Thus, for the sake of die area, a transistor width much smaller than the optimal width can be used with very little loss in power efficiency.

III. A CMOS Dual Charge Pump

To improve power efficiency, a new charge pump control circuit is proposed. As an example to illustrate the effectiveness of this new scheme, Fig. 3 is the circuit diagram of a proposed CMOS dual charge pump for RS-232C applications which is a popularly used EIA (Electronic Industries Association) standard for serial communication. The circuit of the positive charge pump in Fig. 3 is the same as the conventional charge pump, but the clock generation circuit is different. In principle, the operation of the circuit in Fig. 3 is time-divided into two segments or phases. The operation of the positive voltage doubling portion is the same as that in Fig. 1. The inverting portion of the charge pump circuit operates as follows. The transfer capacitor C_3 is charged to the positive



(a)



(b)

Fig. 2. (a) The conduction and dynamic power losses versus transistor width. (b) The power efficiency versus transistor width.

output voltage via the transistors M_5 and M_6 which are turned on during the first phase of operation of the circuit, while the transistors M_7 and M_8 are turned off. During the second phase of circuit operation the transistors M_5 and M_6 are turned off. The voltage across the transfer capacitor C_3 is shared with the reservoir capacitor C_4 by turning on the transistors M_7 and M_8. The positive end of C_3 is connected to ground through M_7, making the polarity of the output node V_- negative. The magnitude of V_- is less than that of V_+ due to the resistive voltage drops across the transistors. Since the operation of the inverting charge pump is similar to that of the positive charge pump, the analysis in Section II also applies, i.e., the optimal transistor width is still given by (13), except that V_+ should be replaced by V_-.

In order to reduce the size of transistors in Fig. 3, the transistors M_1, M_3, M_4, and M_5 are P-channel MOSFET, and the transistors M_2, M_6, M_7, and M_8 are N-channel MOSFET. The ring oscillator, shown in Fig. 3, generates a clock nominally at 25 Hz. The ring oscillator is driven by V_{DD} instead of V_+ and V_-, so that its oscillation frequency will not be affected by the output voltages V_+ and V_-. However, the voltage swing of the two-phase nonoverlapping clocks must be larger than zero to V_{DD}, e.g., to turn off transistor M_3, the high voltage level of the clock must be V_+; to turn off transistors M_6 and M_8, the low voltage level of the clock

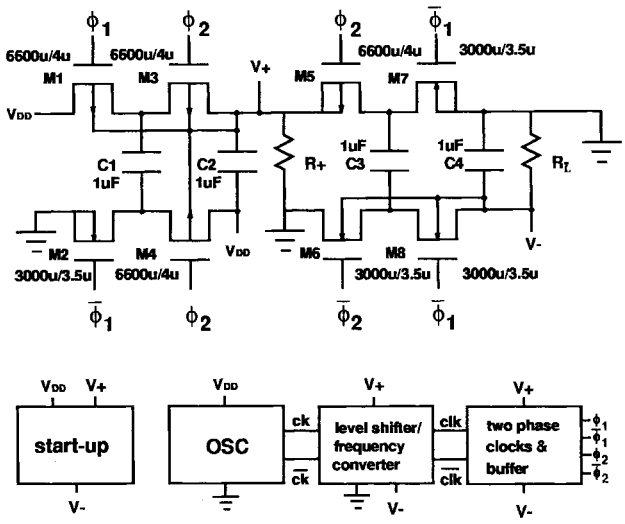


Fig. 3. A CMOS dual-charge pump circuit.

must be as low as V_-. Therefore, a level shifter is needed to increase the clock's voltage swing to V_- and V_+.

Fig. 4 is the circuit diagram of the level shifter/frequency converter. Transistors M_1 to M_4 form a conventional level shifter, i.e., the signals on nodes 1 and 2 have the same frequency as that of the input clock signal CK, but the voltage swing is increased from 0-to-V_{DD} to 0-to-V_+. Transistors M_5 to M_8 form another level shifter, i.e., the voltage swing of the output clock signal CLK is increased from 0-to-V_+ to V_--to-V_+. A closer look at the operating principle of this circuit reveals that the frequency at nodes 1 and 2 is not necessarily the same as that of CK. Due to the cross coupling of transistors M_1 and M_3, the level shifter is a bistable circuit. The switching of nodes 1 and 2 is a typical positive feedback process. Assume initially $CK = 0$ V, $\overline{CK} = 5$ V, node 1 $= V_+$, and node 2 $= 0$ V, then transistors M_1 and M_4 are on, and transistors M_2 and M_3 are off. This circuit is in one of its two stable states. When CK is changed to 5 V, $\overline{CK}$ will be changed to 0 V, thus transistor M_4 is turned off and transistor M_2 is turned on. Because transistors M_1 and M_2 are both turned on, the voltage on node 1 decreases from V_+ to a voltage decided by the voltage dividing action between transistors M_1 and M_2. If this voltage is lower than $V_+ - V_{TP}$, where V_{TP} is the threshold voltage of the PMOS, then transistor M_3 will be turned on. The voltage on node 2 will increase from 0 V toward V_+. As the voltage on node 2 increases, the on-resistance of the transistor M_1 decreases which causes the voltage on node 1 to decrease further. This is a typical positive feedback process. When the loop gain exceeds one, the voltages on nodes 1 and 2 will quickly change and enter another stable state. Note that in either stable state, there is no static current, because either M_1 and M_4 or M_2 and M_3 are completely turned off. The time it takes for the loop gain to exceed one (response time) depends on the transistor size ratio between the PMOS and NMOS, capacitance at nodes 1 and 2, and the voltage difference between $V_{DD}$and V_+. If the period of the input clock CK is much shorter than the response time, then the level shifter will not switch state. If the period of the input

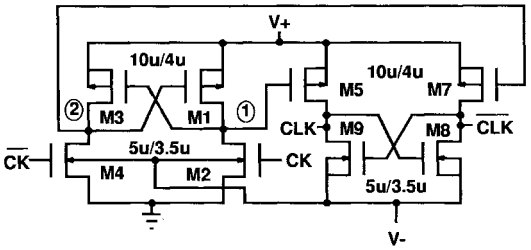


Fig. 4. Circuit diagram of the level shift/frequency converter.

clock, CK, is slightly shorter than the response time so that after one clock cycle the voltages on nodes 1 and 2 did not return to their initial values, then the level shifter will take more than one CK's cycle to switch state. Thus, the output CLK is still a periodic clock, except that the frequency is lower. In a normal level shifter, the sizes of M_2 and M_4 are made much larger than that of M_1 and M_3 to reduce the response time so that CK and CLK have the same frequency.

In Fig. 4, the transistor sizes of the NMOS (5 μm/3.5 μm) and PMOS (10 μm/4 μm) are purposely made to be about the same so that the response time is comparable to the period of CK. Fig. 5 shows the relationship between the response time and the output voltages V_+ and V_-. The three curves are for $|V_-| = V_+$, $|V_-| = V_+ - 0.5$, and $|V_-| = V_+ - 1$, respectively. The supply voltage V_{DD} is 5 V. It can be seen that the response time increases rapidly as V_+ and $|V_-|$ increase. With CK at 25 kHz, the CLK will not change states in one clock cycle if the values of V_+ and V_- correspond to a response time longer than 20 μs, the half period of 25 kHz. When CLK is not switching, V_+ and V_- will decay due to the current drawn by the loading. Eventually, V_+ and V_- will be low enough to cause the CLK to switch and pump V_+ and V_- higher than the switching threshold again, and the process repeats again. Because the output voltages V_+ and V_- decrease when load current increases, the level shifter effectively varies its output's frequency according to the load current. Fig. 6 shows the simulation result of the switching of the level shifter/frequency converter circuit with $R_+ = R_- = 1$ kΩ. It can be seen that during the period when CLK is high, V_+ is pumped to a higher voltage. When CLK is low, V_+ decays due to the load current. When V_+ decays to a low enough voltage to enable the switching of the level shifter, CLK will become high again at the next rising edge of CK. In Fig. 6, the frequency of CLK is half that of CK. When the load current is smaller, V_+ and V_- will decay slower, and CLK will switch at a lower frequency. When loading increases, the frequency of CLK will increase until it becomes the same as CK. Thus, this level shifter/frequency converter circuit changes the input clock's voltage swing and frequency simultaneously.

Fig. 7 is the two-phase nonoverlapping clock generator and buffer circuit. The two-phase nonoverlapping clock guarantees the transistor switches in the charge pump are operated in a break-before-make fashion to eliminate short-circuit current which wastes power and causes reliability problems on the metal lines. The left half of Fig. 7 is a conventional two-

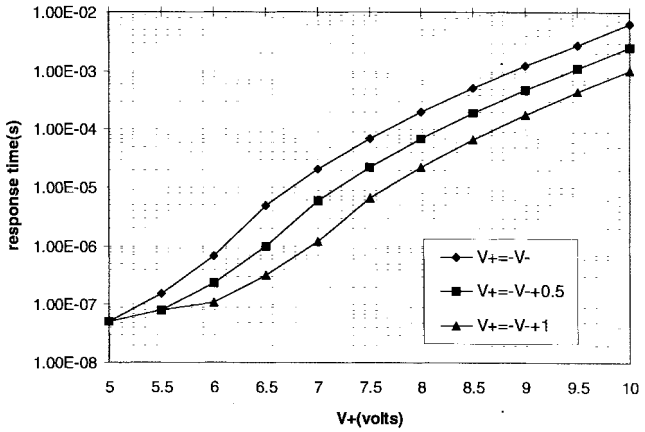


Fig. 5. The relationship between the response time of the level shifter in Fig. 4 and the voltages V_+ and V_-.

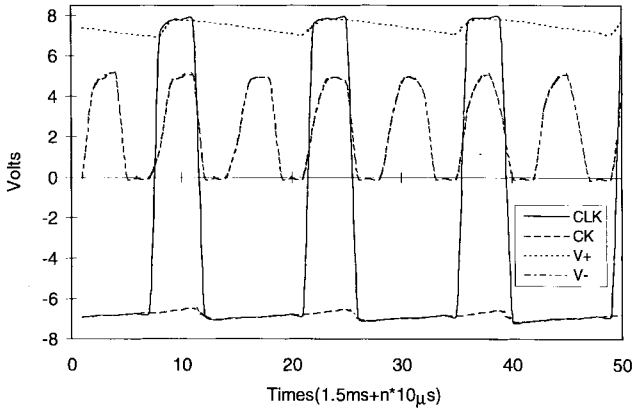


Fig. 6. Simulation result of the level shifter/frequency converter with $R_+ = R_- = 1$ kΩ.

phase nonoverlapping clock generator and buffer circuit which produces two-phase nonoverlapping clocks, ϕ_1, $\overline{\phi}_1$, ϕ_2, and $\overline{\phi}_2$. However, due to the large gate capacitance of the transistor switches (6600 μm/4 μm for PMOS and 3000 μm/3.5 μm for NMOS), large rise/fall time may cause the two-phase clocks to overlap. One solution is to increase the length of the inverter chain so that the nonoverlapping period is longer than the rise/fall time. The other is to use a large buffer to decrease the rise/fall time. Both methods require more power dissipation. We proposed a slow turn-on, fast turn-off method to obtain the two-phase nonoverlapping clocks. As shown in Fig. 7, each transistor switch is broken into several smaller transistors, and resistors are placed in series between the gates of these smaller transistors. Note that these resistors are the effective resistance of the gate poly so that no additional chip area is needed. There are eight transistor switches in Fig. 3, for clarity, only four transistor switches are shown here. Additional small PMOS' were used to increase the charging speed of the gate of PMOS switches. Similarly, additional small NMOS' were used to increase the discharging speed of the gate of NMOS switches. During discharging of the gate of the PMOS switch, the additional PMOS' are turned off, and the gate of PMOS switch is an RC delay line, thus the PMOS switch will be turned on slowly. During charging, the additional PMOS'

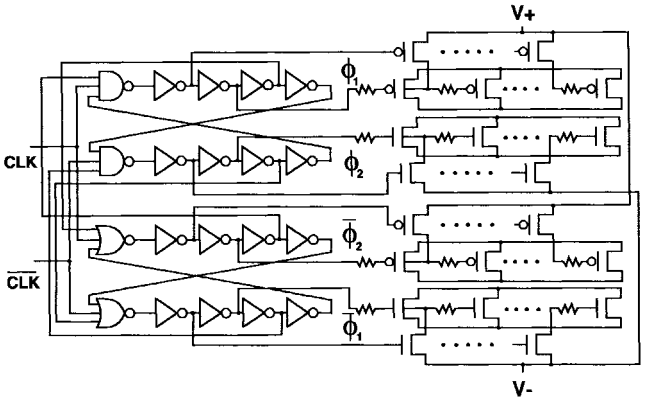


Fig. 7. Circuit diagram of the two-phase clocks and buffer circuit.

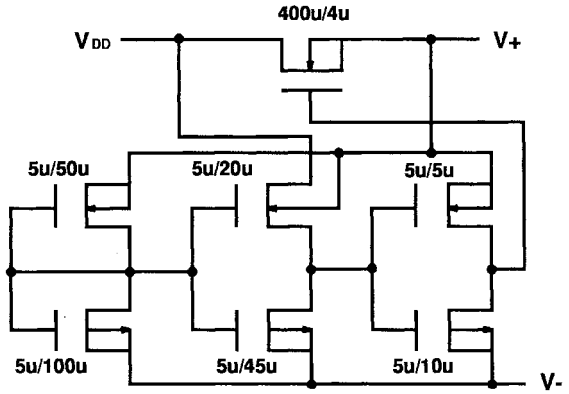


Fig. 8. Circuit diagram of the start-up circuit.

are turned on, effectively shorting the resistors, so that the gate of the PMOS switch is quickly charged to V_+ to turn off the PMOS switch quickly. A similar scheme is used for the NMOS switches. With this fast turn-off, slow turn-on scheme, a more power-efficient short inverter chain and small buffer can be used to obtain two-phase nonoverlapping clocks.

Fig. 8 is the start-up circuit which is needed to ensure proper pumping action and avoid latch-up during power-up. As discussed earlier, the two-phase nonoverlapping clock generator and buffer circuit must be powered by V_+ and V_-, otherwise the PMOS and NMOS switches will not be turned off during pumping, which will prevent V_+ from increasing beyond V_{DD}. However, during power-up, the V_+ and V_- are initially at 0 V, i.e., pumping action cannot be started. Thus, before V_+ is pumped to a voltage higher than V_{DD}, all the p-n junctions at the sources of the PMOS in the ring oscillator and the transistors M_1 and M_4 in Fig. 3 are forward biased. Currents will be injected into the substrate to charge the substrate to about $V_{DD}-0.5$ V. If these charging currents are allowed to flow laterally over a large distance, the probability of latch-up increases. The circuit in Fig. 8 consists of three inverters and a large PMOS switch. The first inverter is a self-biased inverter with its output tied to input. The first two inverters' transistors are sized so that when V_+ is smaller than $V_{DD}+0.2$ V, the output of the first inverter is a logical zero to the second inverter. Therefore, the output of the third inverter is also a logical zero, which keeps the large PMOS switch turned on once the supply voltage is applied. This provides a very low resistance path between V_{DD} and V_+. The substrate will be charged through this PMOS switch so that V_+ will be the same as V_{DD} when V_{DD} is ramping up to its steady-state value, i.e., the p-n junctions at the sources of the PMOS in the ring oscillator will not be forward biased. Since V_+ is routed using a metal line to the rest of the chip to make substrate contact, the substrate will be charged to V_{DD} by vertical substrate current, not lateral substrate current, to avoid latch-up. This circuit gives V_+ an initial voltage to start the pumping process. However, if the PMOS switch is still on when V_+ is larger than V_{DD}, then V_+ will be clamped by V_{DD}. Therefore, once V_+ is pumped to a voltage higher than $V_{DD}+0.2$ V, the output of the third inverter becomes a logical 1, turning off the PMOS switch so that V_+ can be pumped up to its final steady state voltage. Thus, this circuit connects V_+ to V_{DD} when V_+ is smaller than $V_{DD}+0.2$ V, and disconnects V_+ from V_{DD} otherwise. In this way, the charge pump circuit can start up properly and without latch-up.

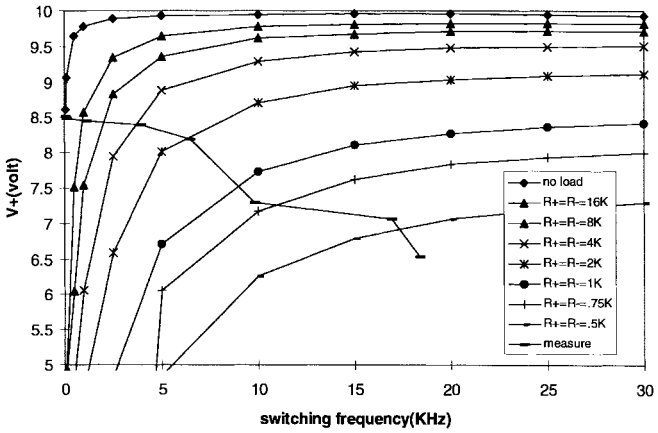


Fig. 9. Simulation and measured positive output voltage of the dual-charge pump at various switching frequencies and loading.

The operation of a dual charge pump circuit with conventional level shifter, i.e., it is a conventional charge pump, was simulated by HSPICE. The simulation results of the positive and negative output voltages versus the switching frequency and output loading are shown in Figs. 9 and 10, respectively. It can be seen that, for a given load resistance, the output voltage increases with switching frequency and saturates above a certain frequency. For a given switching frequency, the output voltage decreases with increasing load current. This circuit is designed to supply up to 12 mA at V_+ and V_- outputs while maintaining $V_+ > 6.5$ V and $V_- < -6$ V. In order to guarantee the output voltage levels at maximum loading, a 25 kHz clock signal is chosen based on Figs. 9 and 10. With a fixed switching frequency, a substantial supply current is needed even at no load. For applications that operate most of the time at no load, this is a great power loss. In this paper, the level shifter/frequency converter shown in Fig. 4 was used to reduce the power loss by varying the switching frequency according to the load current.

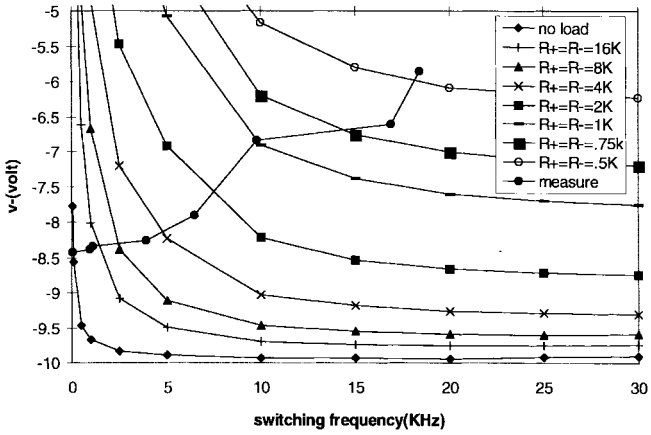


Fig. 10. Simulation and measured negative output voltages of the dual-charge pump at various switching frequencies and loading.

IV. Experimental Results

The circuit shown in Fig. 3, except the 1-mF capacitors and load resistors, was fabricated in a 3-μm p-well, double-poly single-metal CMOS technology with breakdown voltage of 18 V. Fig. 11 is a chip micrograph, the die size is 4.7 $\times$ 4.5 mm^2, the majority of the chip area is occupied by the eight MOS switches. For comparison, a charge pump circuit with conventional level shifter and clock buffer was also fabricated. With $V_{DD} = 5$ V, the measured output voltages and switching frequencies of the new charge pump are plotted in Figs. 9 and 10 along with the simulation results of the conventional charge pump. For load resistance above 1 kΩ, the measured results agree with the simulation, e.g., for 1 Ω load and 10 kHz switching frequency, V_+ is 7.3 V and V_- is -6.8 V for measured results, and V_+ is 7.1 V and V_- is -6.8 V for simulated results. For 750 and 500 kΩ loads, the measured outputs are smaller than the simulation. The measured results of the conventional and new charge pump circuits are also listed in Table I. For the conventional charge pump, the switching frequency is about 20 kHz for all loading, less than the designed 25 kHz. For the new charge pump, the switching frequency at no load is 70 Hz, less than the designed 100 Hz. It increases when loading becomes heavier. For load resistance of 500 Ω, the switching frequency increases to 18.4 kHz, also less than the designed 25 kHz. Thus, the proposed level shifter/frequency converter in the new charge pump does covert the switching frequency according to the loading.

The advantage of the new charge pump in terms of power dissipation can be viewed in two ways: supply current and power efficiency; both are shown in Table I. The power efficiency is calculated using the conventional definition of the output power divided by the input power. The power efficiencies of the conventional and new charge pumps are shown in Fig. 12. At 0.5 kΩ load, the new charge pump has better power efficiency than that of the conventional charge pump. For 0.75 kΩ and 1 kΩ loads, the conventional charge pump is better. For load resistance larger than 2 kΩ, the new charge pump is much better. Considering supply current, for all loading, the supply current of the new charge pump is always smaller than that of the conventional charge pump. The difference in the supply current increases with increasing load resistance. Thus, the power savings is the greatest at no load. At no load, the supply current is decreased from 6.17 to 0.19 mA, about 32 times smaller. Note that at no load, although the charge pump is switching at 70 Hz, the ring oscillator is still operating at 20 kHz, which accounts for the 0.19 mA supply current. The amount of power savings decreases at heavier loading. At the maximum loading of 500 Ω, the supply current is still 1.1 mA smaller,

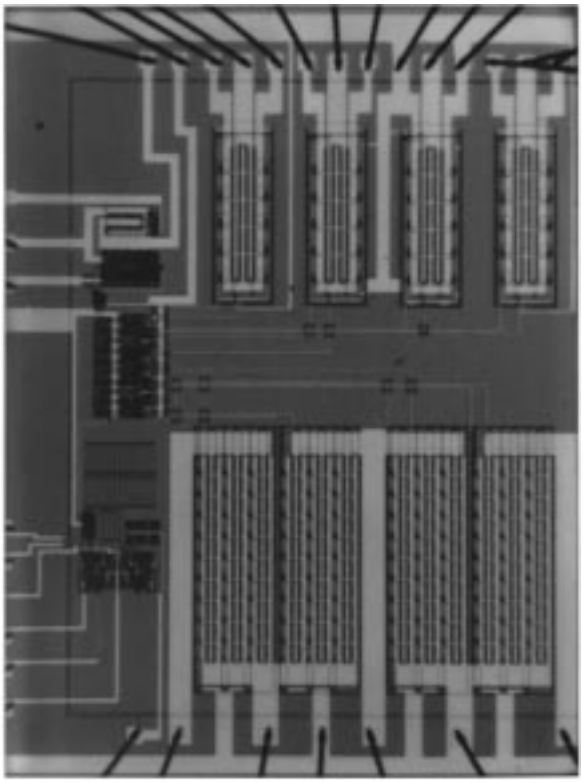


Fig. 11. A chip micrograph of a CMOS dual-charge pump.

TABLE I
Measured Results of the Conventional and New Dual-Charge Pump Circuits

	conventional charge pump				
load	V+	V-	f(kHz)	Idc(mA)	efficiency(%)
0.5k	6.29	-5.43	18.6	50.7	54.5
0.75k	7.28	-6.73	18.9	37.6	69.7
1k	7.72	-7.3	19	30.6	73.8
2k	8.55	-8.38	19.3	18.9	75.8
4k	9.11	-9.03	19.5	12.5	65.8
8k	9.41	-9.32	19.6	9.36	46.8
16k	9.56	-9.45	19.7	7.79	29
no load	9.61	-9.59	19.7	6.17	0
	new charge pump				
load	V+	V-	f(kHz)	Idc(mA)	efficiency(%)
0.5k	6.54	-5.85	18.4	49.6	62.1
0.75k	7.07	-6.6	16.9	36.2	68.9
1k	7.29	-6.84	9.79	28.4	70.4
2k	8.19	-7.9	6.46	16.2	79.9
4k	8.39	-8.26	3.92	8.41	82.4
8k	8.45	-8.34	1.12	4.34	81.2
16k	8.49	-8.39	0.95	2.3	77.4
no load	8.52	-8.43	0.07	0.19	0

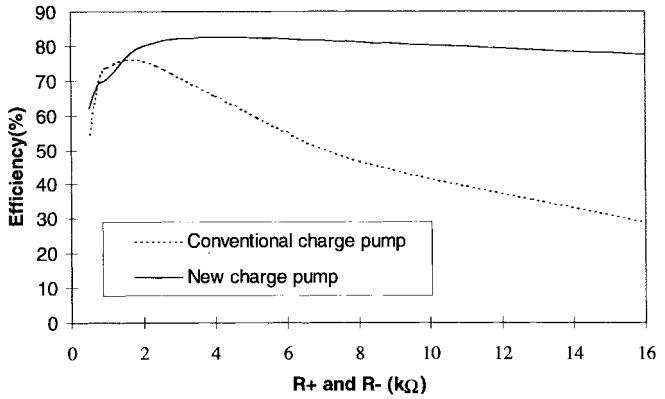


Fig. 12. The power efficiencies of the conventional and new charge pumps.

which is more than 2% power savings. The power savings at light loading mainly comes from the lower dynamic power dissipation due to the lower switching frequency. However, at heavy loading of 500 Ω, the switching frequencies of the two charge pumps are about the same, and power savings comes from the level shifter and clock driver.

The other advantage of the new charge pump is that the breakdown voltage requirement is smaller. Note that at 500 Ω load resistance, the voltage outputs of the new charge pump are larger than those of the conventional charge pump. Thus, the new charge pump is capable of delivering more current and voltages at heavy loading. However, for load resistance larger than 750 Ω, the voltage outputs of the new charge pump are smaller than those of the conventional charge pump. In most of the charge pump applications, this is actually an advantage, not a drawback, because when the load circuit draws less current, the output voltages of the charge pump need not be increased. For example, in the RS-232C applications, no matter how much current the load circuit draws, the load circuit will work as long as V_+ is larger than 6.5 V and V_- is less than −6.0 V. Having larger charge pump output voltages only increases the breakdown voltage requirement of the MOS transistor, e.g., for the conventional charge pump, the MOS transistor must be able to sustain a voltage of 19.2 V; for the new charge pump, the breakdown voltage requirement is only 17 V. Therefore, the lower output voltages of the new charge pump at lighter loading is actually an advantage. In terms of the breakdown voltage requirement, the best solution is to regulate the output voltages. However, this requires more circuit and power, as discussed in the introduction.

It should be noted that at no-load, the most power efficient scheme is to shut down the entire circuit. However, this leads to a latency during wake-up because it takes time for the output voltages V_+ and V_- to reach their respective steady state values from 0 V. The wake-up time depends on the value of the transfer and holding capacitors used. When a square wave power supply (amplitude is 5 V and frequency is 300 Hz) is applied to the charge pump circuit with $C = 1\ \mu$F, $R_+ = 2$ kΩ and $R_- = 2$ kΩ, the measured waveforms of the positive output voltage V_+ (upper trace) and power supply (lower trace) are shown in Fig. 13. The effect of the start-up circuit can be seen from the measured result that when supply voltage

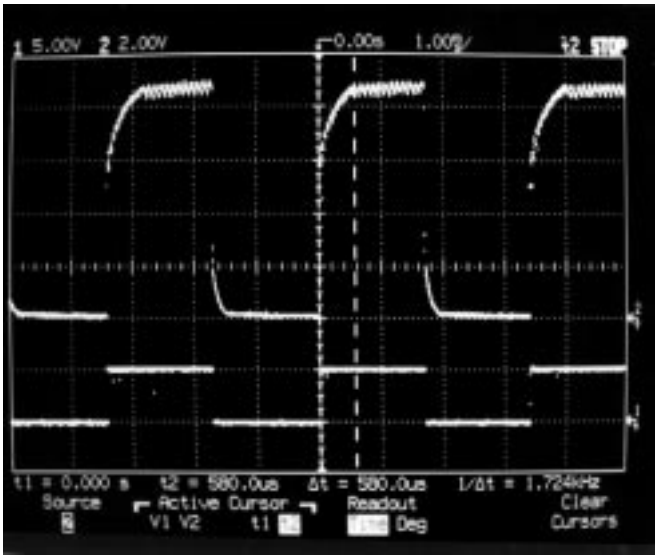


Fig. 13. Measured positive output waveform under a square wave power supply.

changes from 0 to 5 V, the output V_+ jumps immediately from 0 to 5 V instead of 4.4 V, indicating that the output V_+ is charged by V_{DD} through the PMOS switch in Fig. 8, not through the p-n junction. After the initial jump, the output then gradually increases to its steady state value of 8.2 V. The rise time and ripple of V_+ are 580 μs and 0.4 V, respectively. The negative output voltage V_-, which is not shown in Fig. 13, decreases from 0 V to −7.9 V. The fall time and ripple of V_- are 600 μs and 0.4 V, respectively. The rise/fall time and ripple of V_+ and V_- increase with the load current. In applications that can tolerate such a latency during wake-up, the shut-down scheme should be used. For applications that require the charge pump to stay active, lowering the switching frequency seems to be the best solution.

V. Conclusions

A formula to determine the optimal transistor switch width of the charge pump was developed. A level shifter design that also functions as a frequency converter to automatically vary the switching frequency of a dual charge pump circuit according to the loading was proposed. The frequency tuning range of this circuit was designed to be from 100 Hz to 25 kHz. This circuit is intended to improve the power efficiency of the conventional charge pump circuits that use a fixed switching frequency, which leads to power efficiency degradation when loading is less than the rated loading. The switching frequency was designed to be 25 kHz with 12 mA loading on both inverting and noninverting outputs. The switching frequency is automatically reduced when loading is lighter to improve the power efficiency. A slow turn-on, fast turn-off driving scheme was used in the clock buffer to reduce power dissipation. A start-up circuit was included to ensure proper pumping action and avoid latch-up during power-up. The new dual-charge pump circuit was fabricated in a 3-μm double-poly single-metal CMOS technology, the die size being 4.7 × 4.5 mm^2. The measured results show that this circuit improves the efficiency of the charge pump, especially at light loading.

At no load, a factor of 32 in reduction of supply current is obtained. At rated loading of 500 Ω, the power savings is 2%. The breakdown voltage requirement of the transistor is reduced from 19.2 to 17 V.

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