

EFFICIENCY INVESTIGATION OF BUCK DC-DC CONVERTER FOR RF APPLICATIONS

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This paper was focused over the efficiency evaluation and optimization of switch-mode dc-dc converter for RF applications. AMS CMOS 0.35 μm technology was used for investigations. Effect of different factors over the circuit's behavior was considerate. Soft-switching control techniques was analyzed and compared with basic regulation's method of buck converter. Influence of current-mode of operation was explored. Efficiency of about 76 % at 400 MHz switching frequency is illustrated for voltage conversion from 3.6 V to 1.2 V.

Keywords: dc-dc converter, fully monolithic design, efficiency, CMOS 0.35 μm technology

1. INTRODUCTION

Today, battery operated portable electronic devices such as cellular phones, pagers, laptop computers; palm-size devices became very popular. A way to decreasing the size, weight and consequently the price of these devices is miniaturizations. Process technology scales and the circuits integrated on chip became more sophisticated. One of the major problems is how to use much more efficiently energy from battery. Requirements for longer battery life are very important for portable electronic (communication) devices. An approach is to minimize power dissipation in LSI (Large-Scale Integration) circuits used in the above mentioned equipment. Effective way to lower the power dissipation in LSI is to decrease operating voltage V_{dd} . Power dissipation (losses) are proportional to V_{dd} . They are two methods to reduce voltage from battery to the desire level – linear regulation (linear regulators) and switch mode dc-dc conversion (dc-dc converters). Principle of switch-mode dc-dc conversion gives many advantages from the efficiency point of view. Monolithic buck converter for RF applications was investigated on AMS CMOS 0.35 μm technology. The main goal of this research is analysing circuit at different working conditions and find the region where could be received the best efficiency results.

2. PROBLEM STATEMENT

To reduce size of dc-dc converters is necessary to be integrated all of the components on chip. A high switching frequency is the key design parameter, which gives permission to make monolithic integration of active and passive devices and to achieve high efficiency. At this high switching frequency, the energy dissipated in power MOS transistors dominates the total losses in dc-dc converter. To receive the

best possible efficiency we need to operate exactly at the frequency, where the inductor of low-pass filter has maximum quality factor Q . In CMOS technology, passive components and especially integrated inductor are very lossy. The passive components are for energy storage and output filtering.

Efficiency, current ripple and output voltage ripple are the main important parameters in the dc-dc switching-mode buck converter. To build high efficiency buck converter with small current ripple, big inductor with high quality factor Q is needed. Because of the technology limitations that's not possible at the moment. In order to reduce inductor's value, high switching frequency f_s of the main power switch have to be utilized. On the other hand with increasing of f_s , losses in the switches are increased. This leads to degrading of efficiency of the converter, because of the proportionality between losses and switching frequency f_s . The requirements of dc-dc converter to be fully monolithic and to have high efficiency are opposite.

3. RESULTS

In Fig. 1 is presented investigated circuit of well known switch-mode buck converter. AMS CMOS 0.35 μm process is used for simulations.

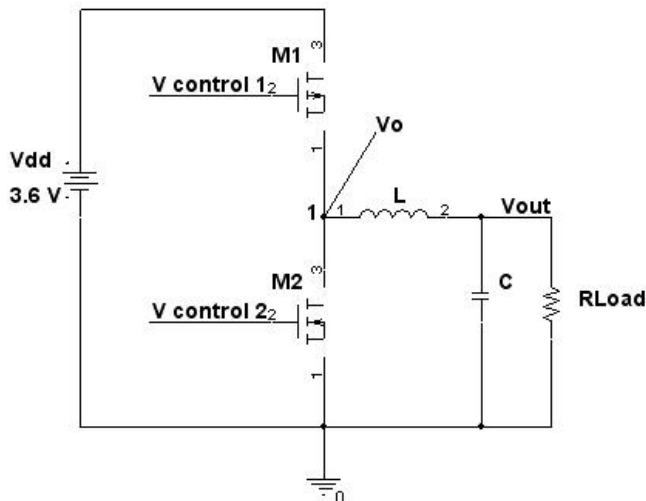


Fig. 1 Buck Converter.

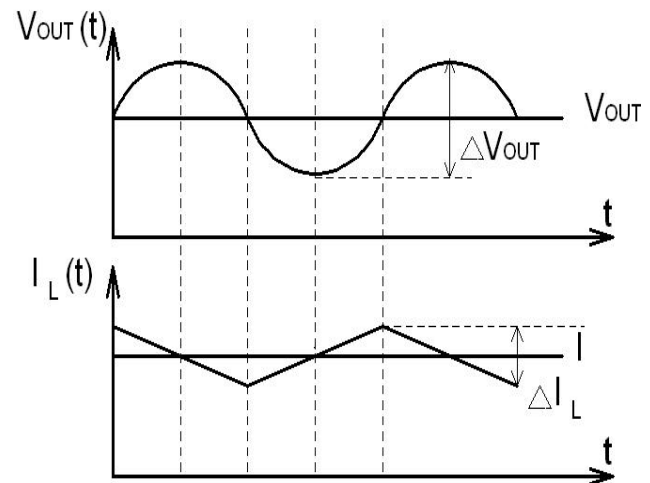


Fig. 2 Waveforms of output voltage and inductor current.

In Fig. 2 are shown waveforms of the output voltage and inductor current. Efficiency is the main important parameters in the dc-dc switching-mode buck converter and can be expressed as:

$$\eta = \frac{P_{OUT}}{P_{IN}} \quad (1)$$

where P_{OUT} is output power of the converter,

$$P_{OUT} = \frac{V_{OUT(av)}^2}{R_{Load}} \quad (2)$$

and P_{IN} is input power,

$$P_{IN} = I_{IN(av)} \times V_{dd} \quad (3)$$

They are couple of factors which affect to the efficiency behavior.

3.1 Switching frequency - f_s

Power dissipations in the transistors are proportional related with the switching frequency. In the other hand high frequency is desirable, because this allows sizes of the filter components to be smaller. This is very important when we talk about fully monolithic dc-dc converter, where all the elements including filter are integrated on the chip. One of the major problems utilizing monolithic passive components and especially inductors is there low Q factor, coming from the technology limitations. In these investigations wave shapes of the current through the transistors are kept constant with the variation of the f_s (at the same time values of the inductors was changed). In Fig. 3 are graphically presented simulated results, which expressed how efficiency η depends from f_s . Simulations was done at constant inductor's current ripple – ΔI_L . As can be seen in Fig. 3 with increasing of f_s efficiency goes down. The explanation is proportionality between f_s and transistor's losses.

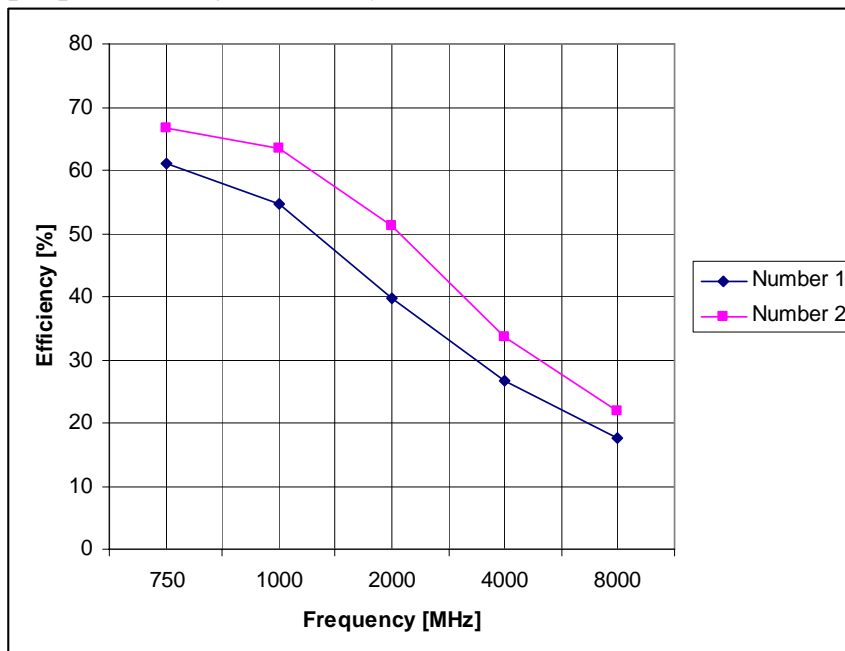


Fig. 3 Efficiency vs. frequency f_s ($\Delta I_L = \text{const.}$)

- (1) two transistors are reverse regulated.
- (2) transistor M2 is switched “on” with delay after switching “off” of M1.

3.2 Soft switching

If diode in the standard buck converter is replaced by the transistor (M2), controlled in appropriate manner could be achieved zero voltage switching (ZVS). This could be realized with regulation of the switch “on” time of that transistor, after the switch “off” of the main transistor (M1). Similar type of regulation is known as a soft switching. Because of ZVS efficiency results can be improved. Simulations received after utilizing this method shows better results compare to the standard way

of regulation. This is illustrated in Fig. 3, where curve number 1 and curve number 2 shows results received respectively after reverse regulation of the transistors and after soft switching.

3.3 Shape of the current through the transistors

Other factor which affect to the efficiency η is shape of the current through transistors. They are two boundary cases which are illustrated in Fig. 4. When the inductor is huge this current has rectangular shape – Fig. 4a. Fig. 4b indicates the work of the converter at the boundary between discontinuous and continuous conduction mode. At this mode Zero Current Switching (ZCS) can be achieved. When the shape of the current trough the switching transistor is similar to the shape shown in Fig. 4b, transistor is switching “on” at zero current.

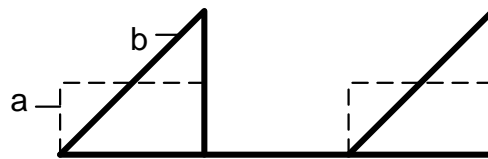


Fig. 4 Current through the transistor.

This phenomena leads to decreasing of power losses of transistors and consequently increasing of η .

3.4 Input voltage and load current

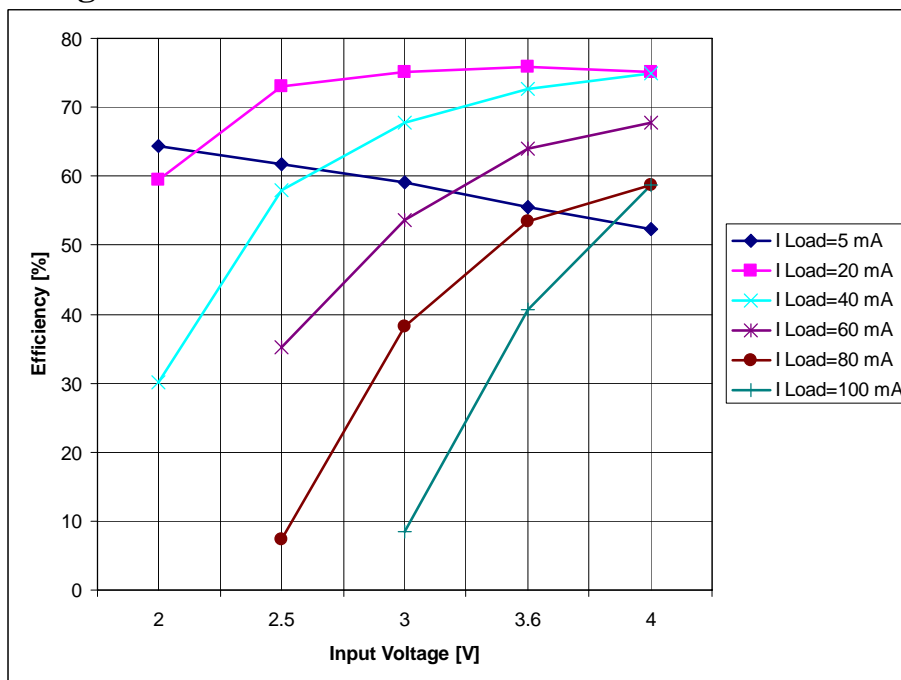


Fig. 5 Efficiency vs. Input Voltage (with ideal inductor) – $f_s = \text{const.}$

In Fig. 5 are shown family of curve which illustrated how efficiency η depend from input voltage at different load currents. The simulations for all of the cases in this figure were done at switching frequency equal to 400 MHz. From the picture bellow is obvious, that the best results are at load current equal to 20 mA. At this current converter operate at boundary between discontinuous and continuous

conduction mode. With other words in this case ZCS is achieved. As was mention in 3.3 this will be improve the efficiency η results. Simulations results presented in Fig. 5 prove that.

3.5 Q factor of the integrated inductor

From the efficiency point of view is better to be used offchip inductor, because of the higher possible inductance and better Q factor. To reduce size of dc-dc converters is necessary all of the components to be integrated on chip. Monolithic inductors have very low Q factor and efficiency goes down. In Fig. 6 are given graphically presented simulations results received after the use of standard AMS inductor. They are performing at the same condition like the results shown in Fig. 5.

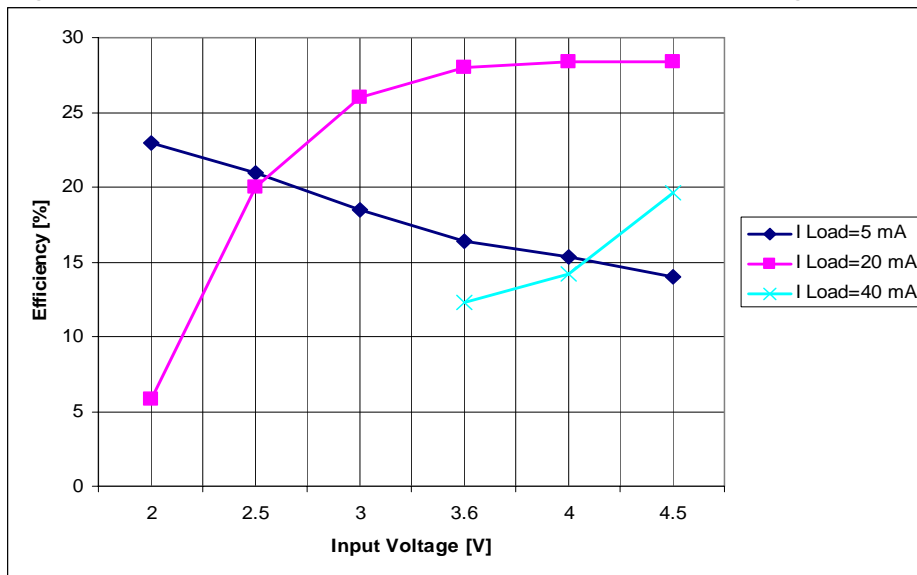


Fig. 6 Efficiency vs. Input Voltage (real ideal inductor) – $f_s = \text{const.}$

3.6 Current mode of operation of the converter

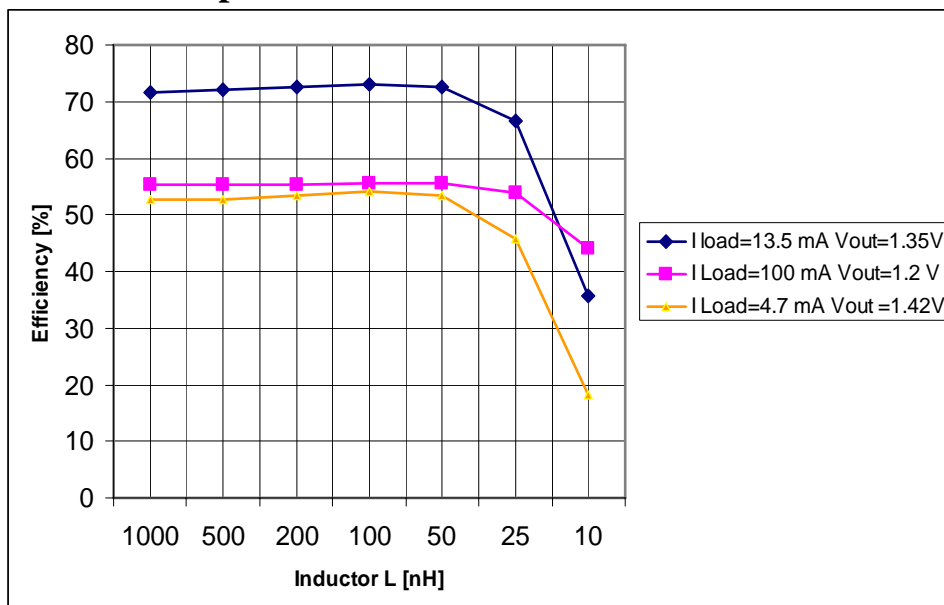


Fig. 7 Efficiency vs. inductor current ripple $I_{Load} = \text{const.}; f_s = \text{const.}; V_{in} = \text{const.}$

In Fig. 7 are presented how efficiency depends from the inductance value. The graphics show, that optimum could found. This relation is gain connected to the current mode of operation of the dc-dc converter. At low inductance circuits operate at continuous mode of operation and η goes down.

The maximum is appearing when converter work at the boundary between boundary between discontinuous and continuous conduction mode. At high value of inductance circuit operate at discontinuous conduction mode. This statement is proved by the results illustrated in Fig. 7. As can be seen the maximum of efficiency η is around 50 nH where circuit work at this mode of operation.

4. CONCLUSIONS

Switch-mode buck dc-dc converter for RF applications was investigated on AMS CMOS 0.35 μm technology. The focus of this work was efficiency η dependence from circuit's parameter, mode of operation of presented architecture and methods of regulation of the transistors. Simulations results show 7% efficiency improving when soft switching method is used. The best achieved results were received when converter works at the boundary between boundary between discontinuous and continuous conduction mode. In this mode of operation the main transistor is switching "on" at zero current. Investigations shows, that basic buck converter present bad result when the standard integrated AMS CMOS 0.35 μm inductor is used. That's because of very low Q factor of the monolithic inductors.

5. ACKNOWLEDGMENTS

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