Efficiency Study of a 2.2 kV, 1 ns, 1 MHz Pulsed Power Generator Based on a Drift-Step-Recovery Diode

Lev M. Merensky, Alexei F. Kardo-Sysoev, Doron Shmilovitz, and Amit S. Kesar

***Abstract*— Drift-step-recovery diodes (DSRDs) are used in pulsed-power generators to produce nanosecond-scale pulses with a rise rate of the order of 1 kV/ns. A 2.2 kV, 1 ns pulsed power circuit is presented. The circuit features a single prime switch that utilizes a low-voltage dc power supply to pump and pulse the DSRD in the forward and reverse directions. An additional low-current dc power supply is used to provide a voltage bias in order to balance the DSRD forward with respect to its reverse charge. The DSRD was connected in parallel to the load. In order to study the circuit's efficiency, it was operated over a wide range of operating parameters, including the main and bias source voltages, and the trigger duration of the prime switch. A peak voltage of 2.2 kV with a rise time of less than 1 ns and a rise rate of 3 kV/ns was obtained, where the efficiency was 24%. A higher efficiency of 52% was obtained when the circuit was optimized to an output peak voltage of 1.15 kV. The circuit was operated in single-shot mode as well as in bursts of up to 100 pulses at a repetition rate of 1 MHz. The experimental results are supported by a PSPICE simulation of the circuit. An analysis of the circuit input and output energies with respect to the MOSFET and DSRD losses is provided.**

***Index Terms*— Circuit simulation, drift-step recovery diode, power semiconductor diode switches, pulse generation.**

I. Introduction

NANOSECOND pulsed-power generators can be used in applications such as ultrawideband ground-penetrating radars and underground detection [1], [2], the study of the effect of intense electric fields on biological matter [3], and accelerator beam steering [4]. Drift-step-recovery diodes (DSRDs) are fast opening switches which are suitable for use in these generators since they produce nanosecond pulses with high peak and average power. Especially when high pulse repetition frequency is used to achieve a high average power, the circuit efficiency becomes an important factor. This paper focuses on these aspects.

DSRDs use a fast reverse recovery characteristic. The physical principle of the reverse recovery effect was studied by numerous authors [5]–[8]. A DSRD-based circuit operates as follows. Typically, at the zero state there is no current flowing through any of the circuit components. As the circuit is triggered, a preliminary switch directs a forward current for pumping the DSRD. The current duration is typically a few tens to a few hundreds of nanoseconds. This current injects a plasma of charged carriers into the DSRD junction [9]. In the next step, a reverse current is directed through the DSRD. Since the DSRD junction is loaded with charged carriers, the DSRD will initially conduct this reverse current until all of the charges that were injected in the previous step are removed. The DSRD will then rapidly cut off the current. Typical DSRDs may produce switching rates of the order of 1 kV/ns, such as 1 kV in 1 ns, 500 V in 0.5 ns, or 100 V in 0.1 ns [10].

Circuits for driving DSRDs have been studied and presented in numerous topologies, see [11] and [12]. These circuits use a preliminary switch that serves as a compression stage for driving the DSRD. In [13], a 3 kV, 5 ns preliminary compression stage consisting of a transistor and a nonlinear transformer was used to drive the DSRD. The reported efficiency for this preliminary stage was between 40% and 50%.

A theoretical analysis shows that the ratio between the circuit's capacitors and inductors has to be carefully chosen in order to efficiently drive the DSRD [3]. In [14], a solid-state-based Marx generator was used along with a saturating transformer for driving a bank of junction recovery diodes. The authors concluded that, in order to efficiently obtain large pulse amplitudes, the Marx bank should apply a high voltage across the saturating transformer.

A DSRD-based circuit for driving a silicon avalanche diode to produce an output pulse of 1.8 kV with a rise time of 100 ps was described in [15]. In that paper, the values of the circuit components were optimized and an efficiency of 22.9% was reported.

A circuit for DSRD characterization, in which the forward and reverse currents through the DSRD could be controlled independently, was described in [16]. In that paper, the balance between the input and output energies with respect to the circuit switching losses was obtained.

An experimental study of the efficiency of a DSRD-based pulsed power circuit has not been presented yet. This paper presents a 2.2 kV, 1 ns pulsed-power circuit based on a DSRD. The objectives of this paper are to measure the circuit efficiency with respect to its operating parameters and to analyze the switching losses.

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L. M. Merensky and A. S. Kesar are with the Applied Physics Division, Soreq Nuclear Research Center, Yavne 81800, Israel (e-mail: levme@soreq.gov.il; kesar@soreq.gov.il).

A. F. Kardo-Sysoev is with the Power Semiconductor Devices Laboratory, Ioffe Physical Technical Institute, St. Petersburg 194021, Russia (e-mail: alx@helen.ioffe.rssi.ru).

D. Shmilovitz is with the School of Electrical Engineering, Department of Engineering, Tel Aviv University, Tel Aviv 69978, Israel (e-mail: shmilo@post.tau.ac.il).

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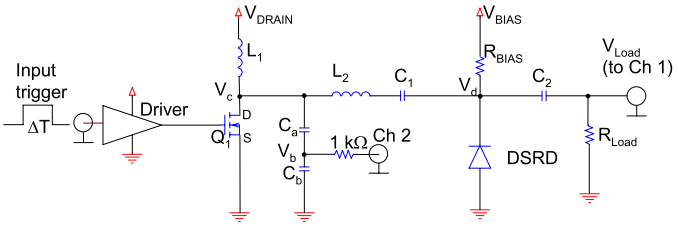

Fig. 1. DSRD-based pulsed-power circuit.

TABLE I
CIRCUIT PARAMETERS

Pump coil, L_1	85 nH
L_2	70 nH
C_1	2.2 μF
C_2	1 μF
C_a, C_b	200 pF each
R_{BIAS}	7.5 kΩ
Load impedance, R_{Load}	50Ω

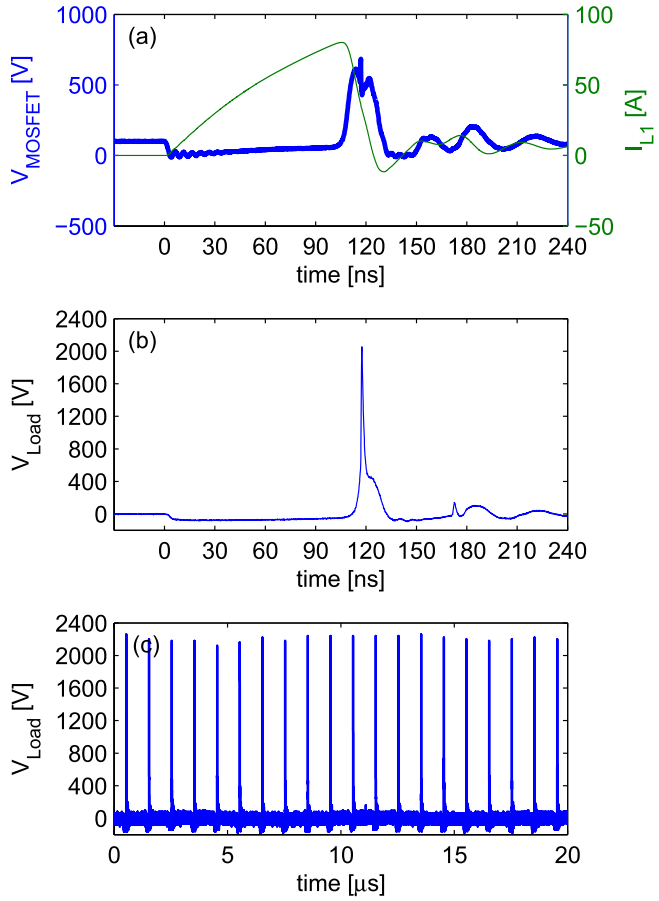

Fig. 2. Circuit signal versus time for $\Delta T = 100$ ns. (a) MOSFET voltage (left axis, thick line) and the current through L_1 (right axis, thin line). (b) Load voltage for a single pulse. (c) Load voltage by a trigger burst of 20 pulses at a repetition rate of 1 MHz. In (a) and (b), V_{DRAIN} is 100 V, and in (c) V_{DRAIN} is 120 V.

II. EXPERIMENTAL SETUP

The pulsed-power circuit is shown in Fig. 1. The circuit parameters are given in Table I. The inductors consist of air coils. The transistor marked as Q_1 is a power MOSFET, DE475-102N21A, produced by IXYS. This transistor serves as a prime switch. The DSRD was fabricated at the Ioffe Physical Technical Institute, St. Petersburg, Russia, and was constructed from a stack of several p^+–p–n–n^+ chip diodes.

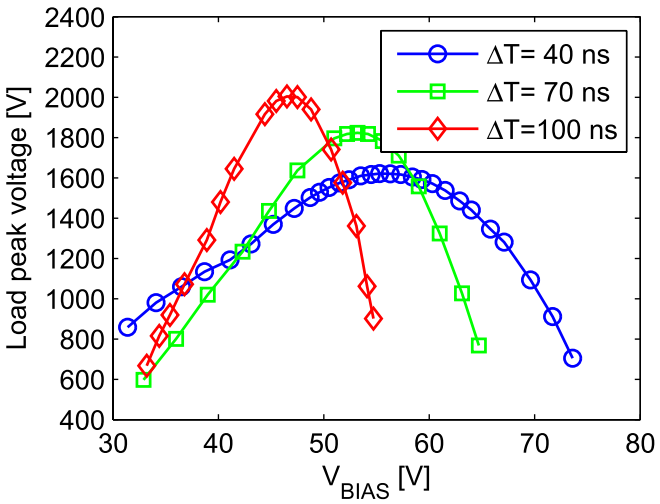

Fig. 3. Load peak voltage versus V_{BIAS} where ΔT was 40 ns (circles), 70 ns (squares), and 100 ns (diamonds). V_{DRAIN} was kept constant at 100 V.

The circuit operation is as follows. Initially at time $t = 0$, the MOSFET is turned off and no current flows in the circuit. The capacitor C_a is charged to V_{DRAIN} while C_b is discharged. The capacitor C_1 is charged to a dc bias voltage $V_{\mathrm{DRAIN}} - V_{\mathrm{BIAS}}$, where $V_{\mathrm{DRAIN}} > V_{\mathrm{BIAS}}$, and the dc block capacitor C_2 is charged to V_{BIAS}.

The power MOSFET Q_1 is driven by an input trigger pulse with a duration ΔT of a few tens of nanoseconds. When the MOSFET is turned on, the inductor L_1 is charged via V_{DRAIN} while the DSRD is pumped in the forward direction by the energy in C_1. At the end of the input trigger, the MOSFET is turned off and the energy stored in L_1 is transferred to L_2 through C_a and C_b to pulse the DSRD in the reverse (cathode to anode) direction. This reverse current drains the stored charge that was pumped previously into the DSRD junction. When the stored charge in the DSRD junction is removed, the DSRD rapidly turns off within a nanosecond timescale, causing the current to pass through C_2 to the load in a nanosecond pulse form.

The circuit contains two measuring channels that were connected to an oscilloscope. The load voltage, Channel 1, was measured via a −86 dB attenuator. The MOSFET drain voltage V_C was measured through the network of C_a, C_b, and a 1 kΩ resistor in series to the oscilloscope 50 Ω input impedance (1/21 voltage divider) of Channel 2. The MOSFET drain voltage is therefore

$$V_C(t) = V_{C_a}(t) + V_{C_b}(t) \tag{1}$$

where $V_{C_b} = 21 V_{CH2}$, $V_{C_a}(t) = V_{C_a}(0) + {C_a}^{-1} \int_0^t I_{C_a}(\tau)\, d\tau$, and the current through C_a is

$$I_{C_a}(t) = \frac{V_{C_b}(t)}{1050} + \frac{1}{C_b}\frac{dV_{C_b}}{dt}. \tag{2}$$

The charging current of L_1 can be calculated from (1) as

$$I_{L_1}(t) = \frac{1}{L_1}\int_0^t [V_{\mathrm{DRAIN}} - V_C(\tau)]\, d\tau \tag{3}$$

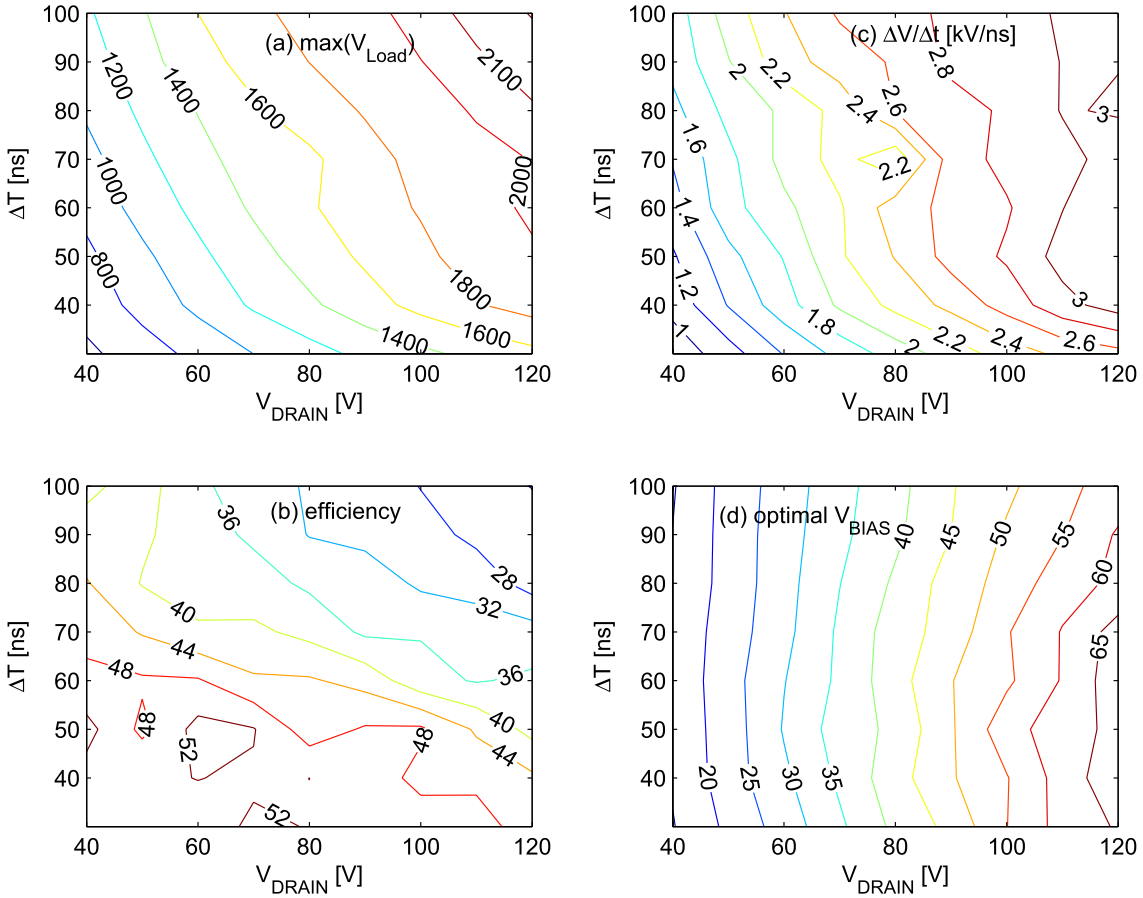

Fig. 4. Contour plots of the load peak voltage (a), efficiency (b), the maximum rise-rate of the pulse (c), and optimal tuning voltage (d) versus the supply voltage, V_{DRAIN}, and trigger duration, ΔT.

and in each pulse the energy extracted from V_{DRAIN} is

$$E(\text{Drain supply voltage}) = V_{\mathrm{DRAIN}} \int I_{L_1}(t)dt. \quad (4)$$

The total energy dissipated on the load is

$$E(\text{Load}) = R_{\mathrm{Load}}^{-1} \int |V_{\mathrm{Load}}(t)|^2 \, dt. \quad (5)$$

Assuming negligible energy extracted from V_{BIAS} compared to the energy extracted from V_{DRAIN}, the efficiency is

$$\eta[\%] = \frac{E(\text{Load})}{E(\text{Drain supply voltage})} 100. \quad (6)$$

III. Results

The circuit presented in Fig. 1 was operated with the parameters shown in Table I and $\Delta T = 100$ ns. Fig. 2(a) shows the MOSFET signal by (1) (thick line, left axis) and the current through L_1 by (3), both measured via Channel 2. Fig. 2(b) shows the load voltage for a single pulse, and Fig. 2(c) shows a burst of 20 pulses at a repetition rate of 1 MHz. The circuit was operated in bursts of up to 100 pulses at a repetition rate of 1 MHz. In Figs. 1(a) and (b), V_{DRAIN} was 100 V, and in (c) V_{DRAIN} was 120 V.

The peak voltage at the load for $V_{\mathrm{DRAIN}} = 100$ V and $\Delta T = 100$ ns was 2.0 kV and its rise time was less than 1 ns. From (4) and (5), it follows that the supply and load energies were 558 and 155 μJ, respectively. Thus, the average power during the 1 MHz burst was 155 W.

The effect of the tuning voltage V_{BIAS} on the load peak voltage is presented in Fig. 3 for $V_{\mathrm{DRAIN}} = 100$ V and $\Delta T = 40$ ns (circle marks), 70 ns (square marks), and 100 ns (diamond marks). From this figure, it follows that the long trigger duration (i.e., 100 ns) resulted in the highest load voltage, and that, as the trigger duration increased, the load voltage became more sensitive to the tuning voltage.

Fig. 4 presents the contour plots of (a) the load peak voltage, (b) the efficiency by (6), and (c) the maximum rise rate of the pulse in units of kV/ns measured over an interval of 0.5 ns, versus the supply voltage V_{DRAIN} and trigger duration ΔT. The highest peak voltage of 2.2 kV with a rise rate of 3 kV/ns was obtained when V_{DRAIN} was 120 V and ΔT was 100 ns. The efficiency at this operating point was 24%. The highest efficiency of 52% was obtained when V_{DRAIN} was 60 V and ΔT was 50 ns, resulting in a load peak voltage of 1.15 kV. The tuning voltage V_{BIAS}, resulting in the maximum peak voltage in Fig. 4(a), is presented by the contours in Fig. 4(d). As seen in this figure, the optimal tuning voltage depends mostly on V_{DRAIN}. The relationship can be approximated as $V_{\mathrm{BIAS}}^{\mathrm{Optimal}} \simeq 0.614 V_{\mathrm{DRAIN}} - 8.31$.

IV. Simulation

The circuit presented in Fig. 1 was simulated by a PSPICE simulation with the same passive components as given in

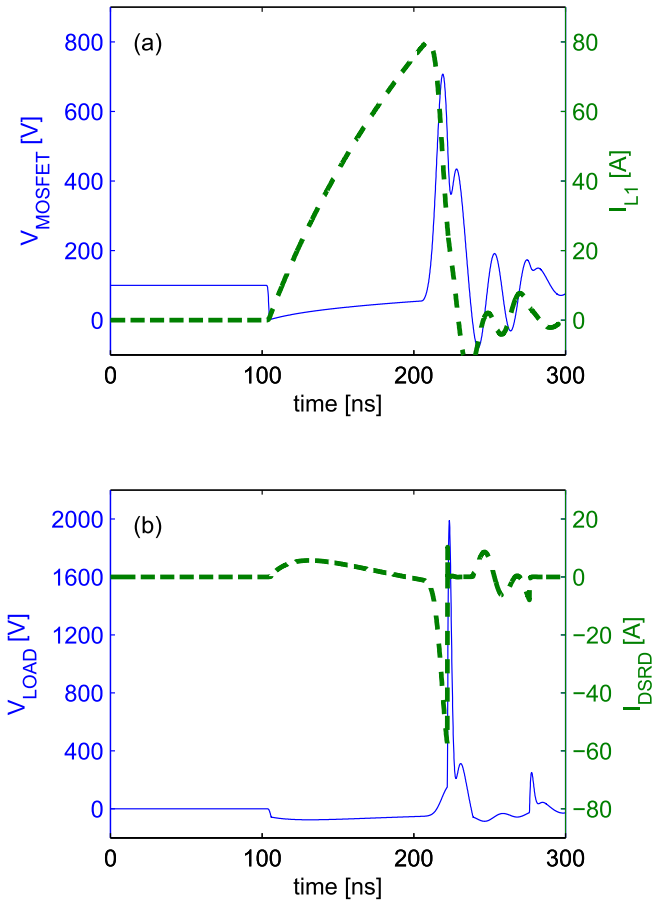

Fig. 5. (a) Simulation of the MOSFET voltage (solid line, left axis) and the current through L_1 (dashed line, right axis). (b) Simulation of the load voltage (solid line, left axis) and the DSRD current (dashed line, right axis).

Table I. The MOSFET was modeled as a nonideal switch taking into account its rise and fall time, its output capacitance, and its dynamic resistance in the conducting mode. Since there was no available PSPICE model for the DSRD that we used, it was found that the DSRD behavior could be simulated by placing a 1N4007 diode in parallel with a 15 pF capacitor, with both components in series with a 3.5 Ω resistor.

Fig. 5 presents pulse waveforms versus time obtained by the PSPICE model, where V_{DRAIN} was 100 V and V_{BIAS} was 54 V. The MOSFET drain voltage (solid line, left axis) and the current through L_1 (dashed line, right axis) are shown in Fig. 5(a). The peak MOSFET drain voltage was 708 V and the maximum current was 80 A. The load voltage (solid line, left axis) and the DSRD current (dashed line, right axis) are shown in Fig. 5(b). The load peak voltage was 1.99 kV and the rise time was ∼1 ns. It is seen that the DSRD turned off when its reverse current was −58 A. The DSRD charge can be analyzed by an integration on its current $Q_{DSRD} = \int I_{DSRD}\, dt$ (not shown in the figure). It follows that the turn off time of 222 ns occurred when the charge dropped to zero, in agreement with the expected behavior of DSRDs [12], [16]. Energy analysis shows that the energy drawn from the drain supply voltage was 558 μJ, the MOSFET and DSRD switching losses were 317 and 53 μJ, respectively, and the load energy was 187 μJ.

V. Conclusion

A 1 ns pulsed power circuit based on a DSRD was presented. The circuit features a single prime switch that uses a low-voltage (less than 120 V) dc power supply in order to pump and pulse the DSRD in the forward and reverse directions. An additional low-current dc power supply was used to provide bias in order to balance the DSRD forward with respect to its reverse charge. The DSRD was connected in parallel to the load. The pulse peak voltage was 2.2 kV with a rise time of less than 1 ns and a rise rate of 3 kV/ns. Thus, the dc to peak pulse compression was 18.3. The circuit was operated in the single-shot mode as well as in burst mode of up to 100 pulses at a repetition rate of 1 MHz, i.e., an average power of 155 W during the burst.

Parametric study, Fig. 4, revealed a compromise between high efficiencies at low values of V_{DRAIN} and ΔT versus high peak power at higher values of these parameters. This behavior is circuit dependent, and in our circuit relates mostly to the MOSFET and DSRD rating.

A PSPICE simulation was carried out in order to deepen our understanding on the circuit operation. We modeled the MOSFET as a nonideal switch. The DSRD was modeled by a 1N4007 diode in parallel with a 15 pF capacitor, with both components in series with a 3.5 Ω resistor. Comparing the simulation and experimental results shows that a good correlation was obtained for the current through L_1 and the load peak voltage. A spike in the MOSFET signal is seen at time $t = 120$ ns in Fig. 2(a). This is due to the fast rising voltage of the DSRD. The discrepancy between the energy of the load (155 μJ in the experiment and 187 μJ in the simulation at $V_{DRAIN} = 100$ V and $\Delta T = 100$ ns) is probably related to inaccurate modeling of the DSRD. In order to obtain a joint energy analysis of the experimental and simulation results, we believe that the simulation's MOSFET 57% losses can be taken into account in order to conclude that the DSRD losses were 15%.

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References

[1] V. Prokhorenko, V. Ivashchuk, and S. Korsun, "Ground penetrating radar VIY-2," *IEEE Aerosp. Electron. Syst. Mag.*, vol. 20, no. 7, pp. 16–18, Jul. 2005.

[2] A. S. Kesar, "Underground anomaly detection by electromagnetic shock waves," *IEEE Trans. Antennas Propag.*, vol. 59, no. 1, pp. 149–153, Jan. 2011.

[3] J. M. Sanders, A. Kuthi, Y.-H. Wu, P. T. Vernier, and M. A. Gundersen, "A linear, single-stage, nanosecond pulse generator for delivering intense electric fields to biological loads," *IEEE Trans. Dielectr. Electr. Insul.*, vol. 16, no. 4, pp. 1048–1054, Aug. 2009.

[4] F. Arntz, A. Kardo-Sysoev, and A. Krasnykh, "SLIM, short-pulse technology for high gradient induction accelerators," in *Proc. IET Eur. Pulsed Power Conf.*, 2009, pp. 1–4.

[5] H. Benda and E. Spenke, "Reverse recovery processes in silicon power rectifiers," *Proc. IEEE*, vol. 55, no. 8, pp. 1331–1354, Aug. 1967.

[6] I. V. Grekhov, V. M. Efanov, A. F. Kardo-Sysoev, and S. V. Shenderey, "Power drift step recovery diodes (DSRD)," *Solid-State Electron.*, vol. 28, no. 6, pp. 597–599, 1985.

[7] J. D. Taylor, *Ultra-Wideband Radar Technology*. New York, NY, USA: CRC Press, 2001.

[8] R. Baburske, B. Heinze, J. Lutz, and F.-J. Niedernostheide, "Charge-carrier plasma dynamics during the reverse-recovery period in p^+-n^--n^+ diodes," *IEEE Trans. Electron Devices*, vol. 55, no. 8, pp. 2164–2172, Aug. 2008.

[9] A. Kyuregyan, "Theory of drift step-recovery diodes," *Tech. Phys.*, vol. 49, no. 6, pp. 720–727, 2004.

[10] V. A. Kozlov, I. A. Smirnova, S. A. Moryakova, and A. F. Kardo-Sysoev, "New generation of drift step recovery diodes (DSRD) for subnanosecond switching and high repetition rate operation," in *Proc. Conf. Rec. 25th Int. Power Modulator Symp. High-Voltage Workshop*, 2002, pp. 441–444.

[11] A. F. Kardo-Syssoev, V. M. Efanov, S. V. Zazulin, and I. G. Tchashnikov, "Pulse generating circuits using drift step recovery devices," U.S. Patent 6 087 871, Feb. 26, 1997.

[12] A. F. Kardo-Sysoev, "New power semiconductor devices for generation of nano- and subnanosecond pulses," in *Ultra-Wideband Radar Technology*, J. D. Taylor, Ed. New York, NY, USA: CRC Press, 2001, ch. 9.

[13] V. S. Belkin and G. I. Shulzchenko, "Forming of high-voltage nanosecond and subnanosecond pulses using standard power rectifying diodes," *Rev. Sci. Instrum.*, vol. 65, no. 3, pp. 751–753, 1994.

[14] J. M. Sanders, A. Kuthi, and M. A. Gundersen, "Optimization and implementation of a solid state high voltage pulse generator that produces fast rising nanosecond pulses," *IEEE Trans. Dielectr. Electr. Insul.*, vol. 18, no. 4, pp. 1228–1235, Aug. 2011.

[15] L. M. Merensky, A. F. Kardo-Sysoev, A. N. Flerov, A. Pokryvailo, D. Shmilovitz, and A. S. Kesar, "A low-jitter 1.8-kV 100-ps rise-time 50-kHz repetition-rate pulsed-power generator," *IEEE Trans. Plasma Sci.*, vol. 37, no. 9, pp. 1855–1862, Sep. 2009.

[16] A. S. Kesar, Y. Sharabani, L. M. Merensky, I. Shafir, and A. Sher, "Drift-step-recovery diode characterization by a bipolar pulsed power circuit," *IEEE Trans. Plasma Sci.*, vol. 40, no. 11, pp. 3100–3104, Nov. 2012.

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