Efficient 3D Modelling for Extraction of Interconnect Capacitances in Deep Submicron Dense Layouts

A. Toulouse, D. Bernard, C. Landrault and P. Nouet
LIRMM, UMR C55060 CNRS / Université Montpellier II
Tel: (+33) 467.41.85.27 Fax: (+33) 467.41.85.00 E-mail: nouet@lirmm.fr

Abstract

This paper introduces a set of analytical formulations for 3D modelling of inter-layer capacitances. Efficiency and accuracy are both guaranteed by the process characterization approach. Analytical modelling of interconnect capacitances is then demonstrated to be an helpful alternative to lookup tables or numerical simulations.

1. Introduction

It is now well established that interconnects drastically affect performances of VLSI circuits [1-3]. Even if resistances must be taken into account, capacitances remain the most limiting factor.

On the one hand, they affect the total load that must be driven by logical gates. Power consumption is then directly dependent to this capacitive load while propagation delays can only be deduced from the study of distributed RC networks. On the other hand, crosstalk evaluation requires the knowledge of node to node capacitive coupling. Finally, capacitance extraction from a layout must be investigated at different levels:

- at node level, only node total capacitance is required to evaluate power consumption,
- at node-to-node and distributed network levels, mutual capacitances must be computed to evaluate crosstalk and elementary capacitances.

It is then a major concern to evaluate node to node mutual capacitances.

2. State of the art

2.1. Analytical formulations

Numerous analytical models have been published [4-8]. They are generally based on formulations validated by numerical simulations. They exhibit a lack in accuracy that is due to several assumptions on technology such as the shape of wire cross-sections (rectangular, trapezoid,...) and planarity. Moreover, these formulations generally require a reference plane to compute accurately capacitances.

2.2. Standard model

Post-layout extractors generally use 2D "flattened" models [9] and foundries are providing parameters for such "standard" models by measuring large dimension capacitors or a set of small capacitors connected in parallel.

The simplest model for inter-layer capacitances is the plate capacitor one. Edges of both plates are coincident and physical modelling is achieved by the decomposition of the total capacitance in two terms: the capacitance per area unit (C_S) and the capacitance per perimeter unit (C_{SW}).

For two overlapping wires (Fig. 1), it is then necessary to take into account fringing capacitances of layer edges inside layer track (C_{ij} and C_{ji}) that are higher than C_{SW} used for coincident edges. It comes:

$$C_x = C_S.A + C_{SW}.L_{SW} + C_{ij}.L_{ij} + C_{ji}.L_{ji} \quad (1)$$

where A is the overlapping area and L_{SW}, L_{ij} and L_{ji} are respectively the part of the overlapping perimeter corresponding to coincident edges, non-coincident edges with layer i inside layer j and non–coincident edges with layer j inside layer i. Consequently, the sum $L_{SW} + L_{ij} + L_{ji}$ is equal to the whole perimeter of the overlapping area between layer i and j.

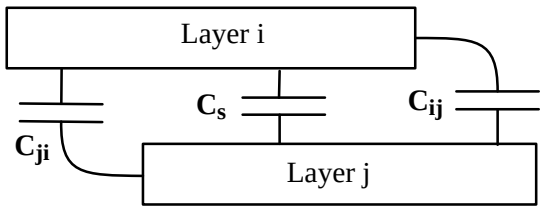

Figure 1: Fringing and area effects on node to node interlayer mutual capacitance.

2.3. Look-up tables

New emerging techniques for capacitance extraction from a layout use look-up tables [10]. Starting from a vertical description of a given technology, numerical simulations are

performed to build a table with a set of reference data for specific patterns. During post-layout extraction, elementary capacitances are then calculated by identification and extrapolation from the more convenient patterns in the table.

2.4. Accuracy fundamentals

When dealing with interconnect capacitance extraction, accuracy remains a major concern. Due to the large diversity of patterns, accuracy must be evaluated in terms of minimal and maximal uncertainty on each elementary pattern rather than averaged on a wide range of patterns.

Numerical finite element simulations can address high accuracy under the assumption of a perfect knowledge of process dependent effect such as under or over etching. Consequently, silicon data are required for verification.

In our approach, we are first using silicon patterns for calibration and numerical simulations are only used to verify boundary effects or tendencies.

3. Technology characterization and calibration

Extraction model calibration use to be performed using unrealistic patterns while silicon verification was only implemented at the electronic cell or system level. In using a realistic set of interconnect test patterns, we are now able to calibrate extraction models and then to monitor a given process during its life.

3.1. Test patterns for characterization

In this paper, we have chosen to illustrate our approach with the modelling of Metal1 (M1) / Metal2 (M2) capacitive coupling. Concerning this pair of layers, we have designed a set of 23 realistic test patterns. These patterns are sufficient to exhibit limitations of the standard model due to:

- dependence of the fringing coefficients on the extension of one layer with respect to the other one,
- dependence of a given coupling on the vicinity of unrelated lines,
- small dimension effects.

This silicon based characterization approach was not previously used due to two essential drawbacks:

- the number of patterns that are required to fully characterize all interconnection layers of a particular technology is huge (several hundreds for a 6 metal layer technology),
- capacitance measurement resolution in the 100 aF range is necessary to exhibit small dimension effects.

3.2. Test pattern on-chip measurement

In order to measure a large number of interconnect capacitance test patterns, we are using an on-chip measurement technique. Two techniques have been investigated. Both exhibit sub-fF measurement capabilities. The first one [11,12] is more simple in terms of experimental setup but it is more convenient for characterization at node level than for node to node mutual capacitance evaluation. The second technique we are using [13] allows measurement of the whole set of node-to-node capacitances at the expense of a small silicon area and pin overhead (about 1 I/O PAD and 0.1 mm^2 by capacitance).

3.3. Standard model calibration

From measured values, we first extract the four parameters of the standard model accordingly to four dedicated test patterns: a large plate capacitor, two coincident stacked lines, a M2 line over a M1 plane and a M1 line under a M2 plane. As a rule of thumb, it is worth noting that the width of metal lines is set to the minimum pitch to increase sensitivity to fringing effects.

Table 1: Extracted parameters.

Parameters	Fast	Typ.	Slow	Extr.
C_S (aF/μm^2)	45	49	55	41.92
C_{SW} (aF/μm)	19	22	24	46.82
C_{12} (aF/μm)	19	22	24	59.32
C_{21} (aF/μm)	75	82	92	72.12
Error (%)	26.7	24.6	22.7	12.7

In table 1, extracted parameters are given and compared with foundry parameters. It can be noticed that the process we used was a fast one. Moreover fringing effects in both coincident (C_{SW}) and M1 inside M2 (C_{12}) cases are strongly under-estimated by the foundry.

3.4. Limitations of the standard model

We have defined an accuracy estimator corresponding to the average error on the whole set of 23 patterns. For the standard model, this error is higher than 10 % even in the best case with ad-hoc parameters (called extracted, Extr). A more careful study demonstrates two limitations:

- fringing coefficients C_{ij} are constant,
- 3D effects are not modelled.

As an example, Figure 2 describes one family of test patterns dedicated to the characterization of M2 inside M1 fringing. Capacitance is measured between one M2 line and a M1 plane. First, only line number 2 is present at the center of the M1 plane. Several capacitances are measured for various extensions of M1 outside M2 edges (called L_{dep}). Increasing values of the mutual capacitance are obtained when increasing L_{dep}. Secondly, lines 1 and 3 are added and separation between M2 lines (S_{m2}) is set to different values while L_{dep} is equal to 10 μm. In this last case, mutual capacitance between M2 center line and M1 is decreasing

with S_{m2}. Both phenomenon are explained by a non constant fringing parameter C_{21}.

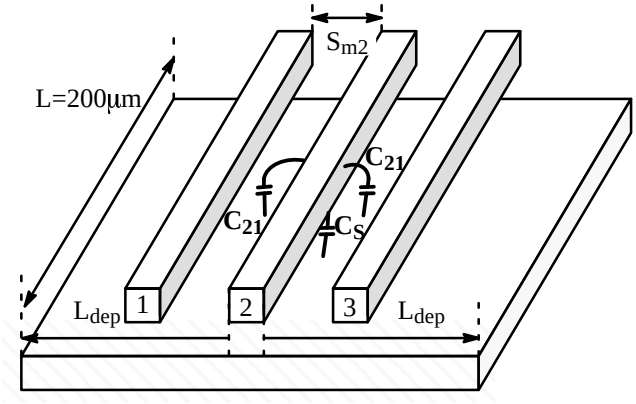

Figure 2: Test pattern for fringing effect.

4. Overview of our semi-empirical model

In our approach we are using simple relations based on quasi-physical parameters that can be directly extracted from a process characterization step. In that way, we are not making any assumptions neither on vertical dimensions nor on cross-sectional shapes. Starting from the standard model and its four parameters (equ. 1), we are introducing analytical functions to be used in place of the constant parameters for fringing effects (C_{21}, C_{12} and C_{SW}). Then we have added a new parameter to represent three dimensional effects due to elementary lines crossing.

4.1. Modelling the extension length

We first define the variation of the fringing coefficients with respect to L_{dep} by subtracting the area related contribution to each measured capacitance. We then obtain a fringing coefficient as a function of L_{dep}. The analytical expression is then built in order to range from both limit values, C_{sw} for coincident edges up to C_{ij} when layer j extend largely from layer i edge. This variation can be described as a function of the extension length by a decreasing exponential term. Using A_{ij} as a calibration parameter it comes:

$$C_{ij}(L_{dep}) = C_{SW} + (C_{ij} - C_{SW}) \cdot e^{-\frac{A_{ij}}{L_{dep}}} \qquad (2)$$

where C_{SW} and C_{ij} are constant parameters issued from the standard model. They correspond respectively to the fringing coupling for coincident edges (L_{dep}=0) and for large extension of layer j outside Layer i edge (L_{dep}>>A_{ij}). Both A_{21} and A_{12} are fitting coefficients that are determined for small extension magnitudes.

On Figure 3, results from our model are reported (C_{mod}) and compared with both the fast parameters given by the foundry (C_{fa}) and the measured parameters directly deduced from the technology calibration (C_{meas}). Positive (respectively negative) values of L_{dep} means extension of M1 (M2) outside M2 (M1). Boundary parameters from the standard model (C_{12}, C_{21} and C_{SW}) have also been reported. It is worth noting that negative values of L_{dep} have been used for graphic illustration purposes and remains without any physical signification.

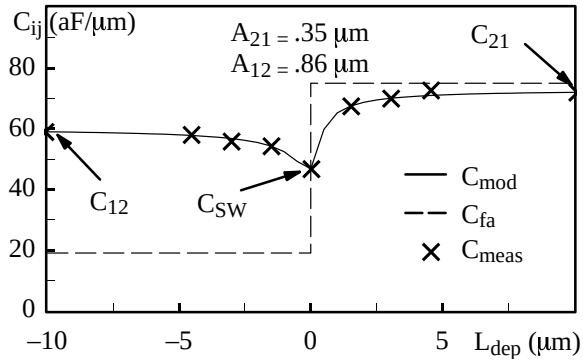

Figure 3: Fringing coefficient vs L_{dep}.

4.2. Modelling unrelated line effects

For realistic capacitive patterns, it is mandatory to take into account neighboring lines effect on the fringing coefficient. We use several test patterns described in Figure 2 to establish the reduction of mutual capacitance due to separation with unrelated lines #1 and #3. This "screening" effect is very important when neighbor lines are closer. Once again, an exponential term is used to describe the variation as:

$$C_{ij}(S_{mi}, L_{dep}) = C_{ij}(L_{dep}) \cdot e^{-\frac{S_{ij}}{S_{mi}}} \qquad (3)$$

where S_{ij} is a technology dependent parameter.

As an example, C_{21} (M2 line over a M1 plane) is reported on figure 4 for increasing separation (S_{m2}) between the center M2 line and unrelated lateral M2 lines. Accuracy of our model is demonstrated with respect to both simulated and measured capacitances. At that point, 2D numerical simulation has been used to verify the model over a wide range while only two measured points are available.

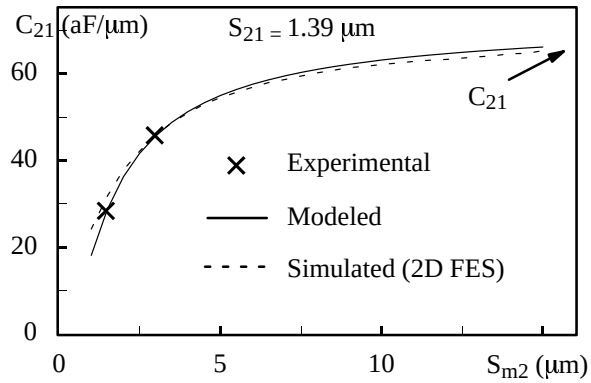

Figure 4: Fringing coefficient vs S_{m2}.

4.3. Modelling 3D effects

The last major improvement of our model concerns 3D effects. These effects can not be neglected in realistic small dimension patterns. On figure 5, we introduce our test pattern constituted by two sets of elementary lines describing a matrix. Our interest concern the modelling of the coupling between both central lines, i.e. lines 2 and 5.

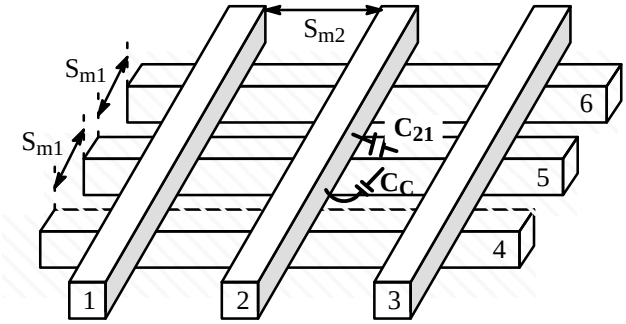

Figure 5: Test pattern for 3D effects.

In an earlier development of our model [14], we first propose to add a constant offset to the capacitance in order to modelize coupling outside the overlapping area. However, offset magnitude is dependant on the vicinity of unrelated lines. Finally, we have designed a set of nine test patterns with various uncorrelated separations between M1 and M2 lines. Once again, we observed that coupling variations can be described as an exponential variation in the following equation:

$$C_c(S_{m1}, S_{m2}) = C_0 + (C_c - C_0).e^{-\frac{C_1}{S_{m1}}-\frac{C_2}{S_{m2}}} \quad (4)$$

where C_c and C_0 represent respectively the maximum and minimum values of the offset due to one elementary corner. C_1 and C_2 are then determined to fit the variation of the corner effect for various separation between central lines and unrelated lateral lines.

5. Discussion

The proposed model must be discussed in terms of complexity, accuracy and efficiency.

Complexity of our model is really low compared to the one generally observed in accurate analytical models. No vertical dimensions are required and the total node-to-node capacitance is decomposed in only three terms with a physical origin: the area dependent coupling, the fringing coupling and the 3D coupling.

Accuracy is a major concern when extracting capacitances from a layout. In our approach we are dealing with boundaries to avoid side effects that can drastically affect accuracy during extraction. Using measured values to determine the boundaries of a given parameter and then a linear exponential variation to “link” both extreme values insure an accuracy well controlled and free of unexpected patterns.

Efficiency is guaranteed by the approach we have chosen. We are not providing complex analytical expressions or a black box tool but a real and complete methodology that allows in several identified steps to perform capacitance extraction with a standard industrial extraction tool and without any cross-sectional information on the process. It is worth noting that one of the more efficient aspects of this model concerns the validity of the equations without any assumption on a reference plane.

Both efficiency and accuracy are demonstrated on figure 6 where the accuracy of our model appears as an interesting alternative to the standard model (small number of parameters but inacurate) or look-up tables (high accuracy but large number of parameters).

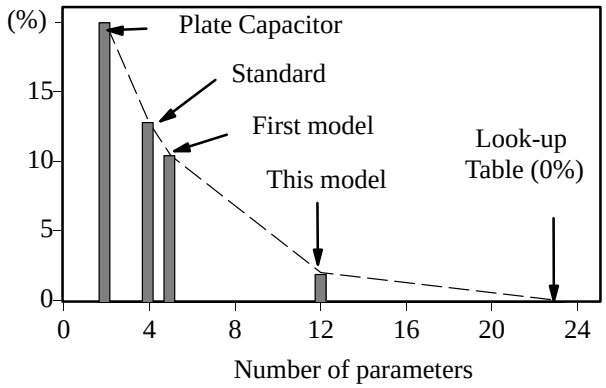

Figure 6: Average error (in percent) versus the number of parameters of each model.

6. Conclusions

In this paper we have introduced a complete methodology for the extraction of interconnect capacitances from a layout. Our methodology includes:

- the definition of a minimum set of test patterns in order to demonstrate the limitations of the standard model and to provide data to calibrate our model,
- an on-chip capacitance measurement technique allowing accurate measurement of very low node-to-node capacitances at a low silicon cost,
- a set of simple equations describing capacitive coupling in a deep submicron technology.

It is worth noting that similar work has been performed concerning intra-layer capacitances that are of particular interest for crosstalk noise evaluation.

Perspectives of our work concern the plug-in of our equations in a standard extraction tool in order to evaluate the computing cost of the proposed equations. This cost can already be related to the cost of extra information that must be extracted from the layout:

- the number of corners,
- the separation between a given line and its neighbors.

7. References

1. P. Felix, “Interconnects for ULSI: State of the art and Future trends”, Proc. ESSDERC, 1995, pp. 5–14.
2. K. Rahmat and al., “A Scaling Scheme for Interconnect in Deep–Submicron Processes”, Proc. IEDM, 1995, pp. 245–248.
3. M.T. Bohr, ”Interconnect Scaling - The Real Limiter to High Performance ULSI”, Proc. IEDM’95, pp. 241-244.
4. T. Sakurai, “Closed–Form Expressions for Interconnection Delay, Coupling, and Crosstalk in VLSI’s”, IEEE Trans. El. Dev., Vol. ED–40, No. 1, pp. 118–124, Jan. 1993.
5. G. S. Samudra and al., “A set of Analytic Formulas for Capacitance of VLSI Interconnects of Trapezium Shape,” IEEE Trans. El. Devices, vol. 41, no. 8, pp 1467–1469, Aug. 1994.
6. N. Delorme and al., “Inductance and capacitance analytic formulas for VLSI interconnects,” IEEE El. Device Letters, vol. 32, no. 11, pp 996–997, 1996.
7. N.D. Arora and al., “Modeling and Extraction of Interconnect Capacitances for Multilayer VLSI Circuits”, IEEE Trans. on CAD, Vol. CAD–15, No. 1, pp. 58–67, Jan. 1996.
8. C. Kortekaas, “Interconnect Capacitance Characterization for MOS–IC Process– and Circuit Design”, Proc. IEEE ICMTS’88, pp. 39–44, Vol. 1, No. 1, Feb. 1988.
9. Diva^{TM} Interactive Verification, Reference Manual, vol. 1, Cadence, Dec. 1992.
10. S.Y. Oh and al,”3D GIPER Global Interconnect Parameter Extractor for Full-Chip Global Critical Analysis”, Internationnal Electron Devices Meetings, pp. 615-618, 1996.
11. B. Laquai and al., “A new method and test structure for easy determination of femto–Farad on–chip capacitances in a MOS process”, Proc. ICMTS, Vol. 5, pp. 62–66, March 1992.
12. D. Sylvester and al., “Investigation of Interconnect Capacitance Characterization Using Charge-Based Capacitance Measurement (CBCM) Technique and 3D Simulation”, IEEE J. of Solid-State Circuits, Vol. 33, No 3, March 1998.
13. P. Nouet and al., ”A New Test Structure for Interconnect Capacitance monitoring”, ICMTS’97, pp. 81-84, March 1997.
14. P. Nouet and al., ”Use of Test Structures for Characterization and Modeling of Inter- and Intra-Layer Capacitances in a CMOS Process”, IEEE Trans. on Semiconductor Manuf., Vol. 10, No 2, pp. 233-241, May 1997.