Open access • Journal Article • DOI:10.1049/IET-SMT.2010.0032

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Published on: 19 Aug 2010 - Iet Science Measurement & Technology (IET)

Topics: Power integrity, Integrated circuit design, Signal integrity, Integrated circuit and Electromagnetic compatibility

Efficient Analysis and Design Strategies for RF Boards Dedicated to Integrity Monitoring of ICs Using an EM/Circuit Co-Design Technique

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Abstract

At the moment a lot of attention is devoted to power integrity (PI), signal integrity (SI), and electromagnetic compatibility (EMC) of integrated circuits (ICs). For PI-, SI-, and EMC-aware design, the modelling and characterisation of ICs is indispensable. Nevertheless, measuring the performance of ICs is not straightforward. Often, the behaviour of the IC-under-test is characterised by placing it on a radio frequency (RF) board and by performing measurements on the board. It was observed that this board often influences the characterisation of the IC. In this paper we focus on efficient analysis and design strategies for reliable RF boards dedicated to integrity monitoring of ICs. The approach presented here is based on an EM/circuit co-design technique. We apply the technique to a canonical test board used for, a.o., conducted susceptibility testing of ICs up to a frequency of 2.5 GHz. This is considered to be a relatively high frequency for conducted susceptibility testing of ICs, having the advantage of incorporating the important 2.45 GHz ISM band. Simulation results illustrate the novel techniques and demonstrate their validity and efficiency for analysis, deembedding, and design purposes.

1 Introduction

Parasitic high-frequency behaviour, leading to power integrity (PI), signal integrity (SI), and electromagnetic compatibility (EMC) problems has been studied for many decades. Especially

at the level of the printed circuit board (PCB), much literature is available, see e.g. [1] and the references therein. With increasing complexity and miniaturisation of microelectronic components on the one hand, and rising frequencies and bitrates on the other hand, there is an increasing demand for efficient EMC, SI, and PI testing of Integrated Circuits (ICs) [2]. The International Electro-technical Commission (IEC) is standardising or has already standardised many IC-level EMC tests, both for conducted and radiated emission (CE and RE) [3], and for conducted and radiated immunity (CI and RI) [4]. The IEC is also in the process of standardising the modelling of the EMC-behaviour of ICs [5]. To measure emission or immunity aspects, the IC is placed onto a test PCB. This PCB typically contains all circuitry necessary for the functional behaviour of the IC, as well as additional provisions for measuring the EMC-behaviour. The effects induced by the PCB itself should be limited in order to properly assess the EMC performance of the IC-under-test, independent of the PCB used as a platform. This requires a very careful design of the PCB, especially when performing high-frequency measurements. At least, the characteristics of the PCB should be known accurately, preferably by means of simulations. This avoids to manufacture multiple prototypes. Additionally, it also allows to deembed these characteristics afterwards. A deembedding procedure is also necessary to conceive measurement based behavioural models of ICs.

In this paper we focus on the analysis and design of test PCBs for the characterisation of ICs. A canonical case study, i.e. a realistic board to characterise the IC's susceptibility to conducted radio frequency (RF) noise, is presented. Recently, several publications discussed the modelling and characterisation of the susceptibility of ICs to RF power injection [6–11]. One procedure to determine the IC's susceptibility is by means of the direct power injection (DPI) test, which is a CI test standardised by the IEC [12]. Accurate knowledge of the amount of RF power that is injected into the pins of the IC-under-test is indispensable for accurate DPI testing and for deembedding the PCB's influence. As frequencies and bitrates do not cease to increase, in this paper we extend the upper frequency limit to 2.5 GHz, as such including the important 2.45 GHz ISM band. Design of test boards up to high frequencies can only be successful if all high-frequency phenomena at the PCB level are taken into account. This can be most accurately achieved by full-wave modelling of the PCB and the interconnects [13, 14] combined with circuit models accounting for all parasitics of the discrete components. For reliable and efficient RF board design or analysis, adopting a co-optimisation/co-design strategy that includes circuit aspects on the one hand and electromagnetic (EM) field effects on the other

hand is imperative. Thereto, in this paper, a dedicated EM/circuit analysis and design strategy is applied to achieve our goals.

In Section 2 a brief summary of the pertinent EM/circuit co-design technique, adopted in this paper, is given. Section 3 starts with a conceptual configuration of a DPI test board, from which a canonical case study is derived. Finally, some concluding remarks are formulated in Section 4.

2 EM/circuit co-design

Consider the design of IC-level EMC test boards at relatively high frequencies (up to 2.5 GHz). These PCBs consist of one or more dielectric layers with planar metallisations and they are populated with lumped passive components (resistors, capacitors, and inductors) and the IC-under-test. Circuit simulators, relying on Kirchhoff's current and/or voltage laws, are powerful design tools, as they are fast, able to deal with active nonlinear components, and easily integrated with advanced optimisation techniques. However, to properly design microwave and RF circuits, all the physical effects of the actual geometry layout need to be taken into account, in particular the high-frequency effects at the level of the board with its printed metallisations. Electromagnetic (EM) solvers, relying on Maxwell's equations, are able to accurately predict and describe all high-frequency phenomena. Unfortunately, these EM solvers are slow and therefore not very suited for optimisation purposes. Hence, integrated solvers, which allow EM/circuit co-optimisation and co-design, are necessary for state-of-the-art high-frequency/high-speed electronic design automation (EDA). The above issues are elaborated in [15] and are summarised in Fig. 1.

Also in [15], an indirect approach to combine EM and circuit simulations is presented. An electromagnetic model database (EMDB) is developed that contains EM simulation results (under the form of S-parameters) of the physical structures, i.e. in our case the PCB with its printed metallisations. The EM/circuit co-design environment, as proposed in [15], has been implemented in the commercially available EDA framework Advanced Design System (ADS) from Agilent Technologies, Santa Rosa, CA, USA. EM/circuit co-optimisation is typically an iterative process and it requires multiple EM simulations. Highly dynamic interpolation schemes are incorporated into ADS, allowing to co-optimise the lumped elements and the metallisation patterns, while only requiring a low number of iterations and full-wave EM simulations. The

goal of this paper is to demonstrate, for the first time, the necessity and efficiency of combined EM/circuit co-optimisation for the analysis and design of reliable EMC test boards. As the EDA tool ADS leads to fast and accurate analyses and optimisations, this tool is further used in Section 3.

3 DPI test board optimisation

3.1 Conceptual configuration of DPI test boards

For a general description of the DPI test setup we refer to the pertinent international standard [12]. Here, we briefly describe the gist of it. In general terms, the goal of the DPI test is to assess the IC's immunity against conducted RF noise. For that purpose, the IC-under-test is placed onto a test PCB. This PCB contains all necessary circuitry such that the IC can function in the same way as it is supposed to in its intended application. Additionally, provisions are made such that some pins of the IC are subjected to RF noise. Thereto, an RF generator delivers RF power to the PCB's RF input ports. These ports are realised using subminiature version A (SMA) connectors. Each SMA is connected to a pin of the IC via a power injection path on the board. Both frequency and strength of the RF power are varied during the test, and meanwhile, the behaviour of the IC is monitored. This is done by connecting monitoring equipment, e.g. an oscilloscope, to pins of the IC. During the test, while sweeping the frequency and power of the RF noise, the correct functionality of the IC must remain intact. Otherwise, the IC fails the DPI test. Every pin of the IC that is suspected to be exposed to RF noise during its intended application should be subjected to the test.

Although we here focus on DPI test boards, it is important to mention that, often, IC-level EMC test boards are conceived as multipurpose (also called combined) test boards, i.e. they are not only used for a single test only, such as DPI (which is a CI test). The combined test boards can also be used for other tests (CE, RI, and RE). E.g., the DPI test board can be combined with an RE test board for the measurement of radiated emission in a TEM-cell [16]. During this TEM-cell test, described in [16], RF noise radiated by the IC is measured by placing the IC in a TEM-cell. The IC should of course be tested whilst functioning properly. Hence again, for this RE test, the IC is placed onto a test PCB and all necessary means, allowing the IC to function as it is supposed to in its intended applications, are also provided. It is recommended to locate *only* the IC-under-test on one side of the board (from now on called the bottom side),

while all other routing and circuitry reside on the other side of the board (from now on called the top side). This setup has as a goal to prevent (RF) currents from flowing on the bottom side of the PCB, as these currents would influence the IC's RE TEM-cell test.

A conceptual configuration of a combined DPI/TEM-cell test PCB is shown in Fig. 2. Although not strictly required in [12] and [16], in our opinion it is advantageous to conceive such IC-level EMC test boards as double-sided PCBs with a grounded co-planar waveguide (GCPW) topology on both sides. As opposed to EMC-unaware designs with a microstrip topology, a maximum amount of copper should be used on both sides. Then both layers approach a continuous ground plane as much as possible and radiation from the PCB is minimised. On the bottom, the reader recognises the IC-under-test, located at the centre of the board. GCPW traces, connected to each pin of the IC, fan out and are connected to the other side of the board by means of vias. On the top side, all lumped components (often Surface Mounted Devices (SMDs)) and the routing of signals and RF currents are located. One notices an SMA connector to feed RF power to a pin of the IC, and some necessary circuitry and lumped components that ensure a proper functioning of the IC, in particular the DC supply. It is also possible to connect monitoring equipment with pins of the IC.

It is clear that care should be taking during measurements: proper grounding of all measurement equipment is essential and all ground current return paths should be well-defined. A detailed explanation on earthing and grounding of measurement setups can be found in [17]. Additionally, in this particular case, the size of the test board should mate with the wall port of the TEM-cell and the periphery of the test board's ground plane should be plated to facilitate contact with this wall port (see [16]). Furthermore, the ground reference planes on both sides should be densely connected by vias. It is advised to have a maximum distance between these vias of $\lambda_{\text{eff}}/20$, where λ_{eff} is the effective wavelength corresponding to the highest frequency of concern [1].

3.2 Canonical case study: schematic and requirements

In this paper we focus on the DPI test performed at two adjacent pins of an IC. One of these pins is the DC feed pin. This particular pin can be expected to be subjected to RF noise in its intended application. For this canonical case study, we suppose that the pin next to the DC supply pin is also expected to be subjected to RF noise. This case study is both illustrative and complex. The approach and results presented below are applicable or can be extended to

many other practical configurations.

Consider the schematic of Fig. 3. The RF power is injected into two adjacent pins of the IC-under-test by means of SMA connectors and current injection paths with DC blocking capacitors C1 and C2. As also mentioned in [12], the blocking capacitors protect the RF signal generator, by avoiding supplying DC to it. As one of these two pins is the IC's DC feed pin, this pin is also connected to the DC supply by means of an RF choke or filter L. This choke L prevents RF current to flow to the DC supply. Monitoring equipment can be connected to both pins. The decoupling networks (here resistors R1 and R2) protect this equipment and make sure that the IC's functionality is not compromised.

As stated in the introduction, it is required that ICs comply with strict EMC norms, and also, that the EMC test setups are reliable. Therefore, it is interesting to mention that, apart from the international standards such as [12], original equipment manufacturers (OEMs) also issue test requirements, e.g. [18]. These requirements are often based on the IEC standards and they have to be followed by the OEM's IC suppliers. In particular for DPI test setup, the transfer characteristics of the power injection paths from the SMAs to the pins of the IC-under-test, are of great interest. The following is stated in [12]: *"To characterise the power injection setup, replace the IC by a proper 50 Ω port and measure the S_{21} parameter from the RF injection port to the pad of the specified IC pin in a 50 Ω system. The S_{21} parameter must have a constant behaviour over the used frequency range without any resonance (see the example ...). A maximum deviation of 3 dB is allowed."* This is correctly interpreted in [7], where it is mentioned that *"the DPI standard requires the characterisation of the injection setup, essentially its transfer gain (S_{21} parameter) when the device under test (DUT) is replaced by a 50 Ω port. The ratio between the power delivered to the load should be 0 dB with a maximum tolerance of 3 dB across the whole frequency range [2]. For the moment most of the proposed injection setups cannot guarantee a total transfer of incident power to the DUT."* At first sight, it might seem counterintuitive to replace the pin of the IC by a 50 Ω load or port, because it is unlikely that the IC's input impedance matches 50 Ω. However, upon knowledge of the real input impedance, this procedure allows to determine the amount of power that is really injected into the pin. Additionally, knowledge of the transfer characteristics allow deembedding of the test board's influence. Preferably, these characteristics are determined by means of accurate simulations, as this avoids to manufacture multiple prototypes.

Taking the above into account, the schematic of Fig. 3 is replaced by the schematic of

Fig. 4. There are four network terminations (i.e. ports with a port impedance of 50 Ω) in this case study. Note that in the RF four-port network the monitors are replaced by open circuits and the DC supply is replaced by a through-connection. It is of course required that during the DPI test, this DC power supply is properly decoupled just before entering the board, as such avoiding that RF currents are picked up by the DC power cords and passed unimpeded to the RF board [17]. To comply with the above statements, we have to design the board such that the transfer characteristics, expressed by means of the S-parameters of this four-port network, satisfy the following requirements in the complete frequency range of interest: $0 \geq |S_{31}| > -3$ dB and $0 \geq |S_{42}| > -3$ dB. Also, of course, the (forward and backward) crosstalk between the two coupling paths, expressed by the S-parameters S_{21}, S_{41}, S_{32}, and S_{43}, should be minimal, say less than -20 dB. Often, one stipulates the above requirements in the frequency band from 150 kHz to 1 GHz. However, OEMs already nowadays require compliance with EMC regulations in a broader band. Therefore, in this paper we extend the range up to 2.5 GHz in order to include the important 2.45 GHz ISM band too.

3.3 Classical DPI test board design and analysis

To design the test board and to analyse the transfer characteristics of the two power injection paths, we apply the EM/circuit co-design technique integrated in ADS, as described in Section 2. Figs. 5(a) and 5(b) show the PCB's metallisations on the top and bottom side respectively. The vias and through-holes are visible on both figures. The positions of the DC supply connector, the two SMAs (consisting of one signal and four ground vias), the output pins for the monitoring equipment and the position of the two adjacent pins of the IC-under-test are indicated. Also, the positions of the four network ports are shown, as well as the symbols corresponding to the lumped components C1, C2, R1, R2, and L. Consistent with the conceptual design as described in Section 3.1, only the IC is placed on the bottom side. Hence, two vias are present in the two RF power injection paths.

To come up with this initial design, we use classical design rules and also follow recommendations provided by, a.o., the OEMs [18]. The following rules and guidelines are applied:

- The layout of Fig. 5 is made on a standard double-sided FR-4 board with a thickness of 1.6 mm, a relative permittivity $\epsilon_r = 4.35$, and a loss tangent $\tan\delta = 0.01$.
- With the above board characteristics, the GCPW signal trace width equals 1.5 mm and

the gap width, i.e. the width of the void between the signal trace and the reference planes, equals 250 μm in order to have a characteristic impedance of 50 Ω at 2.5 GHz. For these design parameters the effective permittivity $\epsilon_{\text{eff}} = 2.78$ and the effective wavelength $\lambda_{\text{eff}} = 71.9$ mm at 2.5 GHz.

- A grid of ground vias between top and the bottom side spaced D = $\lambda_{\text{eff}}/20$ apart would lead to a very dense grid with a maximum distance of D = 3.6 mm between two vias. This grid is too dense to be of practical use. In our setup (see Fig. 5) D equals 10 mm.

- As this distance D is larger than what is required by the $\lambda_{\text{eff}}/20$-rule, two extra ground vias are strategically located next to the signal vias in the power injection path. These extra ground vias provide an adequate (RF) current return path, required for a good flux cancellation [1]. A detailed study of this effect, as presented in [14], is not repeated here. However, it is important to mention that without these two extra vias, a resonance can be introduced, corrupting the DPI test. Such resonances can only be predicted by full-wave simulations, as presented in [14] and also in this paper.

- To reduce crosstalk between two RF power injection paths, viz. to reduce coupling between the traces, there should be a certain spacing between them. For a microstrip topology it is often advised to apply the so-called "3-W rule" [1], meaning that there should be a distance of 2W between two microstrips that have a trace width W. In our GCPW topology the total width of the traces is given by W = 1.5 mm + 2 $\cdot$ 0.250 mm = 2 mm. Hence, we have kept a distance of w = 6 mm between the centres of the signal traces. At the bottom side, the GCPW traces practically touch each other. However, the length of the RF power injection paths on the bottom side is less than $\lambda_{\text{eff}}/20$ and therefore it can be expected that they do not influence the transfer characteristics much. A full-wave analysis will be performed to be absolutely sure (see further).

- The decoupling between the DC supply and the RF power injection path is an important issue. One might be tempted to use a filter in Pi- or T-topology. Although these kinds of filters do protect the DC supply, in our opinion it is not a good idea to use them. The reason for this is clear. The shunt elements (capacitors) in these filters will cause RF currents to flow to ground, as such protecting the DC supply, but also limiting the amount of power that is injected into the pin of the IC. Hence, such filters will lead to a

high insertion loss along the power injection path, and even worse, at certain frequencies the filter can resonate, causing insertion loss suck-outs. Therefore, here we will use a simple bias tee, as such following the recommendation by OEMs [18]. To choke the RF currents, a simple 5 μH coils is recommended. In our initial design we use a 5 μH axial inductor with an equivalent series resistance (ESR) of 34 mΩ and a self-resonant frequency (SRF) of 87 MHz (EPCOS B82133A5402M000). The DC blocking capacitors C1 and C2 have a value of 6.8 nF. These capacitors are both SMDs and have an equivalent series inductance (ESL) of 1 nH and an ESR of 200 mΩ (e.g. AVX X7R 08055C682MAT2A). It is mentioned in [7] that it is hard to achieve a broadband decoupling by using a simple bias tee, and therefore, an innovative 'Gallenne' injection setup was proposed, which performs excellent in the band from 1 MHz – 1.5 GHz. Here, we opt to reevaluate the simple bias tee as recommended by the OEMs.

- To provide a sufficient decoupling between the IC and the monitoring equipment, in our design the resistors R1 and R2 have a value of 10 kΩ. Both components are SMDs.

- Notice that the DC supply path, with length Δ, can be seen as a loaded stub placed in parallel to the RF power injection path (Figs. 4 and 5). The stub length Δ should be chosen carefully, as stubs typically might cause resonances. Therefore, this issue is treated in detail in the following subsection.

3.3.1 Investigation of the resonance caused by the DC supply path

Consider the DC supply path. Via a series load, i.e. the RF choke L, a shorted stub with length Δ is placed in parallel to the RF power injection path (Fig. 5(a)). We opt to make the stub quite short, e.q. $\Delta = 10$ mm, and hence, by itself it would not cause a resonance (because $\Delta < \lambda_{\text{eff}}/4$). However, we have to consider the combination of the series load L together with the shorted stub. Using classical transmission line theory, this combination can be replaced by an equivalent shunt impedance Z_S in the RF power injection path, where

$$Z_S = Z_L + jZ_0 \tan \beta\Delta, \tag{1}$$

with $Z_0 = 50\ \Omega$ the characteristic impedance, Δ the length of the stub, $\beta = 2\pi/\lambda_{\text{eff}}$ the wavenumber, and Z_L the impedance of the RF choke L. Making the following simplification for

the impedance Z_L as a function of the frequency f,

$$Z_L = \frac{j2\pi f\mathrm{L}}{1-(f/\mathrm{SRF})^2}, \tag{2}$$

where SRF is the self-resonant frequency of the inductor, it is readily seen that a resonance in $|S_{31}|$ occurs when the equivalent shunt impedance $Z_S = 0$, i.e. when

$$G(f) = \tan\beta\Delta, \tag{3}$$

with

$$G(f) = \frac{2\pi f\mathrm{L}}{Z_0\left((f/\mathrm{SRF})^2-1\right)}. \tag{4}$$

Since $\beta = 2\pi/\lambda_{\mathrm{eff}} = 2\pi f\sqrt{\epsilon_{\mathrm{eff}}}/c$, with c the speed of light in free space, (3) is a transcendental equation. Using the above defined values, L = 5 μH, SRF = 87 MHz, Δ = 10 mm, and assuming that $\epsilon_{\mathrm{eff}} = 2.78$ does not vary with frequency, the solution of (3) can be represented graphically (see Fig. 6). The intersection between $G(f)$ and $\tan\beta\Delta$ is found at $f_{\mathrm{res1}} = 2.920$ GHz. By further assuming that $\beta\Delta$ is small, such that $\tan\beta\Delta \approx \beta\Delta$, the solution of (3) is given by

$$f_{\mathrm{res2}} = \mathrm{SRF}\sqrt{1+\frac{c\mathrm{L}}{Z_0\Delta\sqrt{\epsilon_{\mathrm{eff}}}}} = 3.690 \text{ GHz}. \tag{5}$$

This second approximation f_{res2} is also indicated in Fig. 6. So, based on this classical transmission line approach, the choice Δ = 10 mm would not cause any resonance in the frequency range of interest (150 kHz – 2.5 GHz).

3.3.2 Combined EM/circuit analysis of the classical DPI test board design

Let us now carefully analyse this design using combined EM/circuit simulations by concentrating on its pertinent characteristics (S-parameters). The reflection at the two input ports (the two SMAs), the transfer characteristic along the two RF power injection paths and the backward and forward crosstalk characteristics are presented in Figs. 7(a), 7(b), and 7(c) respectively. The following can be concluded:

1. At 1.970 GHz a sharp resonance occurs in one of the power injection paths (see Fig. 7(b)). It becomes clear that the classic transmission line model of Section 3.3.1 leads to an inaccurate estimate of this resonance. Predicting the effect of the stub by merely using this

transmission line models leads to erroneous conclusions, e.g. in our classical RF design the resonance would occur outside the frequency range of interest. So, although this stub is already quite short, i.e. 10 mm, it is still not sufficiently short. This transmission line model does however provide some insight into the physical high-frequency phenomena occurring at the PCB-level. Indeed, by observing (3) or Fig. (6) it is readily seen that lowering Δ will lead to a higher value of f_{res}, viz. the resonance shifts towards higher frequencies. A simple, fast, and — most importantly — accurate way to determine an optimal value for Δ is demonstrated below. By means of the EM/circuit co-design technique, all RF effects of the board will be taken into account, as well as the value of the choke L, and its parasitic effects (which also play an important role).

2. For the RF power injection path between ports 2 and 4, the value of the DC blocking capacitor C2, i.e. 6.8 nF, is too low. Hence, at low frequencies the impedance of this component is too high, e.g. 156 Ω at 150 kHz. Indeed, the reflection $|S_{22}|$ is large at low frequencies (see Fig. 7(a)). For frequencies lower than 235 kHz, less than half of the RF power reaches the pin of the IC, i.e. $|S_{42}| <$ -3 dB, and in particular at 150 kHz, $|S_{42}|$ = -5.4 dB (see Fig. 7(b)). So, a larger capacitor will have to be used. The same conclusion can be drawn for the DC blocking capacitor C1: its value is also too low as well. However, the reflection $|S_{11}|$ is even higher than $|S_{22}|$ and the power transfer is lower ($|S_{31} < |S_{42}|$), see Figs. 7(a) and 7(b). For frequencies lower than 754 kHz, less than half of the RF power reaches the pin of the IC, i.e. $|S_{31}| <$ -3 dB, and in particular at 150 kHz, $|S_{31}|$ = -24.6 dB. This is not only due to the DC blocking capacitor C1, but also because of the RF choke L. Its value is too low. At a frequency of 150 kHz it provides an impedance of only 4.7 Ω. So, a larger inductance will have to be used. It was already clear that full-wave simulations are necessary to improve the DC stub (see higher), we can also benefit from the EM/circuit approach to efficiently obtain better values for L, C1, and C2. Indeed, this technique yields optimal values very rapidly and with minimal effort, taking into account all parasitics of the lumped components. Classical circuit analysis techniques are quite elaborate.

3. From Fig. 7(c) it can be concluded that there is very little crosstalk between the two power injection paths. The values of the pertinent S-parameters are below -23.5 dB over the whole frequency range from 150 kHz to 2.5 GHz. This is most probably due to the

fact that the power injection paths are very short. So, in this initial design, the width w between the paths, chosen in compliance with the classical 3-W layout rule, is actually larger than strictly required. When testing large ICs with many pins, one typically wants to decrease the area occupied by each power injection path. Therefore, below, we will reduce the parameter w while still maintaining an acceptably low crosstalk. This will be investigated by means of the EM/circuit co-optimisation technique.

3.4 Improved test board design and analysis by means of EM/circuit co-optimisation

In this last section the initial design as discussed above will be optimised over the complete bandwidth 150 kHz – 2.5 GHz. First, the lumped components C1, C2, and L, which cause the bad transfer characteristic at low frequencies, are dealt with. Second, the resonance peak in S_{31} will be investigated and removed from the frequency range of interest by adjusting the stub length Δ. Third, to reduce the area occupied by the power injection paths, the spacing between the GCPWs will be lowered, meanwhile monitoring the crosstalk. All optimisation steps are performed using a standard desktop with an INTEL(R) CORE(TM)2 Quad Q6700 CPU @ 2.67 GHz, with 8 GB of RAM, and running a 64-bit version of Windows Vista.

Starting from our initial design we now demand that $|S_{31}| >$ -3 dB and $|S_{42}| >$ -3 dB at 150 kHz and by using the gradient-based optimisation routine of ADS-Momentum, we look for optimal values of C1, C2, and L. (At this point we only optimise the nominal values and do not take the parasitic effects into account, as these have little influence at 150 kHz). In only 7 iterations — each iteration taking approximately 0.12 seconds — we obtain the following optimal nominal values for the capacitors and the inductor: C1 = 16.5 nF, C2 = 10.7 nF, and L = 34.6 μH. In our design, obviously, we have to use commercially available lumped components and we select components with a value close to the optimal nominal values, as follows. The two DC-blocking capacitors C1 and C2 are SMDs with a capacitance of 22 nF, an ESR of 100 mΩ, and an ESL of 1.5 nH (AVX Z5U 08055E223MAT2A). L is an axial RF choke with an inductance of 47 μH, an ESR of 1.5 Ω and a SRF of 32 MHz (Ferroperm Type 1583 RF choke). As their nominal values are higher than what is strictly required, these components lead to even better transfer characteristic at low frequencies, i.e. $|S_{31}|$ = -1.3 dB and $|S_{42}|$ = -0.9 dB at 150 kHz. Still, the sharp resonance peak in $|S_{31}|$ remains present in the band, albeit at a slightly different frequency, namely $f_{\text{res}} = 2.093$ GHz.

Therefore, second, we demand that $|S_{31}|$ > -3 dB at 2.5 GHz and again we use the gradient-based optimisation tool of ADS-Momentum. As a range for optimisation we let Δ vary between 10 mm and 1 mm. ADS optimises the design in one iteration, which takes 33 seconds. During this iteration three additional Momentum-RF EM simulations are required. For these Momentum-RF simulations, multi-threading (4 threads) is applied and the direct (dense) matrix solver is used. The mesh generation (discretisation) leads to ca. 7000 unknown edge currents. Each EM simulation takes on average 164 seconds, mesh generation included. Thus, the total elapsed time for this optimisation is 8 minutes and 45 seconds and the following value is obtained: $\Delta = 3.714$ mm, whereas the original value was $\Delta = 10$ mm.

Third, we reduce the value of the width w between the GCPWs on the top side to a minimal value, using again the optimisation tool of ADS-Momentum, and demanding that the insertion loss along the two power injection path remains lower than 3 dB and the crosstalk is smaller than -20 dB. During one iteration and two additional Momentum-RF EM simulations, in a total simulation time of 5 minutes and 57 seconds, it is found that w can be lowered to a value of w = 2.140 mm. This drastic reduction in spacing between the lines is possible because the lines are quite short.

Finally, we present the pertinent characteristics (S-parameters) of the optimised design (Fig. 8). The following can be concluded:

1. Compared to the initial design of Section 3.3, the reflection (Fig. 8(a)) at both SMAs has decreased.

2. Correspondingly, the RF power transfer along the injection paths complies with the requirements, i.e. $|S_{31}|$ > -3 dB and $|S_{42}|$ > -3 dB (Fig. 8(b)) in the complete frequency range from 150 kHz to 2.5 GHz.

3. From Fig. 8(c) it is concluded that there is still a negligible crosstalk between the two power injection paths.

These resulting S-parameters guarantee a reliable test setup. Additionally, these S-parameters can immediately be used for deembedding the board from the actual measurements of the IC. This step is necessary to conceive behavioural immunity models for the IC. Such approaches have been demonstrated in literature in order to conceive emission models, e.g. [19].

4 Conclusions

In this paper it has been demonstrated that EM/circuit co-design techniques are very useful tools to efficiently analyse and design reliable test boards for the characterisation of the EMC behaviour of ICs. The EM/circuit co-design technique is briefly presented and after the description of a conceptual configuration of DPI test boards, a canonical case study is derived. For this case, the RF power injection paths are analysed and optimised over a large frequency range from 150 kHz up to 2.5 GHz (as such including the important 2.45 GHz ISM band). A first design, following, a.o., some recommendations provided by OEMs and classical RF board design techniques based on transmission line equivalent models, leads to the conclusion that this first design is suboptimal. Using EM/circuit co-optimisation technique allows to derive the optimal values for the lumped components and metallisation patterns on the printed circuit board, leading to a reliable test board. The test boards are analysed by means of their pertinent simulated S-parameters. Apart from avoiding to manufacture multiple prototypes, the resulting S-parameters also allow a rapid deembedding of the RF board from the actual measurements.

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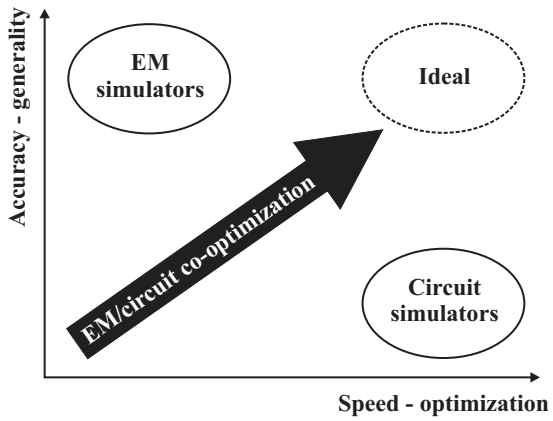


Figure 1: Schematic representation of the necessity of EM/circuit co-design

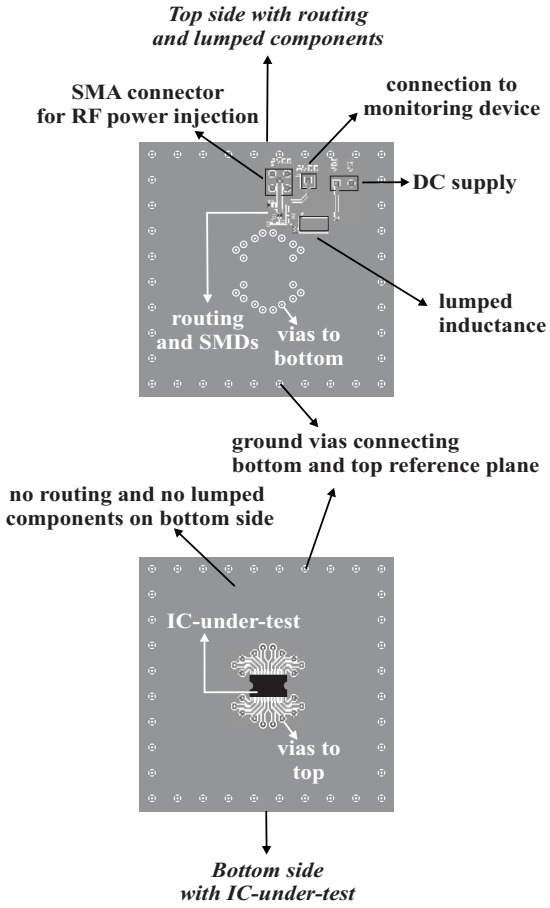


Figure 2: Conceptual configuration of a combined DPI/TEM-cell test board

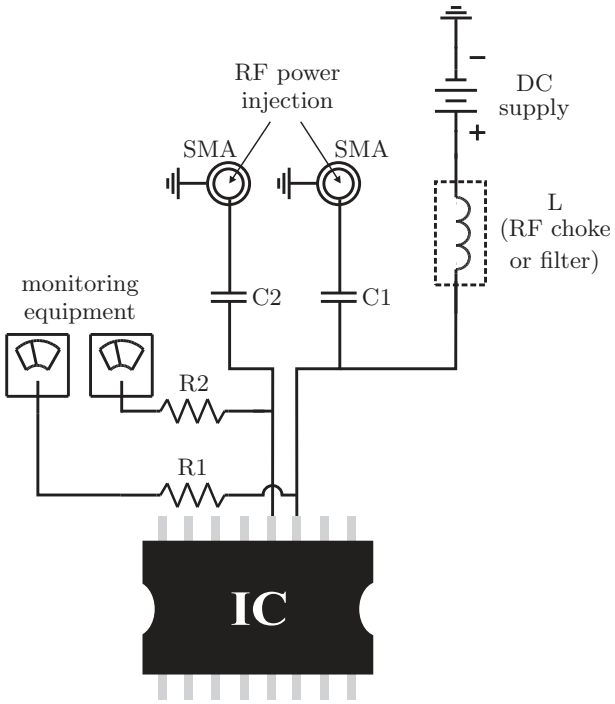


Figure 3: Schematic of the DPI test setup for two adjacent pins. It is clear that this is merely a conceptual representation of (a part of) the test setup.

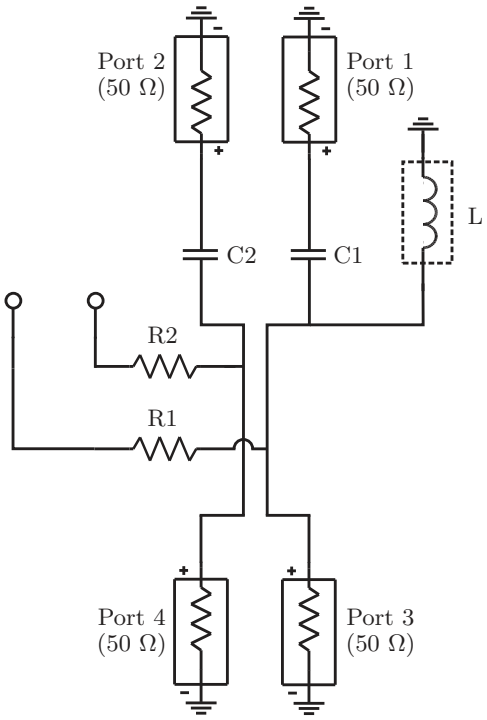
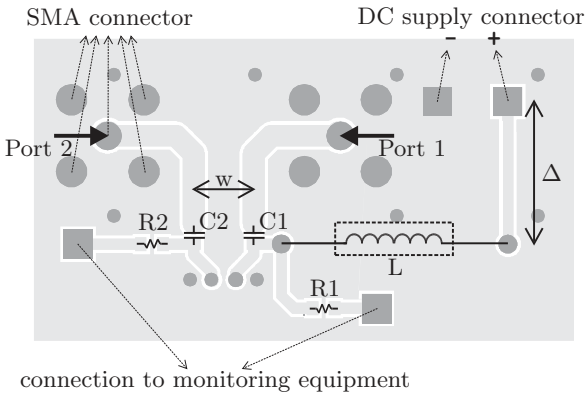
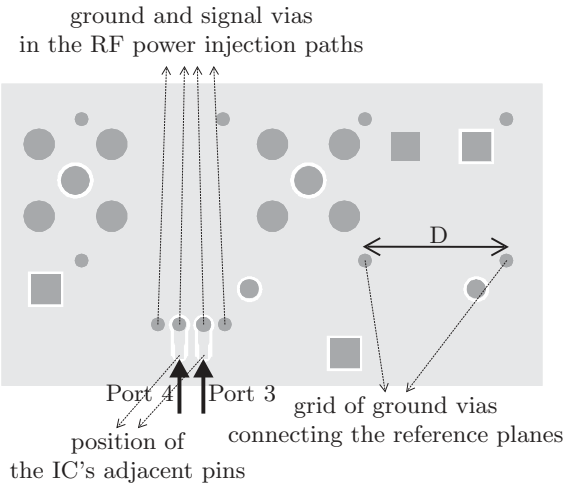


Figure 4: Four-port network corresponding to the schematic of Fig. 3 in order to design and analyse the transfer characteristics of the power injection paths



(a) Top side



(b) Bottom side

Figure 5: Design of the test board (light gray: metallisation; dark gray: via; white: void; dimensions: 38.1 mm × 21.3 mm)

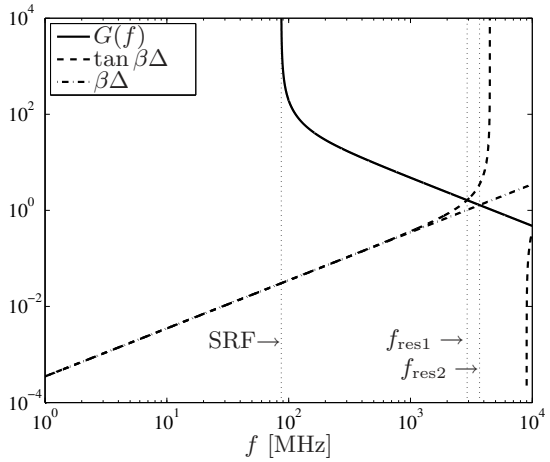
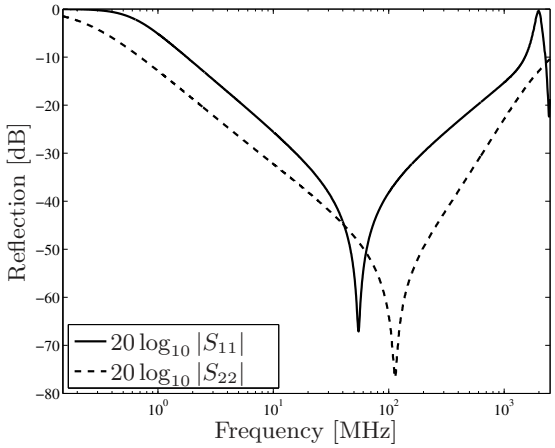
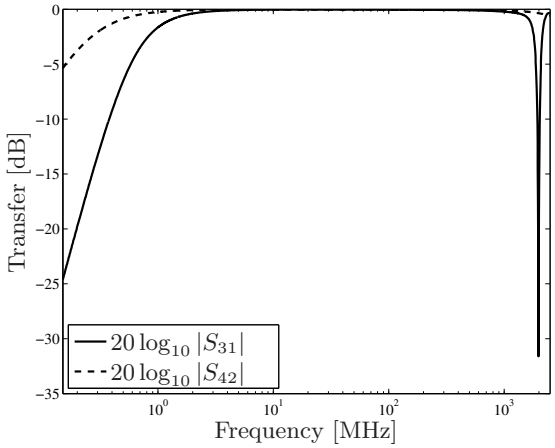


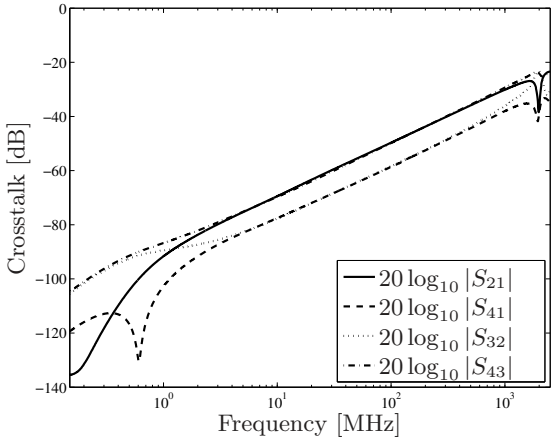
Figure 6: Graphical representation of the transcendental equation (3). Due to the logarithmic scale, the negative parts of $G(f)$ (for $f < \mathrm{SRF}$) and $\tan\beta\Delta$ (for $\pi/2 < \beta\Delta < \pi$) are not visible.



(a) Reflection at the SMAs

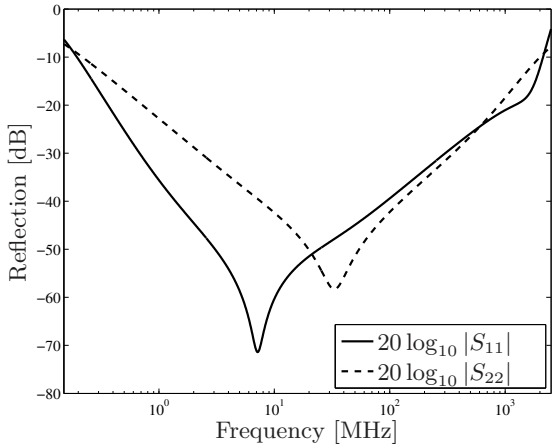


(b) Transfer characteristics along the two RF power injection paths

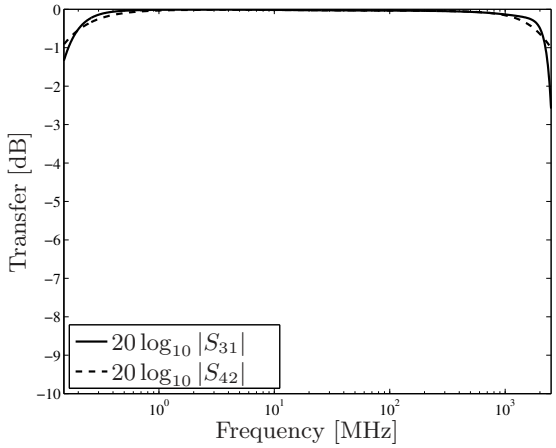


(c) Forward and backward crosstalk characteristics between the two RF power injection paths

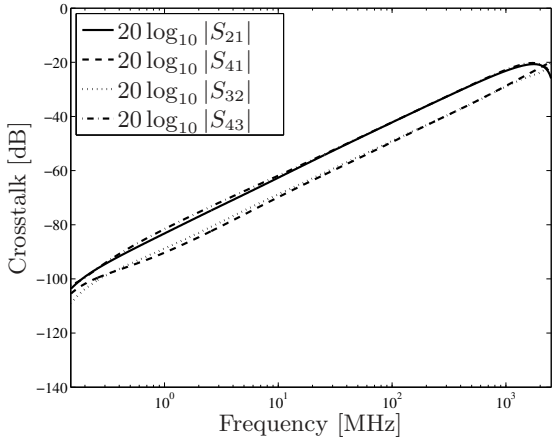
Figure 7: S-parameter characteristics of the initial design



(a) Reflection at the SMAs



(b) Transfer characteristics along the two RF power injection paths



(c) Forward and backward crosstalk characteristics between the two RF power injection paths

Figure 8: S-parameter characteristics of the optimised design