Efficient and Accurate Testing of Analog-to-Digital Converters Using Oscillation-Test Method

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Abstract

This paper describes a practical test approach for analog-to-digital converters (ADCs) based on the oscillation-test strategy. The oscillation-test is applied to convert the ADC under test to an oscillator. The oscillation frequencies are able to monitor the ADC conversion rate, differential nonlinearity (DNL) and integral nonlinearity (INL) at each quantization band edge (QBE). Using this method, no analog stimulus should be supplied and therefore the need for a costly precision signal generator is eliminated. Besides, as the oscillation frequency is evaluated using pure digital circuitry, test accuracy is increased. This test approach is not limited to a special kind of ADC. Simulations and practical implementation prove the efficiency of the proposed test approach for ADCs.

1 Introduction

Analog-to-digital converters (ADCs) are the most frequently encountered mixed-signal circuits. ADCs are precision products and their test requires reference circuits with at least two more bits of resolution than the circuit under test (CUT). Implementation of these reference circuits results in significant area overhead, which calls into question the practicality and reliability of on-chip methods for ADC testing. Many methods for the on-chip testing of ADCs have been presented in the literature. The digital-to-analog converter (DAC) testing approach has been mapped to test ADCs which use a DAC in their architecture [1]. The built-in self-test (BIST) approach presented in [2] requires that both DAC and ADC be available on the same chip and uses an off-chip DAC and external logic testing equipment. Conventional test techniques have been applied to embedded ADCs using microcontroller resources available on the same chip [3]-[5]. A digital BIST for a signal-to-noise-ratio test of an over-sampled ADC, based on an available DSP core, has also been presented [6]. Each of the above-mentioned BIST approaches is applicable to either a specific ADC type or a specific application, which for example, guarantees the existence of extensive on-chip computational ability.

This paper describes a new test approach, based on the oscillation-test strategy [7],[8], for all types of ADCs. This test technique is suitable for both on-chip and off-chip testing situations.

The paper is organized as follows: Section 2 describes ADC error definitions. The proposed test structure is introduced in section 3. Section 4 presents ADC conversion-time, DNL and INL testing procedures. The practical implementation and some results are presented in section 5.

2 ADC Error Definition

Fig. 1 depicts the probability of the codes C_i and C_{i+1}, corresponding to the quantization intervals Q_i and Q_{i+1} below and above a threshold level V_{Ti+1}, for an ideal and a real ADC in a simplified fashion. Threshold voltage V_{Ti+1} is defined as the point where C_i and C_{i+1} exhibit the same probability of 0.5. In Fig. 1, $V^A_{Ti+1}(V^N_{Ti+1})$ represents the actual (nominal) value of the threshold voltage between codes i and $i+1$, $Q^A_i(Q^N)$ and $Q^A_{i+1}(Q^N)$ are the actual (nominal) quantization intervals below and above a threshold voltage $V^A_{Ti+1}(V^N_{Ti+1})$.

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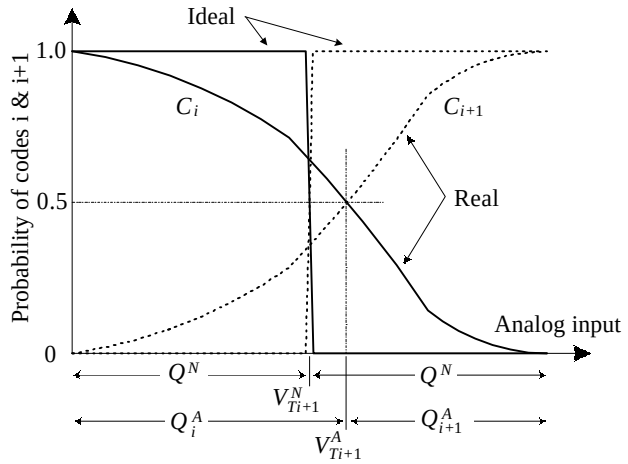

Fig. 1: Quantization band edge (QBE) behavior of ideal and real ADCs. Nominal values are related to ideal ADCs and actual values are related to real ADCs.

As shown for a real ADC in Fig. 1, the V^A_{Ti+1} is displaced from its nominal value, V^N_{Ti+1}, due to the existence of error in a real ADC.

To obtain the ideal characteristics of an ADC, the nominal values of the threshold voltage and quantization band must be found for each input code yielding the theoretical staircase shape as a reference. Deviation of the threshold levels from their theoretical values causes different sizes of quantization intervals, and this is called differential nonlinearity (DNL). The accumulation effect of DNL errors changes the slope of the staircase over the full range, which is characterized by gain error (G_{FSE}) and integral nonlinearity (INL) error.

DNL is defined in terms of the ideal least-significant-bit (LSB) value of the data converter

$$\varepsilon_{i,i-1} = \frac{Q^A_i - Q^N}{Q^N} \quad (1)$$

in which Q^N is equal to 1 LSB. INL error can be calculated by accumulating the various different DNLs

$$\varepsilon_i = \sum_{j=1}^{i} \varepsilon_{i,i-1} \quad (2)$$

INL error at transition level can be measured directly using the following relationship:

$$\varepsilon_i = V^A_{Ti} - V^N_{Ti} \quad (3)$$

where

$$V^N_{Ti} = (i - ½)\text{LSB} \quad (4)$$

Conversion-time is also an important parameter for data converters, especially in applications where high-speed operation is sought. It is defined as the time required for an ADC to perform a complete conversion. It should be noted that conversion-time is not necessarily the inverse of the maximum word rate of an ADC, for example in pipeline ADCs.

3 Proposed Test Structure

The heart of the test structure for ADCs is a feedback loop which forces the ADC under test to oscillate around a predetermined code or codes. The oscillation frequencies of the two least significant bits of the ADC under test correspond to important parameters of the ADC, such as conversion-time and DNL, as will be explained later in this paper. Fig. 2 illustrates the block diagram of the test structure which is based on a feedback approach. This test structure considers the ADC under test as a black box, and therefore can be applied to any type of ADC. The device must be operated in the free-running mode by establishing a proper connection between the *End of conversion* output and *Start conversion* input. In other words, the ADC is assumed to be contiguously converting its input voltage. However, to ensure start-up under all possible conditions, a *Start conversion* pulse is required at the beginning of the test procedure. Fig. 3 illustrates the oscillation of the ADC under test around two predetermined codes, C_j and C_k ($C_k > C_j$). All operations are directed by a control logic (CL) which continuously verifies the actual output code C_x of the ADC. If $C_x = C_j$, the input of the integrator is switched to a current I_2 and the input voltage of the ADC under test V_{IN} increases until the control logic detects $C_x = C_k$, whereupon the switch is changed to position I_1 ramping down the ADC input voltage. The switch S passes the current I_1 until the ADC reproduces code C_j, and the procedure is repeated. Neglecting the operation delay of the control logic, the period of oscillation is given by

$$T = \frac{(V^A_{Tk} - V^A_{Tj+1})C}{I_2} + \frac{(V^A_{Tk} - V^A_{Tj+1})C}{I_1} + 4t_C \quad (5)$$

where t_C is the conversion-time of the ADC under test. Considering $I = I_1 = I_2$, the oscillation frequency is

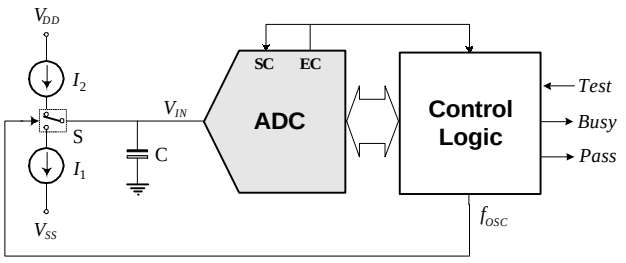

Fig. 2: ADC test configuration (*SC*: Start conversion, *EC*: End of conversion).

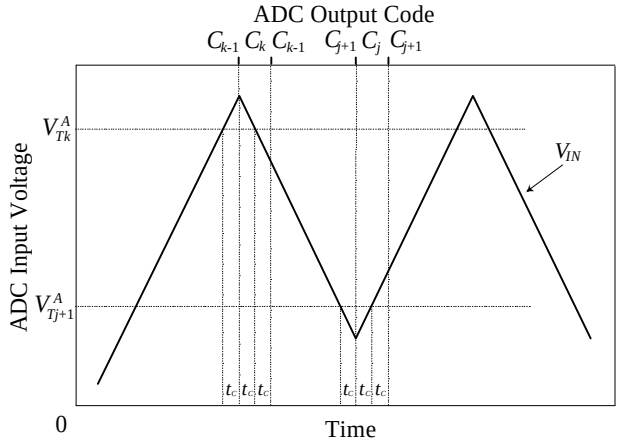

Fig. 3: ADC input voltage oscillation between V_{Tk} and V_{Tj+1} transition thresholds.

$$f_{osc} = 1\Big/\left(\frac{2(V^A_{Tk} - V^A_{Tj+1})C}{I} + 4t_C\right) \qquad (6)$$

It is necessary to note that in the special condition $k = j+1$, the proposed test structure approaches a classic test technique called the servo-loop method [9]. The servo-loop method, which is well known for its high degree of accuracy, is used to detect the ADC transition voltages. The main difference between the servo-loop method and our test technique in this special condition is the following. In the servo-loop technique, the detected transition voltage is filtered to eliminate the oscillations around the transition voltage and is then compared with a reference voltage produced by a DAC having at least two more bits of resolution. Sometimes the transition voltage obtained is directly converted to digital, using a much more accurate reference ADC, and the ADCs' output codes are compared for each transition voltage [10]. The conventional servo-loop method therefore requires a filter and an accurate reference DAC or ADC which cannot be provided in BIST solutions. In our test technique, the objective is not to directly measure the transition voltages. In fact, we only evaluate the oscillation frequency and deduct the important ADC parameters. Therefore, no reference DAC or ADC is necessary and practical on-chip implementation is possible. Furthermore, our technique is more comprehensive and is used to measure a wide range of ADC characteristics.

4 ADC Testing

In this section, the details of measuring different characteristics of the ADC under test by observing an oscillation frequency are given. A real 8-bit successive approximation and flash ADCs have been used to validate the proposed test methodology. A 3-bit full flash ADC has been also designed using the 0.8 μm BiCMOS technology parameters of Northern Telecom Electronics to investigate the fault detection ability and verify the various different test phases proposed.

A. Conversion-Time Testing

The test set-up shown in Fig. 4 can be used for determining the conversion-time t_C of the ADC under test for each possible output code. To measure the conversion-time of a given output code, i.e. C_k, the ADC input is locked to V^A_{Tk} using the feedback loop which forces the ADC output to oscillate between C_k and C_{k-1}. The control logic selects the current I_2, which results in increasing V_{IN}, and compares the output of the ADC with the predetermined code C_k,. When V_{IN} reaches the V^A_{Tk}, after the ADC conversion-time t_C within which the V_{IN} continues increasing, the output code of the ADC will change to C_k, and consequently the current I_1 is selected and the current I_2, is disabled to ramp down the V_{IN}. As I_1 is supposed to be equal to I_2 it also takes t_C for V_{IN} to equal V^A_{Tk} and another t_C to change the output of the ADC to C_{k-1}. By detecting the C_{k-1}, the control logic changes the switch position to select the current I_2 and disable I_1. This process is repeated to oscillate the V_{IN} around V^A_{Tk}, and ADC output code between C_k and C_{k-1}.

From Fig. 4 the f_{OSC} is found to be

$$f_{osc} = \frac{1}{4t_C} \tag{7}$$

which is a special condition of equation (6) where the two different transition voltages are similar. The ADC conversion-time is therefore given by

$$t_C = \frac{1}{4f_{osc}} \tag{8}$$

The oscillation frequency is converted to a digital number and compared with a reference number to evaluate the conversion-time. It is obvious that f_{OSC} does not depend on the capacitor C and current values I, but they must be chosen to keep V_{IN} between V_{Tk-1}^A and V_{Tk+1}^A or $It_C/C < \text{LSB}$. In other words, the pick to pick amplitude of oscillation V_{IN} must be smaller than 2 LSB. The inferior amplitude limit of V_{IN} is determined by the equivalent RMS input noise of the ADC under test.

Measuring the conversion-time at major transition codes is normally sufficient for testing this dynamic parameter.

We have measured the conversion-time of two real ADCs (successive approximation and flash) in practice. The results (55 μs and 1.6 μs) agree with the values reported on the data sheets.

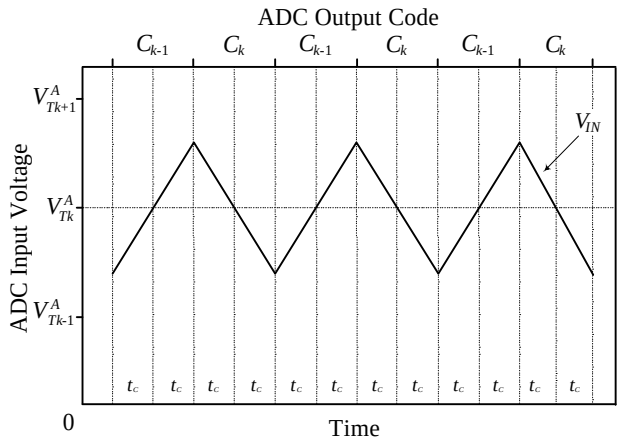

Fig. 4: ADC input voltage oscillation in the vicinity of V_{Tk} to measure the ADC conversion-time t_C.

B. DNL Testing

In order to measure DNL at a specified code C_k, using the test configuration in Fig. 2, the ADC output must be forced to oscillate between C_k and C_{k-2}. Consequently, V_{IN} oscillates between V_{Tk}^A and V_{Tk-1}^A. Using equation (6), the oscillation frequency is described by

$$f_{osc} = 1\Big/\left(\frac{2(V^A{}_{Tk} - V^A{}_{Tk-1})C}{I} + 4t_C\right) \tag{9}$$

$$Q_k^A = V^A{}_{Tk} - V^A{}_{Tk-1} = \frac{I}{2C}\left(\frac{1}{f_{osc}} - 4t_C\right) \tag{10}$$

in which the term $4t_C$ has already been measured during conversion-time testing. The oscillation frequency is converted to a number using FNC and is then compared with a predetermined number which represents the nominal value of the oscillation frequency. This technique has been applied to the successive-approximation ADC to obtain an error plot for DNL data. The obtained frequency for each code was subtracted from a reference frequency and divided by the same frequency to obtain the DNL error. Note that the reference frequency represents 1 LSB. Fig. 5 shows a sample of simulations carried out to test the DNL error of the 3-bit ADC.

C. INL and Gain Error Testing

INL error can be calculated by accumulating DNL errors, as defined in equation (2). At a specific code C_k, the control logic measures the DNL error and then adds this DNL error (respecting its sign) to the previous INL error, calculated for C_{k-1}, to obtain the INL error for C_k. The INL error for the most significant code C_k = (11 ... 1) is called gain error.

The INL at a given code C_k can be evaluated directly by forcing the ADC input to oscillate between C_0 (00 ... 0) and C_{k+1}. Consequently, V_{IN} oscillates between V_1^A and V_{Tk+1}^A. Using equation (6), the oscillation frequency is found to be

$$f_{osc} = 1\Big/\left(\frac{2(V^A{}_{Tk+1} - V^A{}_1)C}{I} + 4t_C\right) \tag{11}$$

$$\varepsilon_k = (V^A{}_{Tk+1} - V^A{}_1) - (V^N{}_{Tk+1} - V^N{}_1) \tag{12}$$

using equation (4) $V^N{}_{Tk+1} - V^N{}_1 = k \times \text{LSB}$.

Therefore, the oscillation frequency represents the actual value of k LSB that is the ideal input voltage of the output code C_k. The INL error can thus be

evaluated by comparing this oscillation frequency with its nominal frequency value, which represents k LSB. As INL data can be obtained from DNL data and vice versa, they can be considered as redundant data. In general, if DNL is tested for all possible output codes, testing INL at some critical point is sufficient to characterize the ADC under test [1].

Conclusion

A new test technique for complete and accurate testing of ADC has been proposed. This test method is capable of measuring DNL, INL and conversion-time of the ADC under test without applying a test stimulus. As no voltage or current measurement is necessary, the performance degradation problem and the need for a high precision DAC or ADC are eliminated. As a digital-output test method, it can be easily integrated with the test methods dedicated to the digital part of the chip under test. The validity of the proposed test technique has been verified through extensive simulations and practical discrete realization. The oscillation-test can be also applied to structural testing of ADCs to speed up the test process for the applications where very small test-time is required.

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For the Fig. 5, please refer to the hard copy of our paper.

Fig. 5: The oscillation of V_{IN} between V_{Tk-1}= 1.79 V and V_{Tk}= 2.51 V to test the DNL error for a 3-bit flash ADC without fault. The ADC's output oscillates between (010) and (100).