Efficient Dual-Band Rectifier Using Stepped Impedance Stub Matching Network for Wireless Energy Harvesting

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Efficient Dual-band Rectifier Using Stepped Impedance Stub Matching Network for Wireless Energy Harvesting

Shun Li, Fei Cheng, Chao Gu, Sha Yu, and Kama Huang, *Senior Member, IEEE*

Abstract—**This letter presents an efficient dual-band rectifier using stepped impedance stub matching circuit. Theoretical analysis of the dual-band impedance matching circuit comprised of a stepped impedance stub is carried out which plays a key role in designing the resultant dual-band rectifier. The proposed dual-band matching circuit can achieve wide frequency ratio which is analyzed and predicted by simulation. For demonstration, a dual-band rectifier working at 0.915 and 2.45 GHz is fabricated with dimensions of 21.47 mm × 18.93 mm. The measured results show that with a 1500 Ω load, the maximum efficiencies of the rectifier reach 74% and 73% at 0.915 and 2.45 GHz, respectively. Due to the simple but efficient structure of the dual-band matching network, the dual-band rectifier in this work exhibits merits of compact size and high efficiency.**

Index Terms—**Wireless energy harvesting, dual-band, high efficiency, rectifier, impedance matching, stepped impedance stub.**

I. INTRODUCTION

The wireless energy harvesting technology (WEH) is a promising technology which can power some low power electrical systems including the wireless communication systems and wireless sensor networks without wires [1]-[4]. WEH aims to collect wasted energy from the ambient environment, so it is a promising solution of reducing pollution when employed in battery less low-power sensors. The microwave rectifier is a key component in a wireless energy harvesting system because the conversion from the received microwave power to the usable DC supply is directly affected by the rectifier. In the past years, many single band rectifiers have been proposed for WEH applications [5]-[7]. Compared with a single band rectifier, broadband [8]-[11], dual-band [12]-[22] and multi-band rectifiers [23]-[26] can harvest microwave energy in more bands thus producing more DC energy. Consequently, broad/multi-band rectifiers have attracted growing attentions in recent years.

The mobile communications and wifi networks usually provide the radiation sources for WEH. Thus, the desired frequencies for dual-band rectifiers are 900, 1800 and 2100 MHz for mobile communications, as well as 915, 2450 and 5800 MHz for ISM band applications. Compared with a dual-band rectifier, the broadband rectifier can cover more bands and harvest more energy. However, it usually has a no more than one octave bandwidth which cannot simultaneously cover 915 and 2450 MHz bands [8]-[11]. The dual-band rectifier can compensate this drawback due to the fact that it is easier to achieve a large frequency ratio including 915/2450 MHz [12]-[14].

The key point for a dual-band rectifier design is the dual-band input matching network. In the previous works, single-stage T-type network [12], two stage T-type networks [16], multi-stub networks [14, 15, 17-20], coupled lines [13], and LC networks [21, 22] have been used as the dual-band matching network in the rectifier circuit design. Most of the designs have more than three segments of transmission lines in the matching network which results in large circuit size and complex design [13]-[20]. The LC matching networks can minimize the circuit size [21, 22]. But the low Q capacitors and inductors would lead to higher loss and lower efficiency of the rectifier compared with the transmission line networks.

In this letter, an efficient dual-band rectifier using a stepped impedance stub matching network is proposed for wireless energy harvesting application. The traditional single-stub impedance matching network only can achieve a single band matching performance [7]. In this work, the uniform impedance single-stub is replaced by stepped impedance stub to achieve dual-band performance. We first demonstrate in the simulation that by controlling the impedance and length of the stepped impedance stub matching network, the frequency ratio of the two working frequency bands can be adjusted and large frequency ratio of 3.77 (650 and 2450 MHz) can be achieved. To verify the design concept, a dual-band rectifier working at 0.915 and 2.45 GHz is fabricated and measured. The resulting rectifier uses only three microstrip lines in the matching network which is less than those in the previous works [13]-[20]. So it releases the design complexity and exhibits compact size. The measured results of the rectifier agree well with the simulated results. The measured $|S_{11}|$ is better than -20 dB at the two operating bands and the peak conversion efficiencies are 74% and 73% at 0.915 and 2.45 GHz, respectively.

Shun Li, Fei Cheng, Sha Yu and Kama Huang are with College of Electronics and Information Engineering, Sichuan University, Chengdu, 610065, China. (E-mail: chengfei@scu.edu.cn)

Chao Gu is with Centre for Wireless Innovation, ECIT Institute, Queens University Belfast, Belfast, BT3 9DT, UK. (E-mail: chao.gu@qub.ac.uk)

II. DESIGN AND ANALYSIS OF THE DUAL-BAND RECTIFIER

The block diagram of the proposed dual-band rectifier which works at f_1 and f_2 is shown in Fig. 1. It consists of a single-stub impedance matching network, a Schottky diode, and a DC pass filter. In the single-stub impedance matching network, the shorted stepped impedance stub comprised of TL3 and TL4 can not only achieve dual-band matching, but also provide DC ground for the rectifier. Z_i and θ_i represent the characteristic impedance and electrical length of the ith microstrip transmission line at f_1 ($i = 1, 2, 3, 4$). The single-series topology is chosen here to eliminate the use of an input DC block capacitor required in the single-parallel topology. Thus, the loss of the DC block capacitor can be eliminated to enhance the rectifier efficiency.
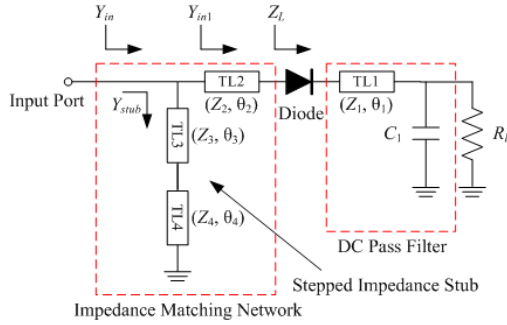

Fig. 1. Schematic of the proposed dual-band rectifier.

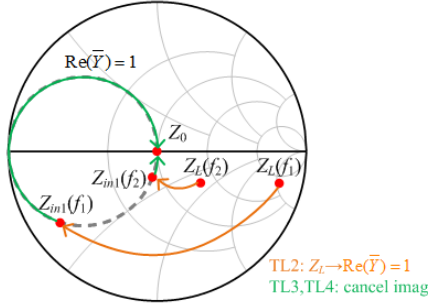### A. Analysis of the dual-band matching network

Fig. 2. Design principle of the input matching network.

Fig. 2 shows the design principle of the input matching network of the dual-band rectifier. As the Schottky diode is a nonlinear component whose impedance is a function of input power and frequency, the diode impedances at f_1 and f_2 GHz are quite different. Thus, Z_L changes with the frequency. $Z_L(f_1)$ and $Z_L(f_2)$ are quite different as shown in Fig. 2. To design the dual-band impedance matching network, firstly, Z_L is transformed to Z_{in1} through a length of series microstrip line TL2. The track of Z_L (f_1 and f_2) moves clockwise. The impedance and electrical length of TL2, Z_2 and θ_3, should satisfy that the real part of normalized $Y_{in1}(f_1)$ and $Y_{in1}(f_2)$ are equal to 1. As shown in Fig. 2, the two points Y_{in1} (f_1 and f_2) are on the circle of Re($\overline{Y}$) = 1. The shorted stepped impedance stub composed of TL3 and TL4 has an input admittance of

$$Y_{stub}(f_i) = -j \frac{Z_3 - Z_4 \tan \theta_4(f_i) \tan \theta_3(f_i)}{Z_3 Z_4 \tan \theta_4(f_i) + Z_3^2 \tan \theta_3(f_i)}, i = 1, 2 \quad (1)$$

which is a pure imaginary number. By properly design Z_3, Z_4, θ_3 and θ_4, the imaginary part of Y_{in1} and Y_{stub} can cancel each other out which makes

$$\overline{Y_{in}}(f_i) = \overline{Y_{in1}}(f_i) + \overline{Y_{stub}}(f_i) = 1, i = 1, 2. \quad (2)$$

Then, the input impedance of the rectifier is matched at two frequencies.

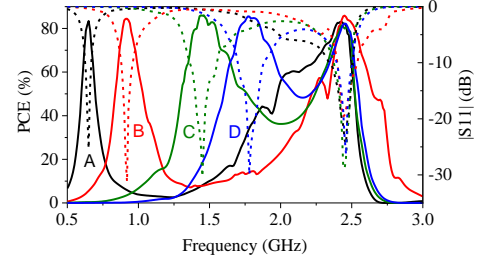### B. Design of the dual-band rectifiers with different frequency ratios

Fig. 3. Simulated $|S_{11}|$ and PCE versus frequency for dual-band rectifiers of 4 frequency ratios. (Dash line: $|S_{11}|$, solid line: PCE)

TABLE I
PARAMETERS FOR THE DUAL-BAND RECTIFIERS OF 4 FREQUENCY RATIOS

Model	Z_1	Z_2	Z_3	Z_4	θ_1	θ_2	θ_3	θ_4
A	51.9	76.1	46.1	30	80.3	282.5	52.4	45.8
B	94.1	97.6	39.8	85.2	66.2	188.1	37.7	22.6
C	95.7	92.4	61.2	37.7	75.9	103.1	25.5	30.7
D	103.2	49.6	98.1	99.6	73.9	82.4	3.8	11.5

Unit: Ω (characteristic impedance) and degree (electrical length @ 2.45 GHz)

The proposed input impedance matching network design is valid for dual-band operation with different frequency ratios. In order to validate it, dual-band rectifiers with 4 different frequency ratios are simulated in ADS. The higher frequency of the rectifiers is fixed at 2.45 GHz while the lower frequency is adjusted at 0.65, 0.915, 1.45, and 1.8 GHz for model A, B, C and D. The corresponding frequency ratios are 3.77, 2.68, 1.69, and 1.36, respectively. In the simulation, the Infineon BAT15-03W Schottky diode is used and it has a series resistance of 5 Ω and zero-bias junction capacitance of 138.5 fF. The original breakdown voltage of the diode in the datasheet is 4.2 V. In our simulation, it was modified to 8.1 V to match the measured peak efficiency point. Moreover, $C_1 = 125$ pF and R_L =1500 Ω. To design the rectifier, firstly, the DC pass filter is designed. TL1 is chosen to have a characteristic impedance of 100 Ω and electrical length of 90 ° @ 2.45 GHz initially. Then, Z_L is calculated by

$$Z_L(f_i) = Z_1 \frac{Z_d(f_i) \| j\omega C_1 + jZ_1 \tan \theta_1(f_i)}{Z_1 + j(Z_d(f_i) \| j\omega C) \tan \theta_1(f_i)} + Z_d(f_i), i = 1, 2 \quad (3)$$

with the diode impedance of [27]

$$Z_d = \frac{\pi R_s}{\cos \theta_{on} \left(\frac{\theta_{on}}{\cos \theta_{on}} - \sin \theta_{on} \right) + j\omega R_s C_j \left(\frac{\pi - \theta_{on}}{\cos \theta_{on}} + \sin \theta_{on} \right)} \quad (4)$$

where R_s is the series resistance of the diode, C_j is the diode junction capacitance, and θ_{on} is the turn on angle of the diode. After that, the input matching network can be gained by the previous analysis. Finally, all the circuit parameters are optimized in ADS. The simulated $|S_{11}|$ and PCEs (Power Conversion Efficiency) are shown in Fig. 3 and the optimized rectifier parameters are listed in Table I. It can be seen that $|S_{11}|$ at the working frequencies is always better than -20 dB which indi-

cates a good matching is achieved at the rectifier input port. It ensures that the rectifiers reflect little energy back to the source and most input RF energy goes into the diode. In Fig. 3, the peak PCEs of the rectifiers are better than 80% at the working frequencies. In general, the proposed matching network can work effectively in the dual-band rectifier design with various frequency ratios.

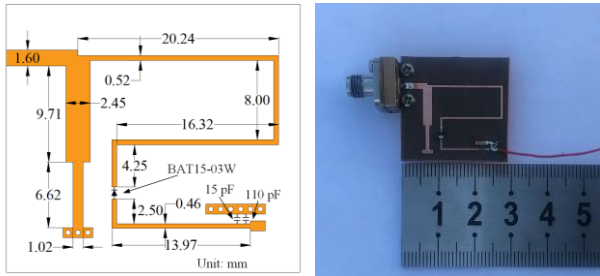### III. IMPLEMENTATION AND MEASUREMENT RESULTS

Fig. 4. Layout and photograph of the proposed dual-band rectifier.

The proposed dual-band rectifier at 0.915 and 2.45 GHz is fabricated on a Taconic TLY substrate with a thickness of 0.508 mm, a relative dielectric constant of 2.2, and a loss tangent of 0.0009. The Infineon BAT15-03W Schottky diode is implemented. In addition, two capacitors of 15 and 110 pF are used in the output DC pass filter. Fig. 4 shows the layout and photograph of the fabricated rectifier. A portion of the microstrip line is folded to minimize the circuit size. The dimensions of the rectifier are 21.47 mm $\times$ 18.93 mm.
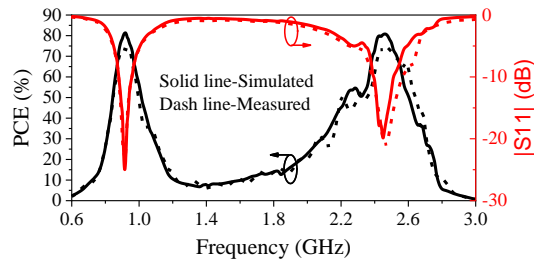

Fig. 5. Simulated and measured $|S_{11}|$ and PCE versus frequency.
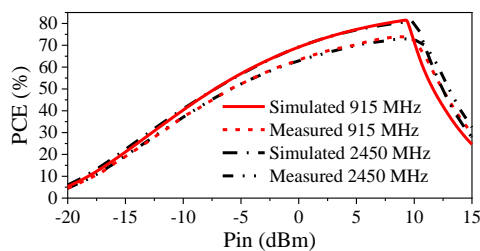

Fig. 6. Simulated and measured PCE versus input power.

Fig. 5 shows the simulated and measured $|S_{11}|$ and PCE changing with the frequency. The rectifier is working at 9 dBm input power with the load resistance of 1500 Ω. The measured and simulated results agree well with each other except that the higher band has a small shift. This may result from the discrepancy of the capacitor and diode model parameters between the simulation predictions and real-world scenarios at high frequencies. The measured $|S_{11}|$ are -23.34 and -21.19 dB at 0.915 and 2.45 GHz respectively while the simulated ones are

-24.98 and -19.87 dB at the two frequencies. The measured maximum PCEs are higher than 70% from 0.89 to 0.95 GHz and 2.42 to 2.51 GHz while the simulated ones are from 0.88 to 0.96 GHz and 2.39 to 2.53 GHz. Fig. 6 shows the simulated and measured PCEs versus the input power at 0.915 and 2.45 GHz with the load resistance of 1500 Ω. The measured maximum efficiencies are 74% and 73% at 0.915 and 2.45 GHz respectively which are about 8% lower than the simulated ones. The measured input power ranges for PCE > 50% are from -5 to 12 dBm at 0.915 GHz and -5 to 13 dBm at 2.45 GHz, respectively. Table II compares the proposed rectifier in this work with some previously published works. As observed, the proposed rectifier has higher efficiency than most other designs and smallest dimensions except the CMOS rectifier chip in [21]. Additionally, the impedance matching network in our design is simplest with only 3 transmission line segments.

TABLE II
COMPARISON BETWEEN THE PROPOSED RECTIFIER AND THE REFERENCES

Ref.	f_{RF} (GHz)	Peak PCE Point		Size (mm²)	Diode	No. of TL
		P_{in} (dBm)	PCE (%)			
[12]	0.915, 2.45	12	81.7, 73.1	74.1 $\times$ 35.3	HSMS 2862	3
	0.915, 2.45	-1	69.2, 64.1	80.3 $\times$ 23.4	SMS76 30	3
[13]	0.915, 2.45	30	66, 58	about 60 $\times$ 79	HSMS 2822, HSMS 2852	4
[14]	0.915, 2.45	14.6	77.2, 73.5	about 60 $\times$ 87	HSMS 2862	5
[15]	0.915, 1.8	5	NA	37 $\times$ 23	HSMS 2850	6
[16]	1.84, 2.14	-18	37.5, 34	146 $\times$ 26.5	HSMS 2852	6
[17]	2.45, 5.8	11	64.8, 64.2	48.1 $\times$ 40.1	HSMS 286	4
[18]	2.45, 5.8	0	57.6, 33.62	89 $\times$ 34	HSMS 2850	6
[20]	1.8, 2.45	9	70, 68	0.25 λ_g^2	HSMS 285C	7
[21]	0.93, 2.63	-1	25.2, 22.5	2.9 $\times$ 4	CMOS	LC
[22]	0.915, 2.45	-15	23,18	NA	SMS76 30	LC
This work	0.915, 2.45	9	74, 73	21.5 $\times$ 18.9	BAT15 -03W	3

No. of TL: number of transmission line segments in the input matching circuit

IV. CONCLUSION

In this letter, an efficient dual-band rectifier using a stepped impedance stub matching network for WEH is presented. The practicality of the proposed topology is demonstrated through the fabrication of a 0.915 and 2.45 GHz dual-band rectifier. At 9 dBm input power level, the maximum conversion efficiencies are 74% and 73% at 0.915 and 2.45 GHz, respectively. Compared with other reported dual-band rectifiers, the proposed rectifier has the advantages of large frequency ratio, high efficiency, simple structure, and small dimensions. The rectifier can be used in a WEH system due to the outstanding performance at low input power.

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