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Efficient FPGA Implementation of Multilayer Perceptron for Real-Time Human Activity Classification

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ABSTRACT The smartphone-based human activity recognition (HAR) systems are not capable to deliver high-end performance for challenging applications. We propose a dedicated hardware-based HAR system for smart military wearables, which uses a multilayer perceptron (MLP) algorithm to perform activity classification. To achieve the flexible and efficient hardware design, the inherent MLP architecture with parallel computation is implemented on FPGA. The system performance has been evaluated using the UCI human activity dataset with 7767 feature samples of 20 subjects. The three combinations of a dataset are trained, validated, and tested on ten different MLP models with distinct topologies. The MLP design with the 7-6-5 topology is finalized from the classification accuracy and cross entropy performance. The five versions of the final MLP design (7-6-5) with different data precision are implemented on FPGA. The analysis shows that the MLP designed with 16-bit fixed-point data precision is the most efficient MLP implementation in the context of classification accuracy, resource utilization, and power consumption. The proposed MLP design requires only 270 ns for classification and consumes 120 mW of power. The recognition accuracy and hardware results performance achieved are better than many of the recently reported works.

INDEX TERMS Human activity recognition, multilayer perceptron, smart military wearables, classifier hardware implementation, field programmable gate array.

I. INTRODUCTION

In the area of ubiquitous sensing, the wearable sensors are used to measure human body attributes like body motion, location, temperature, ECG, etc. The data received from the sensors are integrated, processed and analyzed on network-connected devices like smartphones or laptops. Some of the meaningful information like human activity is also extracted on these devices. In the last decade, the Human Activity Recognition (HAR) based on the wearable sensor has attracted many researchers [1]. Nowadays, the smartphones have become the most feasible device for HAR implementations, because smartphones are equipped with a variety of low power and small size sensors [2], [5]. Many such HAR based applications are successfully implemented on the smartphone platforms [5], [33], [34], like complex activity recognition [3], sporting activity detection [4], etc. However, the smartphone based HAR systems are not suitable and capable to deliver the required performance in case of challenging applications like the workforce monitoring in a military combat scenario [6], [10].

A real-time soldier activity information along with other sensory information is a useful feedback for workforce monitoring, smart backup, rescue operation and virtual war field mapping [6], [10]. This inspired us to incorporate soldier activity recognition in the smart military wearables. Due to difficult combat conditions, the hardware of smart wearables has to meet the stringent system requirements like fast response time, high performance per watt ratio, small form factor, higher reliability and flexibility [10]. Such requirements are achievable only by using parallel processing hardware solutions like FPGAs [22], [28]. The efficient implementation of an activity recognition algorithm on such devices plays a crucial role in wearable system performance.

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The customized hardware implementation has the capability to achieve low latency and low power consumption compared with the software implementations. Hence, the hardware is a favorable choice for HAR implementation for the challenging applications. Few attempts of HAR algorithm implementation on reconfigurable hardware are reported in the literature [22], [29], [30]. These implementations are focused on the hardware design and modeling of activity classifier. Because these classifiers are computationally complex and heavy, it highly influences the overall hardware performance of a HAR system. Therefore, the efficient and flexible hardware implementation of an activity classifier is a challenging problem for the development of the customized HAR system.

In presented work, the hardware-based MLP classifier has been developed for activity recognition in the smart wearable gateway (Xilinx Artix-7 FPGA). The activity classification is obtained from a single accelerometer placed on the soldier's waist. The activity is classified into five basic classes: walking, sitting, standing, laying and activity transitions. Ten MLP models with different numbers of hidden layer perceptrons have been trained and tested on HAR dataset of 20 subjects. For final hardware implementations, an MLP topology with 7-6-5 is selected from the simulation results. Then, the five hardware models of MLP design with different data precision are synthesized, implemented and tested on the Artix-7 FPGA. The detailed competitive analysis of classification accuracy, hardware resource utilization, classification latency and power consumption has been presented for all five models in this work. The real-time and power-efficient intellectual property (IP) core for HAR with adequate classification accuracy is the main contribution of this work. This IP core enables the smart wearable gateway to recognize the current soldier activity in real-time with decent classification accuracy. Likewise, the achieved minimum power consumption of IP core increases the battery life of the smart wearable. The same IP core and development methodology can be further extended to the build the smart wearables for firefighters, police professionals, mines workers, etc. In addition, the comparison of this work with other existing HAR systems and FPGA based MLP implementations is also presented.

The remainder of the paper is organized as follows. In Section-II, we review HAR classifier algorithms and hardware implementation of MLP classifiers reported for various applications including HAR. Section-III discusses detailed hardware design architectures of a perceptron and MLP. In Section-IV, we describe the complete hardware implementation and testing procedures. Section-V discusses the implementation and performance analysis of MLP designs. Finally, Section-VI concludes this work with important research findings.

II. RELATED WORK

Many HAR systems adopted various classification algorithms like the decision tree, Markov models, domain transform, fuzzy logic, support vector machine (SVM), regression methods, artificial neural networks (ANN), K-nearest neighbor (KNN), etc. [1]. Wei *et al.* [7] proposed the two-layer Hidden Markov Model (HMM) for continues and long-term daily activity monitoring which uses wearable body sensors. Andreu and Angelov [8] suggested the fuzzy based algorithm for real-time human activity recognition. In this work, rule-based and self-learning fuzzy classifier extracts class information from wearable wireless accelerometers. After the extensive analysis, Janidarmian *et al.* [31] found that the KNN with ensembles methods shows the best robust results among the other machine-learning models. Rodriguez *et al.* [23] reported BioHarness and smartphone based activity recognition using decision tree for the classification. Zebin *et al.* [24] conducted the comparison between different HAR algorithms for the inertial sensor data. Tang and Sazonov [9] compared the ANN and SVM classification algorithms for the smart shoe. From the accuracy results, Tang et al. concluded that the ANN classification algorithms performs well compared with the SVM algorithm. Therefore, we adopted ANN as an activity classification algorithm for the workforce monitoring.

Many applications adopted ANN for classification, control and calibration tasks in biomedical instrumentation [11], [12], control systems [13], [14], non-conventional energy production [15], [16], etc. However, the efficient implementation and real-time execution of ANN models on embedded platforms are still a challenging problem because it involves plenty of nonlinear activation functions, numerous amounts of additions and multiplications. The implementation of these algorithms demands high performance parallel computing devices like FPGA's. Because of an inherently parallel architecture of ANN algorithms, FPGA devices are becoming a favorable choice compared with sequential devices [17], [25]. The modern FPGA has specialized blocks like DSP and BRAM to handle complex mathematical operations. The soft-core and hardcore processor are also available to enhance sequential capability. This makes the FPGA technology most suitable for the implementation of soft-computing algorithms (like ANN) for real-time applications [18].

The feed-forward type of ANN architecture is the most commonly used ANN architectures, it is also generally known as the MLP. Many FPGA based MLP classifier models are reported in the literature for various applications. Gas classification is one of the popular application of these types of classifiers [19]. Recently, Zhai *et al.* [20] proposed a real-time gas classification system, which takes 540 nanoseconds for the classification. Bahoura [21] designed MLP based blue whale calls classifier using Xilinx system generator toolbox. However, this model is unable to achieve real-time performance. Nevertheless, it requires significantly less development time compared with traditional design methods. Therefore, we selected high-level programming methodology for the development of target MLP design.

Many smartphones based HAR systems are available [32], but a very limited work has been reported on dedicated hardware (FPGA) based HAR implementation. Like in [30], Biswas *et al.* designed and implemented the real-time arm movement recognition that required 41.2 microseconds for recognition. Yan *et al.* [29] tested the MLP based HAR design on the two different FPGAs and got impressive results compared to the smartphones implementations. Basterretxea *et al.* [22] implemented an MLP algorithm on FPGA (Xilinx XC6SLX45CSG324-2) for the generalized HAR system. These work motivated us to implement efficient hardware based activity classification for the smart military wearables. This study explore the efficient and flexible hardware implementation approach for the MLP based activity recognition.

III. HARDWARE ARCHITECTURE

The hardware design of the MLP classifier is broadly divided into two parts. The elementary unit of the architecture is a perceptron model and a united network of these perceptrons is MLP model. A group of multiple and independent perceptrons are referred as a perceptron layer. The feature information is processed and forwarded from one layer to another completely connected layer. This multiple layers of perceptron's are used to solve complex classification problems like activity recognition. This type of network is also known as fully connected feed-forward neural network. In this work, the final MLP activity classifier is constructed from elementary perceptrons using Xilinx system generator toolbox. The detailed mathematical formulation and hardware design of a perceptron and MLP classifier have been discussed in the following two subsections.

A. PERCEPTRON MODEL

A perceptron is a fundamental block of MLP architecture, which is inspired by brain neuron cell. A perceptron receives inputs from the previous layer and forwards the output to next layer after performing some mathematical operations. Equation (1) shows the mathematical operation performed by a perceptron.

$$Y_k(x) = f\left\{\sum_{i=1}^{n}(w_{ki}x_i + b_k)\right\} \tag{1}$$

where, Y_k is a output of k^{th} perceptron, w_{ki} is i^{th} element of the pre-trained weight matrix of k^{th} perceptron in l^{th} layer, x_i is i^{th} input of perceptron and b_k is the bias of a perceptron and f is the activation function. In this work, we are using the sigmoid function as the non-linear activation function and it is the most computationally intensive part in the perceptron design. Therefore, we used the approximation of this function known as the *PLAN* function (f). The *PLAN* function is one of the best approximations of the sigmoid function that requires less hardware resource as compared to other sigmoid approximations [25]. The mathematical description of *PLAN* function is shown in Table 1. Mathematical model of a perceptron that is designed for the FPGA implementation is presented in Figure 1.

TABLE 1. Approximation of sigmoid function.

x	*f(x)*
$0\leq \|x\| <1$	$0.25\times\|x\|+ 0.5$
$1\leq \|x\| <2.375$	$0.0125\times\|x\|+ 0.625$
$2.375\leq \|x\| <5$	$0.03125\times\|x\|+ 0.84375$
$5\leq \|x\|$	1

As highlighted in Figure 1, the input signals are multiplied with the pre-trained weights and then added together with the pre-trained bias. The pre-trained weights and biases are stored in the distributed memory of FPGA fabric. The output of an addition block is connected to the *PLAN* function. The *PLAN* function (f) is efficiently modeled using elementary computational blocks that requires minimum FPGA hardware resource [25]. This same design method has been used for designing of all perceptrons.

We used high-level FPGA design methodology for the implementation of perceptron model. This programming technique significantly reduces the design time and provides sufficient design flexibility. Figure 10 (See Appendix. B) shows a perceptron model designed by the Xilinx system generator toolbox.

B. MLP MODEL

A MLP model contains multiple layers of perceptrons connected in a feed-forward manner. The output of the final layer is terminated with a soft-max function to use it as a classifier. As our implementation is limited to the testing phase of MLP, we used normal maximum instead of the soft-max function to reduce the FPGA resource utilization [26].

The proposed MLP design uses three layers i.e. input, output and a hidden layer. As shown in the Figure 2, Layer 1 is the input layer that performs normalization on all i number of features. Generally, MLP consist of one or more number of hidden layers, but in the present work, we used only one hidden layer to reduce the classification delay and hardware resource utilization. The complete MLP mathematical model is shown in Figure 2, a hidden layer (Layer 2) consists of j number of hidden perceptron. The output matrix of the hidden layer is shown in (2).

$$\boldsymbol{X}^2 = \boldsymbol{f}_1\left\{\boldsymbol{W}^2 \times \boldsymbol{X}^1 + \boldsymbol{B}^2\right\} \tag{2}$$

where $\boldsymbol{W^2}$ is the hidden layer weight matrix, $\boldsymbol{X^1}$ is the output matrix of an input layer, $\boldsymbol{B^2}$ is the bias matrix of the hidden layer and $\boldsymbol{f_1}$ is a sigmoidal approximation. The MLP classifies input features into "k" classes. Therefore, the output layer (Layer 3) consists of "k" output perceptron. The output matrix of this output layer is calculated using equation (3).

$$\boldsymbol{Y} = \boldsymbol{f}_2\left\{\boldsymbol{W}^3 \times \boldsymbol{X}^2 + \boldsymbol{B}^3\right\} \tag{3}$$

where $\boldsymbol{W^3}$ is the weight matrix of the output layer, $\boldsymbol{X^2}$ is the output matrix of the hidden layer, $\boldsymbol{B^3}$ is the bias matrix of the output layer and $\boldsymbol{f_2}$ is the pure linear activation function.

Figure 11 (See Appendix. B) shows the MLP model with 7-6-5 topology, designed by Xilinx system generator toolbox.

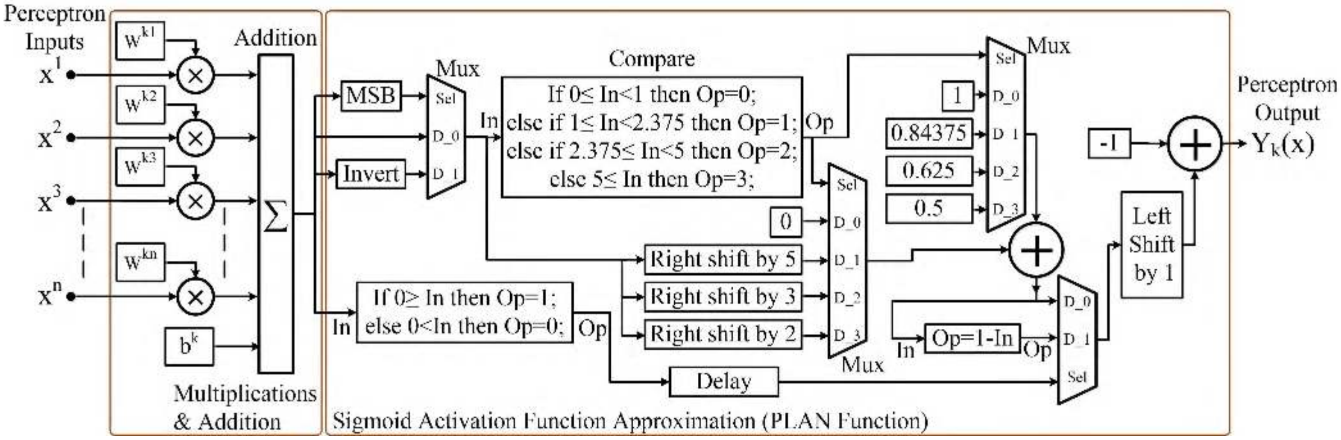


FIGURE 1. Mathematical model of a perceptron.

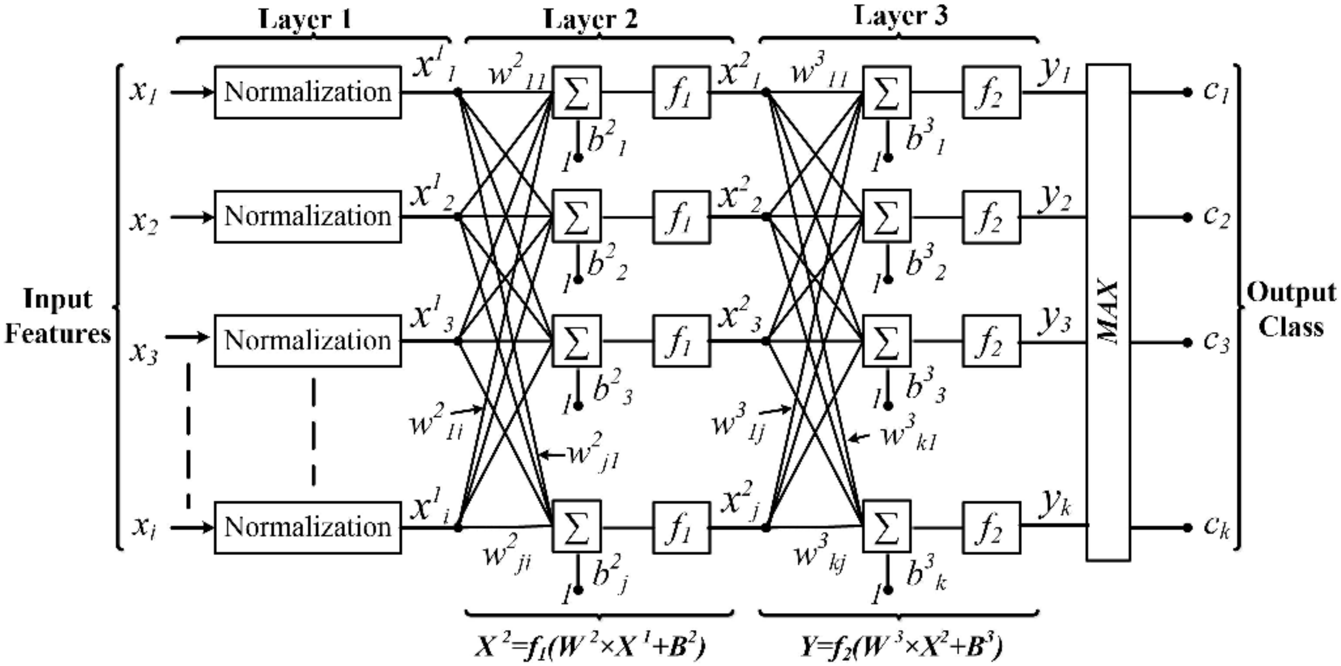


FIGURE 2. Mathematical model of MLP classifier with i-j-k topology.

We selected seven input features for soldier activity recognition that decides numbers of normalization blocks in the input layer. There are five different essential output classes identified for the soldier activity classification that decides numbers of perceptrons in the output layer. The number of hidden perceptrons has been decided from the experimental analysis presented in the fourth section.

We used inherent MLP architecture to achieve the minimum classification latency and maximum design flexibility. As shown in Figure 11 (See Appendix. B), the MLP design consists of eight input signals from which seven signals (F1 to F7) work as feature inputs and "ST" works as an enable signal. There are two output signals in which "CLS" works as an output class signal (walking, sitting, standing, laying and activity transitions) and "D" works as an acknowledgment signal. All of the perceptrons are connected in a feed-forward manner, which works synchronously with a control signal. The internal architecture of all hidden layer perceptrons is similar as shown in Figure 10 (See Appendix. B). The architecture of all output layer perceptrons is also similar to hidden layer perceptron only excluding activation function approximation.

The MLP mathematical model is inherently parallel i.e. every perceptron in a layer works independently. Hardware implementation of this parallel algorithm on sequential devices requires more computation time and power, compared with the parallel processing devices [17]. Hence, we used parallel processing device like FPGA for MLP implementation. The proposed hardware design achieved the complete hardware parallelism required for the computation of a single layer. Every perceptron in the single layer functions independent and parallel with the layer synchronization. This results into the significant reduction in classification latency for the time-sensitive applications like soldier activity recognition.

IV. HARDWARE IMPLEMENTATION AND TESTING

The MLP hardware design is targeted for real-time soldier activity recognition in smart wearable gateway. The activity classification is done by the 3-axis accelerometer data located on the soldier waist. As this work focuses on the hardware design of the MLP classifier, we used the available accelerometer data set for the evaluation of MLP classifier hardware implementation [16]. A sensor node has been simulated in LabVIEW using this dataset. The simulated node is used for the performance evaluation of the MLP design in the hardware. The detailed description of the used dataset, FPGA implementation and testbed setup is given in the following subsections.

A. DATASET DESCRIPTION

The training and testing performance analysis of MLP classifier has been done on UCI transition-aware human activity recognition dataset [36]. A 3-axial accelerometer is used for body motion data acquisition that is placed on the subject's waist with a sampling frequency of 50 Hz. The generated raw data is segmented into 2.56 seconds segments with 50% overlap. Many important features are extracted from these data segments, out of which we have used seven types of data features. The selected features are body acceleration standard deviation of all three axes, the signal magnitude area of body acceleration and gravity acceleration mean of all axis [27]. The five basic and important output classes (walking, sitting, standing, laying and activity transition) are selected for the soldier activity recognition. This work used 7767 feature vector samples of 20 subjects from the complete dataset. The three different combinations of training, validation and testing samples are selected from the original dataset. The numbers of training, validation and testing samples selected for each dataset are mentioned in Table 5 (See Appendix. A).

B. FPGA IMPLEMENTATION

The present application demands efficient MLP performance for field operations. After completion of appropriate training, MLP design works in the testing phase. Thus, there is no need to implement training hardware in actual field operations. Therefore, this work uses the off-line training method to avoid unnecessary hardware burden of training. These MLP designs are trained off-line using the MATLAB. Ten MLP models per dataset with distinct topologies have been trained and validated to finalize the optimum MLP topology. Three sets of testing samples(1165, 1941 and 2718) are used for the testing of all MLP models in MATLAB simulation. The comprehensive analysis of testing results is presented in the next section.

After training, calculated weight and bias matrices have been included in the hardware model of the MLP design. These parameters are stored in the distributed memory of FPGA fabric to avoid time and power-consuming memory read cycles required for external memory access. The five different variant of MLP design has been implemented with five distinct input-output (IO) data precision of all perceptrons. In addition, the data precision of all weights and biases has been set constant with fixed-point 16-bit precision. The complete MLP has been designed by Xilinx system generator design toolbox, which helps to reduce development time and generate the flexible design. This MLP design is packaged into a Xilinx IP Core after completion of design and performance evaluation. This flexible IP core can be implemented on the any Xilinx FPGA by only changing the design token configurations. In this work, the MLP IP core is implemented on the Xilinx FPGA (Artix-7-35T, xc7a35ticsg324-1L) with operating frequency of 100 MHz. The softcore processor (Microblaze) based IP test system has been developed for the hardware performance evaluation of MLP IP core. Figure 12 (See Appendix. B) shows the hardware design of Microblaze based IP test system. The Vivado IP integrator software is used for the complete development of IP test system. The MicroBlaze is programed with IP test application using Xilinx SDK.

C. TESTBED SETUP

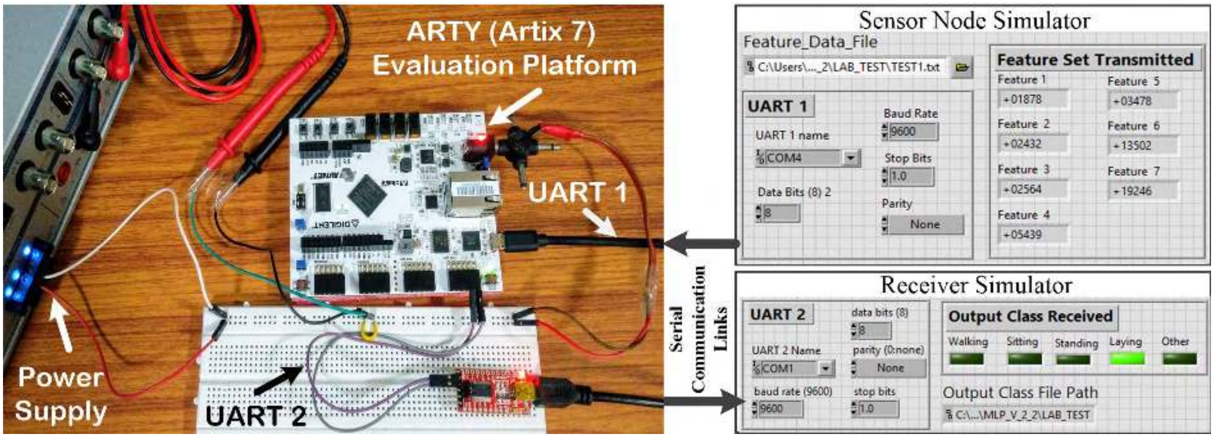
The hardware testing is important to evaluate the operational performance of the MLP IP core. Figure 3 shows hardware testbed setup for MLP IP core testing. Setup is divided into two parts, the first part is Microblaze based IP test design with MLP IP core and second part is LabVIEW based sensor node simulator and receiver simulator. The sensor node in a targeted application handles the data acquisition, segmentation and feature extraction, which is forwarded to the gateway using UART communication link. After the evaluation of output class, the current soldier activity is further forwarded to the receiver. As shown in Figure 3, the same practical scenario has been simulated using LabVIEW based GUI. The sensor node simulator sends test features of dataset-A to the gateway (Artix-7 FPGA) through UART-1 communication link. The activity classification is performed on the gateway using the MLP IP core running and then calculated class is forwarded to receiver simulator using UART-2 link.

V. PERFORMANCE EVALUATION

To meet the defense field requirements, the performance evaluation of MLP IP core is focused on optimum topology selection, classification accuracy, hardware resource utilization, classifier power consumption and classification latency. The detailed analysis of simulation and implementation results have been discussed in the following subsections.

A. MLP TOPOLOGY SELECTION

The training and validation of basic MLP design have been conducted on MATLAB using back-propagation algorithms.



Sensor Node Simulator

Feature_Data_File: C:\Users\..._2\LAB_TEST\TEST1.txt

UART 1

UART 1 name: COM4

Baud Rate: 9600

Stop Bits: 1.0

Data Bits (8) 2: 8

Parity: None

Feature Set Transmitted

Feature 1: +01878

Feature 2: +02432

Feature 3: +02564

Feature 4: +05439

Feature 5: +03478

Feature 6: +13502

Feature 7: +19246

Receiver Simulator

UART 2

data bits (8): 8

UART 2 Name: COM1

parity (0:none): None

baud rate (9600): 9600

stop bits: 1.0

Output Class Received

Walking Sitting Standing Laying Other

Output Class File Path: C:\...\MLP_V_2_2\LAB_TEST

FIGURE 3. Hardware testbed setup for MLP IP Core testing.

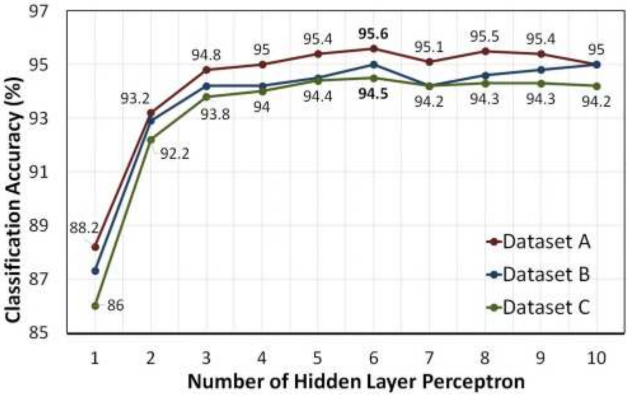


FIGURE 4. Change in classification accuracy with the respective number of hidden layer perceptrons.

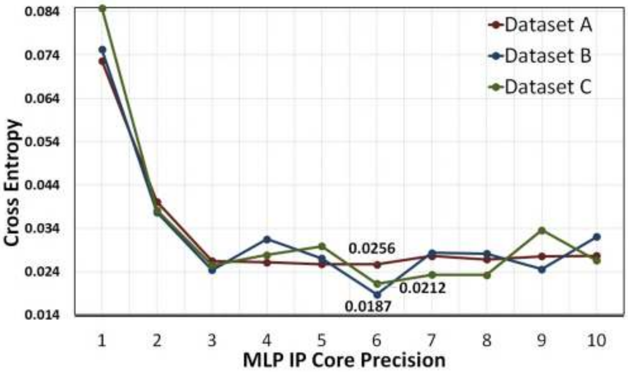


FIGURE 5. Change in cross entropy performance with the respective number of hidden layer perceptrons.

This work used MLP with a single hidden layer, which helps to reduce the classification latency, hardware resources and power consumption. This configuration also minimizes the over fitting in MLP design [40]. The seven types of features are selected for the classification and five output classes are chosen, which gives the MLP design with seven perceptrons in an input layer and five perceptrons in an output layer. Now, the final topology of MLP design depends only on the numbers of hidden layer perceptrons, which is decided from the following analysis.

In this work, the iterative constructive method is used to decide the optimum numbers of hidden layer perceptrons [41]. Ten possible MLP designs have been generated by changing the number of hidden layer perceptrons for each dataset. Thirty independent MLP models have been trained and validated on three datasets A, B and C (see Table 5 in Appendix. A). Then, the generated MLP designs are tested on test samples of respective datasets that works on floating-point data operations.

Figure 4 shows the graph of classification accuracy versus the number of hidden layer perceptrons for all datasets. The accuracy is the average of 10 similar training, validation and testing of each MLP models. As each extra perceptron contributes to the hardware resource utilization and power consumption, hence we allowed maximum ten perceptrons in the hidden layer. It is clear from the Figure 4 that the MLP design with six hidden layer perceptrons gives maximum classification accuracy for all three test datasets. Similarly, The validation performance in from of average cross entropy is also shown in Figure 5. The minimum cross entropy is achieved by the six hidden layer perceptrons for all datasets. Both results indicate that the hidden layer with six perceptrons performed better compared with other combinations. Therefore, we selected MLP topology (7-6-5) with six hidden layer perceptron for the FPGA implementations.

B. HARDWARE CLASSIFICATION ACCURACY

The hardware of finalized MLP model (7-6-5) has been designed by Xilinx system generator toolbox. Five different MLP designs with distinct data precision have been synthesized, implemented and tested. The input and output (IO) bit precision of all the perceptrons have been set distinct in each variant of MLP IP core. The selected precision are 24, 20, 16, 12 and 8 bits respectively. However, the precision of weights, biases and feature inputs have been kept constant as a 16-bit in all variant MLP IP core. All these versions have been implemented and tested using the same procedure as explained in

Section-IV (Subsection B and C). The hardware accuracy of each version is tested on the test data with 1165 samples. Figure 6 shows the classification accuracy with different implemented models. The accuracy is almost constant up to the 16-bit precision model and below this, it starts decaying. The models with 24 and 20 precision requires more power and hardware resources compared with the 16-bit precision, which is explained in the following subsection. Therefore, as per our application constraint, the MLP IP core with the 16-bit perceptrons IO precision is proven as the best solution in the classification accuracy context.

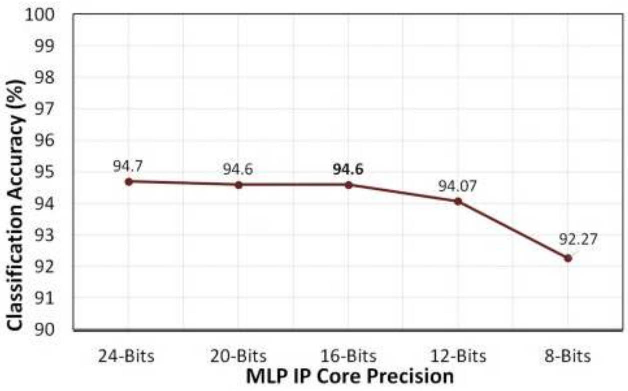


FIGURE 6. Change in classification accuracy with respective MLP IP Core precision.

TABLE 2. Detailed classification results of MLP design with 16-Bit precision.

Positive Class	Sensitivity	Positive Predictive Value	Specificity	Negative Predictive Value	Accuracy
Walking	100%	98.97%	99.27%	100%	99.57%
Sitting	83.03%	89.6%	97.78%	96.16%	95.02%
Standing	91.71%	85.04%	96.31%	98.07%	95.45%
Laying	99.48%	99.48%	99.9%	99.9%	99.83%
Activity Transition	99.91%	87.93%	98.08%	99.37%	99.31%

Table 2 presents the class wise sensitivity, positive predictive value, specificity, negative predictive value, and accuracy. The result indicates that the confidence of output sitting class is comparatively less among all classes. In addition, the classification results of walking, laying and activity transition is more accurate than the sitting and standing class.

C. HARDWARE RESOURCE UTILIZATION ANALYSIS

As mentioned in above subsection, the five different versions of MLP design are implemented on the Artix-7 FPGA. The implementation reports of all five designs have been analyzed collectively. The change in perceptron IO precision effects the hardware resource utilization of MLP IP core design. As shown in Figure 7, the linear reduction in the FPGA resource utilization with respective IO precision is observed. However, the DSP (DSP48E1) utilization remains same for all MLP versions. From Figure 7, it can be observed that the MLP design with 8-bit perceptrons IO precision has emerged as the most efficient design. However, as shown in Figure 6, the classification accuracy of 8-bit MLP design is lowest among all. Therefore, the MLP design with 16-bit IO precision has proved as a high accuracy and moderate resource utilization model.

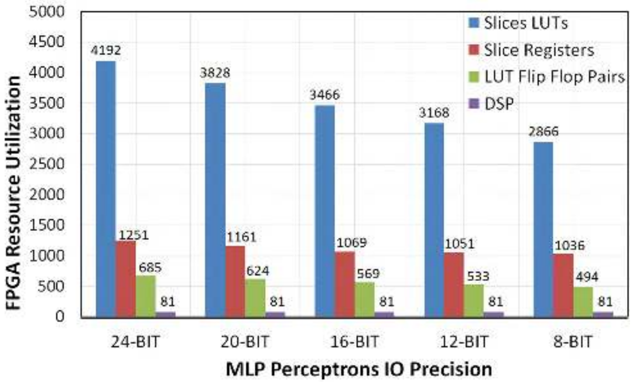


FIGURE 7. Effect of change in MLP perceptrons IO precision on the FPGA resource utilization.

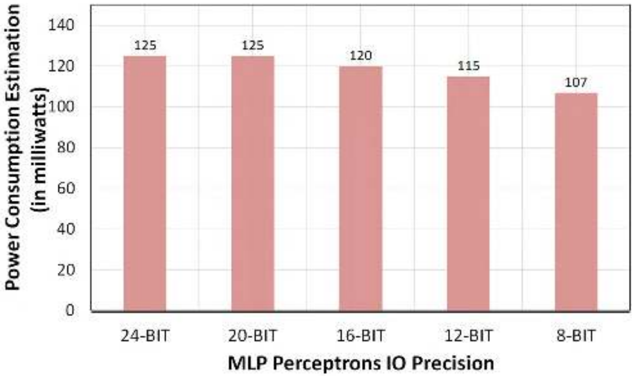


FIGURE 8. Effect of change in MLP perceptrons IO precision on the designs power consumption.

D. POWER CONSUMPTION ANALYSIS

The power consumption of all designs has been estimated by Xilinx power estimator toolbox with same parameter settings. The operating frequency of FPGA is set at 100 MHz for all models.

The power consumption significantly depends upon the FPGA resource utilization and operating frequency. Therefore, the same trends have been observed like hardware resource utilization in power consumption estimations as shown in Figure 8. The DSP slices are the major contributor to the total power consumption of MLP design. It adds 44 milliwatts of dynamic power into each design. As the DSP slices used by all the designs are same, therefore there is a gradual change in the power consumption profile. Like resource utilization scenario, the MLP design with 16-bit IO precision has emerged as an optimal solution for accuracy and power consumption.

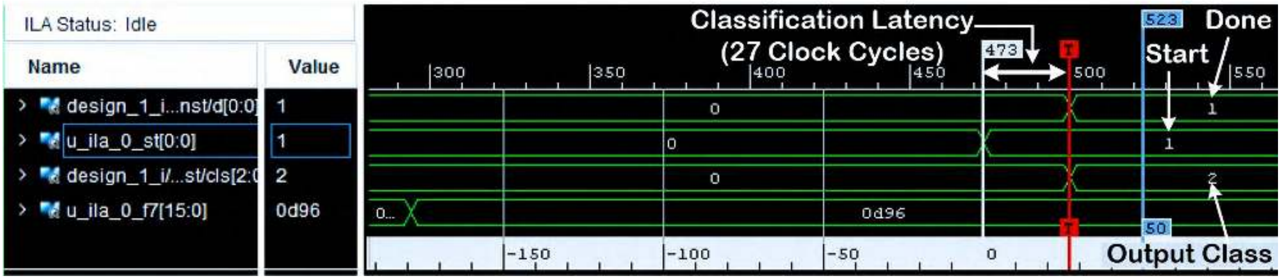


FIGURE 9. Timing response of interfacing signals during live design run on FPGA.

TABLE 3. The accuracy comparison with other HAR implementations.

Works	Classification Algorithm	Implementation Method	Subjects	Activities	Platform	Overall Accuracy
[34]	Multi-classifier	Software	29	5	Android phone	91.70%
[37]	Random Forest	Software	10	8	Weka Software with PC	89.40%
[39]	Multiple Regression	Software	6	12	Matlab Software with PC	90.30%
[38]	1D CNN	Software	5	3	TensorFlow Software with PC	92.71%
[32]	Random Forests	Software	10	5	MEXZU MX3 with Android OS 4.4x	86.20%
[22]	MLP	Hardware	6	7	Spartan-6 (XC6SLX45CSG324-2)	89.20%
This Work	MLP	Hardware	20	5	Artix-7 (35T,xc7a35ticsg324-1L)	**94.60%**

TABLE 4. FPGA performance comparison with MLP classifiers.

Works	MLP Topology	FPGA Platform	Data Precision	Classification Time (Nano-Seconds)	Total Power Consumption	Hardware Resources Utilization			
						BRAM	DSP	FF	LUT
[22]	14-19-19-7	Spartan-6 (XC6SLX45CSG324-2)	16	800 ns	294 mw	39	7	774	1032
[21]	12-7-3	Artix-7 (xc7a100t)	24	19968 ns	123 mw	2	219	13330	21648
[20]	12-3-1	Zynq-7000 (XC7Z010T-1CLG400)	24	540 ns	1776 mw	2	28	2863	4032
This Work	7-6-5	Artix-7 (35T,xc7a35ticsg324-1L)	16	**270 ns**	**241 mw**	**0**	**81**	**569**	**3466**

E. CLASSIFICATION LATENCY

The hardware testing of MLP design is conducted by MicroBlaze based test system and LabVIEW based GUI's. The MLP design is packaged in an IP core, which communicates with a test system using AXI-Lite interface mentioned in Figure 12 (See Appendix. B). The classification latency is calculated by observation of AXI-Lite bus transitions during live hardware design run. The bus transitions are acquired by USB-JTAG programming circuitry and Vivado system debugger toolbox. Figure 9 shows signal transitions during actual MLP algorithm execution with 16-bit IO precisions on FPGA. After sending last feature (f7) to MLP IP core, "st" signal becomes high. At this point, IP starts classification task and generate acknowledgment signal "d" after completion. Total 27 clock cycles are required for classification. The test system and MLP IP operates on 100 MHz so total 270 nanoseconds are required for classification. As highlighted in Figure 9, the "cls" signal is output class send by MLP IP, which is two (sitting) for present feature vector. The hardware architecture of all MLP version is same except perceptrons IO precision. Therefore, the classification latency of all MLP versions is the same.

F. COMPARISON WITH EXISTING WORKS

The HAR systems reliability depends upon the activity recognition accuracy. Table 3 shows the accuracy comparison with some previous works. Various types of HAR classification algorithms were adopted for accelerometer inputs in these works. In works [32], [34], classification algorithms are implemented on the smartphone platform with floating point data precision. The work presented in [22] and this work implemented a classification algorithm on the customized hardware with fixed bit precision. The comparison shows that the accuracy of the proposed classifier outperforms all implementations.

Many recently reported research work implemented the MLP algorithm on various FPGA platforms. We compared this work with similar FPGA based MLP classifier implementations designed for various applications. Table 4 shows the hardware performance comparison of this MLP IP (16-bit precisions) with other MLP implementations. Hardware design simplicity affects the maximum operating frequency, which directly decides classification latency of MLP design. To achieve optimum hardware performance, we adopted the inherent MLP architecture in hardware designing and we

TABLE 5. Details of classification datasets.

Dataset	Training Samples	Validation Samples	Testing Samples	Training+Validation to Testing Ratio
Dataset A	5612	990	1165	85:15
Dataset B	4952	874	1941	75:25
Dataset C	4292	757	2718	65:35

used DSP blocks for multiplications.Due to this approach, the MLP IP core achieved 270 nanosecond classification latency, which is the lowest among all mentioned models. We chose Artix-7 35T (xc7a35ticsg324-1L), which is specially designed to achieve optimum power performance. This FPGA fabric runs on the 0.95 volts supply, which saves around 30% power compared with normal Artix-7 devices [35]. As shown in Table 4, the total FPGA power consumption of complete test design is 241 mill watts out of which 120 mill watts is consumed by MLP IP core. The comparison shows that the performance of MLP IP core is best among other works in terms of time and power.

VI. CONCLUSION

In this paper, we proposed hardware implementation of the MLP classifier for activity classification in smart military wearables. The simulation results prove that the MLP design with 7-6-5 topology gives maximum classification accuracy. The five variants of final MLP designs (7-6-5) with different data precision implemented on the Xilinx Artix-7 FPGA. In which, the classification accuracy of the MLP model with the 24, 20, 16 bits precision is almost constant, below 16-bit it starts decaying. The collective analysis shows that the reduction in resource utilization and power consumption without compromising of the classification accuracy is achievable by reducing the perceptrons IO precision. 0.9% to 3.33% classification accuracy reduction have been observed between simulation and hardware testing results. It is mainly because

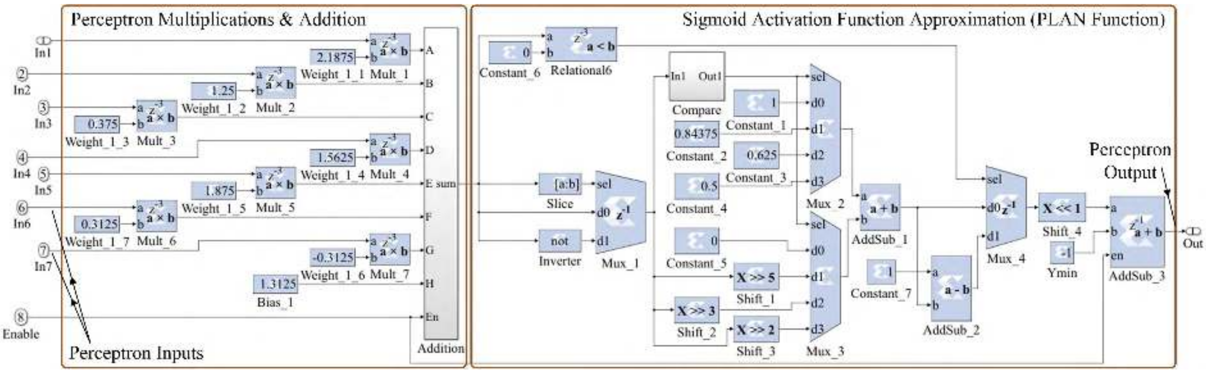


FIGURE 10. Xilinx system generator design of a perceptron.

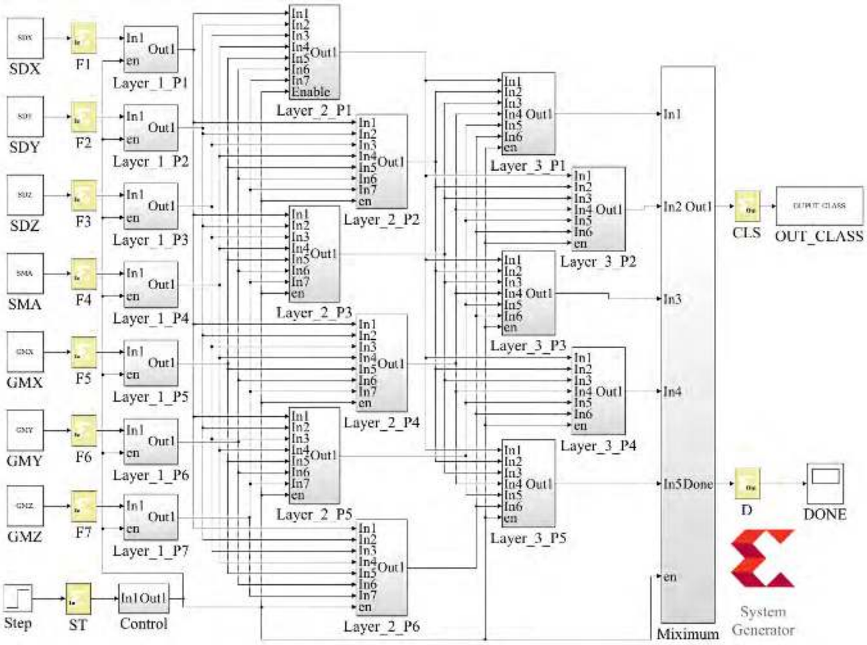


FIGURE 11. Xilinx system generator design of MLP classifier.

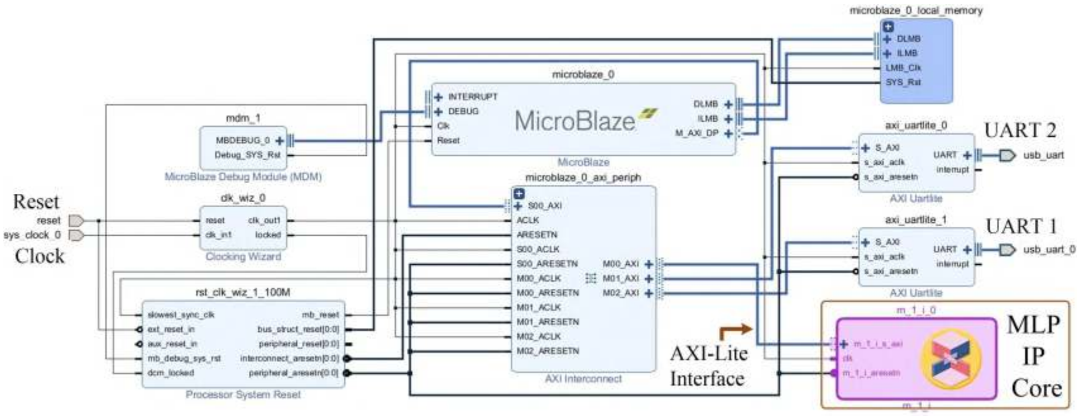


FIGURE 12. Vivado IP integrator design of microblaze based MLP IP test system.

of data format switching (Floating point to fixed point) and sigmoid function approximation.

The implementation result shows that the MLP design with 16-bit fixed-point data precision is the most efficient MLP design in the context of classification accuracy, latency, power consumption and resource utilization. This MLP design requires only 270 nanoseconds for classification using 120 mill watts of dynamic power. The classification accuracy of the proposed HAR classifier is greater among many HAR implementations reported in the literature. Moreover, the proposed MLP classifier outperforms the recently reported FPGA based MLP design in terms of the classification time and power consumptions.

The presented work can be further extended to implement on-chip learning in the hardware that can be integrated into an on-line training hardware of the smart suit. Some of the extra essential output classes also can be easily incorporated into the hardware design due to the flexibility offered by this design.

APPENDIX A
DATASET DESCRIPTION

See Table 5.

APPENDIX B
FPGA IMPLEMENTATION DESIGNS

See Figures 10–12.

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REFERENCES

[1] O. D. Lara and M. A. Labrador, "A survey on human activity recognition using wearable sensors," *IEEE Commun. Surveys Tuts.*, vol. 15, no. 3, pp. 1192–1209, 3rd Quart., 2013.

[2] M. Cornacchia, K. Ozcan, Y. Zheng, and S. Velipasalar, "A survey on activity detection and classification using wearable sensors," *IEEE Sensors J.*, vol. 17, no. 2, pp. 386–403, Jan. 2017.

[3] D. Riboni and C. Bettini, "COSAR: Hybrid reasoning for context-aware activity recognition," *Pers. Ubiquitous Comput.*, vol. 15, no. 3, pp. 271–289, Mar. 2010.

[4] E. Mitchell, D. Monaghan, and N. E. O'Connor, "Classification of sporting activities using smartphone accelerometers," *Sensors*, vol. 13, no. 4, pp. 5317–5337, 2013.

[5] J. Morales and D. Akopian, "Physical activity recognition by smartphones, a survey," *Biocybern. Biomed. Eng.*, vol. 37, no. 3, pp. 388–400, 2017.

[6] S. Leonhardt, T. Falck, and P. Mähönen, *4th International Workshop on Wearable and Implantable Body Sensor Networks (BSN 2007): March 26-28, 2007 RWTH Aachen University, Germany*, vol. 13. Berlin, Germany: Springer, Mar. 2007.

[7] H. Wei, J. He, and J. Tan, "Layered hidden Markov models for real-time daily activity monitoring using body sensor networks," *Knowl. Inf. Syst.*, vol. 29, no. 2, pp. 479–494, 2011.

[8] J. Andreu and P. Angelov, "Real-time human activity recognition from wireless sensors using evolving fuzzy systems," in *Proc. IEEE Int. Conf. Fuzzy Syst. (FUZZ)*, Jul. 2010, pp. 1–8.

[9] W. Tang and E. S. Sazonov, "Highly accurate recognition of human postures and activities through classification with rejection," *IEEE J. Biomed. Health Inform.*, vol. 18, no. 1, pp. 309–315, Jan. 2014.

[10] P. Fraga-Lamas, T. M. Fernández-Caramés, M. Suárez-Albela, L. Castedo, and M. González-López, "A review on Internet of Things for defense and public safety," *Sensors*, vol. 16, no. 10, p. 1644, 2016.

[11] A. T. Özdemir and K. Dani man, "Fully parallel ANN-based arrhythmia classifier on a single-chip FPGA: FPAAC," *Turkish J. Elect. Eng. Comput. Sci.*, vol. 19, no. 4, pp. 667–687, 2011.

[12] I. Mellal, M. Laghrouche, and H. T. Bui, "Field programmable gate array (FPGA) respiratory monitoring system using a flow microsensor and an accelerometer," *Meas. Sci. Rev.*, vol. 17, no. 2, pp. 61–67, 2017.

[13] J. J. M. Nolasco and J. A. P. Medina, "LabVIEW-based classic, fuzzy and neural controllers algorithm design applied to a level control prototype," *IEEE Latin Amer. Trans.*, vol. 15, no. 6, pp. 1154–1162, Jun. 2017.

[14] H.-C. Huang and C.-H. Chiang, "An evolutionary radial basis function neural network with robust genetic-based immunecomputing for online tracking control of autonomous robots," *Neural Process. Lett.*, vol. 44, no. 1, pp. 19–35, 2016.

[15] W. Chine, A. Mellit, V. Lughi, A. Malek, G. Sulligoi, and A. M. Pavan, "A novel fault diagnosis technique for photovoltaic systems based on artificial neural networks," *Renew. Energy*, vol. 90, pp. 501–512, May 2016.

[16] D. Baptista, S. Abreu, C. Travieso-González, and F. Morgado-Dias, "Hardware implementation of an artificial neural network model to predict the energy production of a photovoltaic system," *Microprocess. Microsyst.*, vol. 49, pp. 77–86, Mar. 2017.

[17] A. R. Omondi and J. C. Rajapakse, *FPGA Implementations of Neural Networks*, vol. 365. Dordrecht, The Netherlands: Springer, 2006.

[18] J. Misra and I. Saha, "Artificial neural networks in hardware: A survey of two decades of progress," *Neurocomputing*, vol. 74, nos. 1–3, pp. 239–255, 2010.

[19] F. Benrekia, M. Attari, and M. Bouhedda, "Gas sensors characterization and multilayer perceptron (MLP) hardware implementation for gas identification using a field programmable gate array (FPGA)," *Sensors*, vol. 13, no. 3, pp. 2967–2985, 2013.

[20] X. Zhai, A. A. S. Ali, A. Amira, and F. Bensaali, "MLP neural network based gas classification system on Zynq SoC," *IEEE Access*, vol. 4, pp. 8138–8146, 2016.

[21] M. Bahoura, "FPGA implementation of blue whale calls classifier using high-level programming tool," *Electronics*, vol. 5, no. 1, p. 8, 2016.

[22] K. Basterretxea, J. Echanobe, and I. del Campo, "A wearable human activity recognition system on a chip," in *Proc. IEEE Conf. Design Archit. Signal Image Process. (DASIP)*, Oct. 2014, pp. 1–8.

[23] C. Rodriguez *et al.*, "IoT system for human activity recognition using BioHarness 3 and smartphone," in *Proc. Int. Conf. Future Netw. Distrib. Syst.*, 2017, p. 37.

[24] T. Zebin, P. J. Scully, and K. B. Ozanyan, "Evaluation of supervised classification algorithms for human activity recognition with inertial sensors," in *Proc. IEEE Sensors*, Oct. 2017, pp. 1–3.

[25] A. Tisan and J. Chin, "An end-user platform for FPGA-based design and rapid prototyping of feedforward artificial neural networks with on-chip backpropagation learning," *IEEE Trans. Ind. Informat.*, vol. 12, no. 3, pp. 1124–1133, Jun. 2016.

[26] University of Toronto, Toronto, ON, Canada. *Lecture by Geoffrey Hinton*. Accessed: Jun. 20, 2018. [Online]. Available: https://www.youtube.com/watch?v=mlaLLQofmR8

[27] J.-L. Reyes-Ortiz, L. Oneto, A. Samà, X. Parra, and D. Anguita, "Transition-aware human activity recognition using smartphones," *Neurocomputing*, vol. 171, pp. 754–767, Jan. 2016.

[28] V. S. Patil, Y. B. Mane, and S. Deshpande, "FPGA based power saving technique for sensor node in wireless sensor network (WSN)," in *Computational Intelligence in Sensor Networks*. Berlin, Germany: Springer, 2019, pp. 385–404.

[29] Z. Yan, X. Xu, G. Yu, and H. Yu, "Empowering edge mining on smartphones with reconfigurable fabrics," in *Proc. IEEE Semicond. Technol. Int. Conf. (CSTIC)*, Shanghai, China, Mar. 2018, pp. 1–3.

[30] D. Biswas *et al.*, "Real-time arm movement recognition using FPGA," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2015, pp. 766–769.

[31] M. Janidarmian, A. R. Fekr, K. Radecka, and Z. Zilic, "A comprehensive analysis on wearable acceleration sensors in human activity recognition," *Sensors*, vol. 17, no. 3, p. 529, 2017.

[32] Y. Chen and C. Shen, "Performance analysis of smartphone-sensor behavior for human activity recognition," *IEEE Access*, vol. 5, pp. 3095–3110, 2017.

[33] L. Sun, D. Zhang, B. Li, B. Guo, and S. Li, "Activity recognition on an accelerometer embedded mobile phone with varying positions and orientations," in *Proc. Int. Conf. Ubiquitous Intell. Comput.* Berlin, Germany: Springer, 2010, pp. 548–562.

[34] J. R. Kwapisz, G. M. Weiss, and S. A. Moore, "Activity recognition using cell phone accelerometers," *ACM SIGKDD Explorations Newslett.*, vol. 12, no. 2, pp. 74–82, Dec. 2010.

[35] Xilinx. *ARTY Power Demo, Artix-7-1LI 35T Device*. Accessed: Jun. 25, 2018. [Online]. Available: http://www.wiki.xilinx.com/ARTY+Power+Demo

[36] UCI Machine Learning Repository. *Smartphone-Based Recognition of Human Activities and Postural Transitions Data Set*. Accessed: May 5, 2018. [Online]. Available: https://archive.ics.uci.edu/ml/datasets.html

[37] V. Della Mea, O. Quattrin, and M. Parpinel, "A feasibility study on smartphone accelerometer-based recognition of household activities and influence of smartphone position," *Inform. Health Social Care*, vol. 42, no. 4, pp. 321–334, 2017.

[38] S.-M. Lee, S. M. Yoon, and H. Cho, "Human activity recognition from accelerometer data using convolutional neural network," in *Proc. IEEE Int. Conf. Big Data Smart Comput. (BigComp)*, Feb. 2017, pp. 131–134.

[39] F. Chamroukhi, S. Mohammed, D. Trabelsi, L. Oukhellou, and Y. Amirat, "Joint segmentation of multivariate time series with hidden process regression for human activity recognition," *Neurocomputing*, vol. 120, pp. 633–644, Nov. 2013.

[40] E. Ebrahimi, K. Mollazade, and A. Arefi, "An expert system for classification of potato tubers using image processing and artificial neural networks," *Int. J. Food Eng.*, vol. 8, no. 4, pp. 1–21, 2012.

[41] B. Vaferi, V. Gitifar, P. Darvishi, and D. Mowla, "Modeling and analysis of effective thermal conductivity of sandstone at high pressure and temperature using optimal artificial neural networks," *J. Petroleum Sci. Eng.*, vol. 119, pp. 69–78, Jul. 2014.

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