# Efficient Pattern Mapping for Deterministic Logic BIST

Valentin Gherman, Hans-Joachim Wunderlich
Universität Stuttgart
Pfaffenwaldring 47
D-70569 Stuttgart
Germany
ghermanv@informatik.uni-stuttgart.de
wu@informatik.uni-stuttgart.de

Harald Vranken
Philips Research
Prof. Holstlaan 4, WAY-41
5656 AA Eindhoven
The Netherlands
harald.vranken@philips.com

Friedrich Hapke, Michael Wittke
Philips Semiconductors
Georg-Heyken-Strasse 1
D-21147 Hamburg
Germany
friedrich.hapke@philips.com
michael.wittke@philips.com

## Abstract

Deterministic logic BIST (DLBIST) is an attractive test strategy, since it combines advantages of deterministic external testing and pseudo-random LBIST. Unfortunately, previously published DLBIST methods are unsuited for large ICs, since the computing time and memory consumption of the DLBIST synthesis algorithms increases expotentially, or at least cubically, with the circuit size. In this paper, we propose a novel DLBIST synthesis procedure that has nearly linear complexity in terms of both computing time and memory consumption. The new algorithms are based on binary decision diagrams (BDDs). We demonstrate the efficiency of the new algorithms for industrial designs up to 4M gates.

**Key words:** Logic BIST, BDDs.

## 1. Introduction

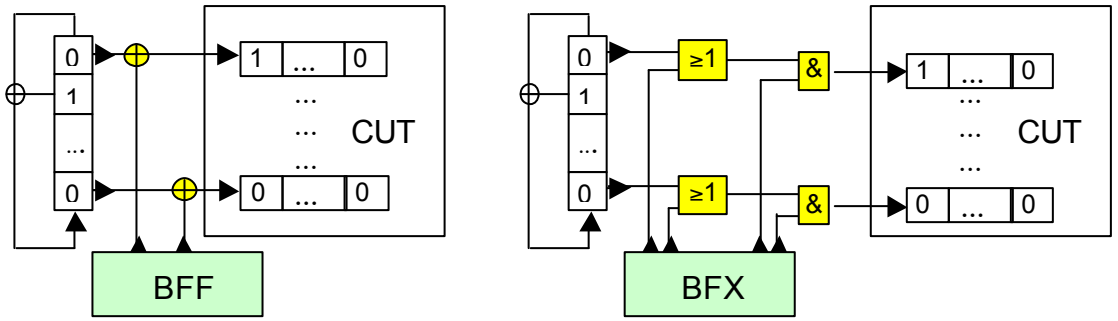
Logic Built-In Self-Test (LBIST) for random logic is becoming an attractive alternative in IC testing. Recent advances in nanometer IC process technology and core-based IC design are leading to more widespread use of LBIST since external testing is becoming more and more difficult and costly. Also requirements on in-field testing and limited access into ICs that contain secure information, are demanding LBIST solutions.

There is a wide range of deterministic logic BIST methods that apply deterministic test patterns and hence improve the low fault coverage often obtained by pseudo-random patterns. Straightforward is the application of additional external deterministic patterns on top of the pseudo-random test [8]. Unfortunately, the very last percentages of fault coverage require the largest amount of deterministic patterns, so the benefits of LBIST are severely reduced by this approach.

More efficient are compression and decompression methods, where a small amount of external test data is continuously fed into the circuit [9][10]. However, this approach is no longer a BIST method; it requires still external ATE and looses some benefits of BIST like in-field testing. An alternative for increasing the fault coverage is inserting test points, which has been proposed for both LBIST and external testing [4][5][11][17]. While the area increase due to test points may be tolerable, they may also introduce additional delays, which could require complete resynthesis and new timing verification. In contrast to the abovementioned LBIST methods, pure deterministic LBIST schemes try to avoid both modifying the core under test (CUT) and applying additional patterns. Their underlying methods can be classified into "store and generate" schemes and "test set embedding" schemes [14].

"Store and generate" schemes consist of hardware structures which store the test patterns on-chip in a compressed form and implement an algorithm for decompression. Widely known representatives of this method are LFSR-reseeding [9], multi-polynomial reseeding [6] and folding counter based-LBIST [7].

"Test set embedding" schemes rely on a pseudo-random test pattern generator plus some additional circuitry that modifies the pseudo-random sequence in such a way that a set of deterministic patterns is embedded. Widely known techniques are bit-flipping [13] and bit-fixing [12]. In the bit-flipping




(a) (b)

**Figure 1:** (a) Bit-flipping and (b) bit-fixing BIST schemes.

approach, the output sequences of an LFSR are inverted at a few bit positions in order to increase fault coverage (Figure 1.a), while the bit-fixing approach applies constant values (Figure 1.b). The test generation process is controlled by a bit-flipping function (BFF) or a bit-fixing function (BFX), respectively.

We use the term *pattern mapping* for referring to the embedding of a set of deterministic patterns into a sequence of pseudo-random patterns. A DLBIST synthesis procedure consists of pattern mapping and generation of the hardware structure to implement the mapping, e.g. by means of a BFF or BFX. The synthesis procedure for generating the BFX as published in [12], is based on rectangle covering, while the synthesis procedure for generating the BFF as published in [13], is based on manipulating sets of test cubes. In both cases, the procedures are based on heuristics that generally require at least cubical, but often exponential, effort in terms of memory consumption and computing time.

In this paper, we present a BDD-based algorithm for test pattern mapping that outperforms previously published algorithms by several orders of magnitude.

## 2. The pattern mapping problem

The "test set embedding" schemes provide both pseudo-random and deterministic test stimuli. Usually, some of the pseudo-random patterns generated by an LFSR, are altered into deterministic test stimuli. Most of the pseudo-random test patterns do not contribute to the fault coverage, since they only detect faults that already were detected by other pseudo-random patterns. Such *useless* pseudo-random test patterns may therefore be skipped or modified in any arbitrary way. The key idea is to modify some useless pseudo-random patterns into useful deterministic test patterns to improve the fault coverage. The deterministic test patterns are determined by an ATPG tool, and they target those faults that are not detected by pseudo-random test stimuli. In such a deterministic test pattern, only few bits are actually specified, while most of the bits are don't care and hence can arbitrarily be set to 0 or 1.

The method presented here can be applied to both the bit-flipping and bit-fixing approach, assuming a few modifications. For the sake of simplicity, we will explain the method by using the bit-flipping approach; also the experimental results are given for this method. In the bit-flipping approach, the modification of the pseudo-random patterns is realized by inverting *(flipping)* some of the LFSR outputs, such that the deterministic stimuli are obtained. The flipping is implemented by combinational logic, called bit-flipping function (BFF). The BFF can be kept quite small by exploiting the large number of useless pseudo-random test patterns that may be modified, and carefully selecting the pseudo-random test patterns on which deterministic test patterns are mapped.

As shown in Figure 2, the BFF inputs are connected to the LFSR, the pattern counter, and the shift counter, while the BFF outputs are connected to the XOR-gates at the scan inputs. The BFF determines whether a bit has to be flipped based on the states of the LFSR the pattern counter (PC), and the shift counter (SC). The PC is part of the test control unit, and counts the number of test patterns applied during the self-test. The SC

is also part of the test control unit, and counts the number of scan shift cycles for shifting data in/out the scan chains.

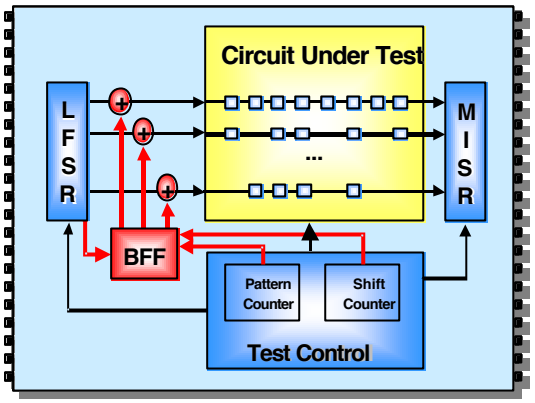



**Figure 2**: Bit-flipping DLBIST architecture.

The BFF realizes the mapping of deterministic test stimuli to pseudo-random test stimuli. Every specified bit (i.e. care bit) in a deterministic pattern either matches to the corresponding bit in the pseudo-random stimulus, in which case no bit-flipping is required, or the bit does not match, in which case bit-flipping is required. For all unspecified bits (i.e. don't-care bits) in the deterministic pattern, the corresponding bits in the pseudo-random stimulus may be arbitrarily flipped or not. The BFF should provide that (1) all conflicting bits are flipped, (2) all matching bits are not flipped while (3) the don't-care bits may be arbitrarily flipped or not.

We first consider a CUT with a single scan chain. The LFSR generates a pseudo-random sequence of test stimuli that is shifted into the scan chain. The LFSR and SC are updated in every clock cycle, while the PC is updated when applying a new test pattern. In every clock cycle, the DLBIST hardware therefore has a unique state identified by the states of the LFSR, PC, and SC. In principle, the states of the PC and SC are already sufficient to uniquely identify a bit in the pseudo-random LFSR sequence. The LFSR states add redundant information, which however may be exploited for further logic optimization of the BFF.

The *on-set* is the set of LFSR+PC+SC states that correspond to the clock cycles in which the pseudo-random LFSR output should be flipped. Similarly, the *off-set* is the set of LFSR+PC+SC states that correspond to clock cycles in which the pseudo-random LFSR output should not be flipped. The *dc-set* is the set of LFSR +PC+SC states that correspond to clock cycles in which the pseudo-random LFSR output may be arbitrarily flipped or not. The *on-set* and *off-set* are disjoint. The *dc-set* contains all states that are not in the union of the *on-set* and *off-set* and is exploited to minimize the logic implementation of the BFF. The size of the *on-set* and *off-set* increases with the number of specified bits and in contrast to standard logic synthesis problems, the cubes in these sets are very irregular. Hence, logic minimization exploiting the *on-set*, *off-set* and *dc-set*, may have exponential complexity in terms of the number of specified bits.

In case of a CUT with multiple scan chains, there are separate on-sets, off-sets, and dc-sets associated with each scan chain. For a CUT with $n$ scan chains, the BFF now consists of the $n$ bit-flipping logics $BFF_i$ for each scan chain. The size of the BFF implementation can be minimized by sharing logic between the $BFF_i$ for various scan chains.

## 3. BDD-based pattern mapping

A binary decision diagram (BDD) is a well-known representation of a logic function [1]. A BDD is a tree-like directed graph, starting from a root vertex. A BDD contains non-terminal vertices that have two outgoing edges, and terminal vertices that only have incoming edges. For example, Figure 3 shows the BDD representation of a parity function. A second advantage of BDDs is that the complexity of many operations on a BDD scales linearly with the number of input variables [2].

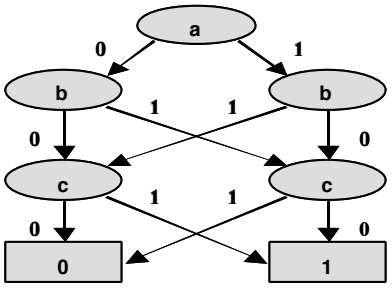



**Figure 3:** BDD representation of parity function.

In the BDD-based bit-flipping synthesis procedure, the *on-set* and *off-set* of the BFF are represented by characteristic functions, the *on-BDD* and the *off-BDD*. The on-BDD will output the value '1' if the input is taken from the on-set, otherwise the output is '0'. Similarly, the off-BDD will output '1', only if the input is selected from the off-set. Checking whether an assignment is element of the off-set or the on-set is linear in the number of input variables of the BDD, whereas the cubical representation requires an effort linear in the cardinality of the sets.

In the presented approach, the sequence of test stimuli is partitioned into two parts. The first part of the sequence is used only for pseudo-random fault detection, and no deterministic stimuli are embedded into this part. The outputs of the BFF should be disabled during this part. The LFSR+PC+SC states for this first part of pseudo-random test stimuli are included in the *dc-set*, since increasing the *dc-set* gives more room for logic optimization of the BFF. However, the BFF will arbitrarily flip some pseudo-random pattern-bits, and some detected faults may no longer be detected by the modified sequence with bit-flipping. In general, most pseudo-random detectable faults are quickly detected by the first few hundreds or thousands pseudo-random test patterns. Disabling the BFF can be achieved using some simple additional circuitry that considers the most significant bits of the PC.

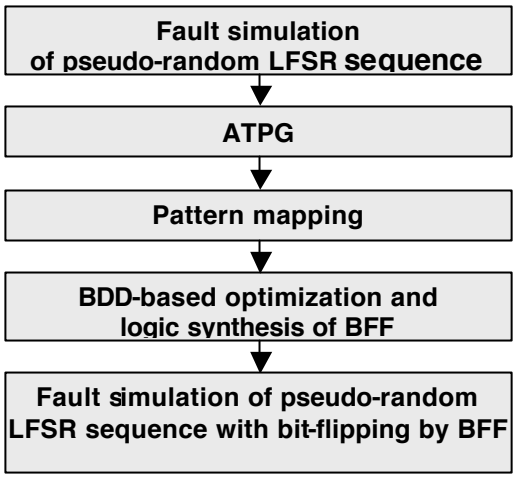



**Figure 4:** Bit-flipping synthesis procedure.

All deterministic patterns are embedded into the second part of the sequence, during which the BFF is enabled. The second part usually is 1/2, 1/4, or 1/8 of the total test sequence.

The BDD-based bit-flipping synthesis procedure is outlined in Figure 4.

## 4. Experimental results

Below, experiments are reported performed on Linux GNU machines equipped with one GB of memory and an AMD Atlon-XP processor running at 1500 MHz. The BDD-based computations were implemented using the *CUDD* package [15].

The benchmark circuits are industrial designs described in Table 1. The first column reports the circuit name encoded like *pN*, where *N* denotes the number of gates in the circuit, while the second column gives the number of scan flip-flops contained in each design. The last two columns report the fault coverage and the fault efficiency obtained after applying 10,000 pseudo-random patterns, which are the percentage of detected faults, respectively, the percentage of detected, redundant and not testable faults, with respect to the total number of faults.

While the original cube-based pattern mapping is an iterative algorithm [13], where ATPG, pattern mapping and fault simulation are alternating, the BDD-based algorithm is a single pass algorithm, which involves ATPG and fault simulation less often. This is also a consequence of the better algorithmic properties and compactness of the BDD-based representation, which allow on optimization of the BFF implementation that doesn't need iterative algorithms. Hence computing time savings are not only due to substituting the cubical calculus by BDD-based algorithms, also for ATPG and fault simulation computing time is saved.

Table 2 shows that mapping time is reduced from several days down to a few minutes, and that also the other tasks have significant improvements. The overall computing time and the memory consumption is seen in Table 3. The BDD-based approach reduces computing time from more than a week down to a few hours, while also the memory requirements scale quite well with the circuit size.

| Design | # Flip-flops | Random fault coverage [%] | Random fault efficiency [%] |
|---|---|---|---|
| p19k | 1407 | 63.11 | 71.68 |
| p59k | 4730 | 87.30 | 97.30 |
| p127k | 5116 | 82.14 | 84.30 |
| p278k | 9967 | 79.92 | 81.61 |
| p333k | 20756 | 93.64 | 95.65 |
| p951k | 104624 | 92.91 | 92.92 |

**Table 1:** Benchmark characteristics.

Finally, the amazing improvements should not be paid by less quality in terms of fault efficiency and hardware overhead. Table 4 reports the fault efficiencies obtained in both cases. In order to have comparable results of time and memory, the fault efficiency of the BDD-based approach was limited to the one reached by the cube-based approach. By spending more resources, even higher fault efficiency could be obtained, only limited by the resources given to the ATPG tool. The last column (*Cell area*) shows the logic overhead of the BFF implementation relative to the cell area of the CUT, obtained using a commercial synthesis tool and a proprietary library. Again, the BDD-based approach outperforms the cubical calculus.

The last design from Table 1 does not appear in Table 2, 3 and 4 because it was just too large for being subject of experiments done with the cube-based representation. During the generation of the BDD-based representation, no static or dynamic variable reordering was used. The variables were a priori and optimally arranged in groups corresponding to the states of the LFSR, PC and SC. The reported experimental results are obtained with the same variable order for all the designs.

Table 5 illustrates how the computational resources are scaling when the targeted fault efficiency is increased to levels close to the maximum allowed by the ATPG tool. Most of the additional run-time is consumed generating deterministic patterns, while the time spent for fault simulation remains constant. These final fault efficiencies are practically not reachable by the cube-based approach in the case of the last four designs. The figures reported in the last column (*Cell area*) are just giving the logic overhead of the BFF implementation; the overhead of the other parts of the DLBIST hardware may be neglected. Table 5 also shows that the overhead decreases significantly for the larger design. The presented approach does not only scale very well in terms of run-time and memory, but also in terms of area overhead.

## 5. Conclusions

A new pattern mapping algorithm for "test set embedding" deterministic BIST schemes was proposed which exploits standard BDD operations. This way, improvements of several order of magnitude are obtainable compared with the cube-based approach, e.g., in terms of both run-time and memory requirements. With this approach, computing and memory resources for DLBIST synthesis are in the same order of complexity as the resources required for ATPG or fault simulation. The gains of efficiency can also be used to obtain even better solutions in terms of hardware overhead and fault coverage.


## Acknowledgment

This research work was supported by the German Federal Ministry of Education and Research (BMBF) in the Project AZTEKE under the contract number 01M3063C.


| | Cube-based | | | BDD-based | | |
|---|---|---|---|---|---|---|
| Design | ATPG time [h:m] | Mapping time [h:m] | Fault simulation time [h:m] | ATPG time [h:m] | Mapping time [h:m] | Fault simulation time [h:m] |
| p19k | 00:12 | 02:48 | 00:52 | 00:00 | 00:02 | 00:01 |
| p59k | 00:15 | 01:50 | 00:29 | 00:01 | 00:02 | 00:03 |
| p127k | 02:19 | 74:28 | 20:38 | 03:49 | 00:12 | 00:11 |
| p278k | 05:20 | 193:10 | 37:23 | 01:59 | 00:06 | 00:21 |
| p333k | 06:46 | 88:16 | 44:31 | 00:37 | 00:11 | 00:17 |

**Table 2:** Computing time for the different tasks of the cube-based and BDD-based algorithm.

| | Cube-based | | BDD-based | |
|---|---|---|---|---|
| Design | Total time [h:m] | Total memory [MB] | Total time [h:m] | Total memory [MB] |
| p19k | 03:52 | 47 | 00:07 | 22 |
| p59k | 02:34 | 114 | 00:08 | 34 |
| p127k | 97:25 | 382 | 04:40 | 94 |
| p278k | 235:53 | 400 | 02:52 | 111 |
| p333k | 139:33 | 529 | 01:21 | 147 |

**Table 3:** Run-time and memory consumption of the cube-based and BDD-based algorithm.

| | Cube-based | | BDD-based | |
|---|---|---|---|---|
| Design | Fault efficiency [%] | Cell area [%] | Fault efficiency [%] | Cell area [%] |
| p19k | 96.87 | 25.26 | 97:55 | 6.95 |
| p59k | 99.06 | 27.12 | 99.17 | 14.09 |
| p127k | 94.67 | 27.86 | 95.82 | 12.83 |
| p278k | 90.83 | 25.77 | 91.56 | 15.49 |
| p333k | 97.46 | 12.07 | 97.56 | 4.04 |

**Table 4:** Fault efficiency and logic overhead of the cube-based and BDD-based algorithm.

| Design | # Embedded patterns | Fault efficiency [%] | Run-time [h:m] | Memory [MB] | Cell area [%] |
|---|---|---|---|---|---|
| p19k | 237 | 99.99 | 00:10 | 29 | 10.38 |
| p59k | 137 | 99.19 | 00:08 | 35 | 14.32 |
| p127k | 761 | 99.79 | 10:41 | 208 | 31.11 |
| p278k | 1894 | 99.33 | 26:29 | 329 | 38.95 |
| p333k | 1396 | 99.53 | 03:12 | 246 | 9.12 |
| p951k | 259 | 99.67 | 14:22 | 666 | 1.49 |

**Table 5:** Performance of the BDD-based approach when the fault efficiency is close to 100%.

## References


[1] S.B. Akers „Binary Decision Diagrams," *IEEE Transactions on Computers*, Vol. C-27, No. 6, June 1978, pp. 509-516.

[2] R.E. Bryant „Graph-Based Algorithms for Boolean Function Manipulation," *IEEE Transactions on Computers*, C-35-8, August 1986, pp. 677-691.

[3] R.K. Brayton, G.D. Hachtel, C.T. McMullen and A.L. Sangiovanni-Vincentelli „Logic Minimization Algorithms for VLSI Synthesis," *Kluver Academic Publishers*, 1997.

[4] M.J. Geuzebroek, J.Th. van der Linden, A.J. van de Goor „Test Point Insertion for Compact Test Sets," *Proceedings of International Test Conference*, IEEE, 2000, pp. 506-514.

[5] J.P. Hayes, A.D. Friedman „Test Point Placement to Simplify Fault Detection," *IEEE Transactions on Computers*, Vol. C-33, July 1974, pp. 727-735.

[6] S. Hellebrand, S. Tarnik, J. Rajski, B. Courtois „Generation of Vector Patterns Through Reseeding of Multiple-Polynomial Linear Feedback Shift Registers," *Proceedings of International Test Conference*, 1992, pp. 120-129.

[7] H. Liang, S. Hellebrand, H.-J. Wunderlich „Two-Dimensional Test Data Compression for Scan-Based Deterministic BIST," *Proceedings IEEE International Test Conference*, *Journal of Electronic Testing - Theory and Applications (JETTA)*, Vol. 18, No. 2, April 2002, pp. 157-168.

[8] G. Hetherington, T. Fryars, N. Tamarapalli, M. Kassab, A. Hassan, J. Rajski „Logic BIST for Large Industrial Designs: Real Issues and Case Studies," *Proceedings of International Test Conference*, IEEE, 1999, pp. 358-367.

[9] B. Koenemann „LFSR-Coded Test Patterns for Scan Designs," *Proceedings of European Test Conference*, 1991, pp. 237-242.

[10] J. Rajski, J. Tyszer, M. Kassab, N. Mukherjee, R. Thompson, K.-H. Tsai, A. Hertwig, N. Tamarapalli, G. Mrugalski, G. Eide, J. Qian „Embedded deterministic test for low cost manufacturing test", Proceedings of *International Test Conference*, IEEE, 2002, pp. 301-310.

[11] B. H. Seiß, P. M. Trouborst and M. H. Schulz „Test Point Insertion for Scan-Based BIST," *European Test Conference* (ETC), April 1991, pp. 253-262.

[12] N. A. Touba, and E. J. McCluskey „Altering a pseudo random bit sequence for scan-based BIST," *Proceedings IEEE International Test Conference*, 1996, pp.167-175.

[13] H.-J. Wunderlich, G. Kiefer „Bit-Flipping BIST," *Proceedings International Conference on Computer Aided Design*, IEEE, 1996, pp. 337-343.

[14] H.-J. Wunderlich „BIST for Systems-on-a-Chip," *INTEGRATION*, the VLSI journal, 1998, pp. 57-78.

[15] http://vlsi.colorado.edu/~fabio/CUDD/cuddIntro.html