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## Electret mechanism, hysteresis, and ambient performance of sol-gel silica gate dielectrics in pentacene field-effect transistors

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The electret induced hysteresis was studied in sol-gel silica films that result in higher drain currents and improved device performance in pentacene field-effect transistors. Vacuum and ambient condition studies of the hysteresis behavior and capacitance-voltage characteristics on single layer and varying thicknesses of bilayer dielectrics confirmed that blocking layers of thermal oxide could effectively eliminate the electret induced hysteresis, and that thin (25 nm) sol-gel silica dielectrics enabled elimination of nanopores thus realizing stable device characteristics under ambient conditions. © 2007 American Institute of Physics. [DOI: 10.1063/1.2821377]

Printed electronic circuits comprising organic field-effect transistors (OFETs) are of great interest in applications ranging from identification tags to switching devices for active-matrix displays.<sup>1-4</sup> Improvement of organic semiconductors, typically benchmarked by transport mobilities, has continued to be the major focus of research efforts. Although it has been recognized that the semiconductor-dielectric interfacial interactions critically influence mobility,<sup>5</sup> hysteresis,<sup>6</sup> and threshold voltage ( $V_{th}$ );<sup>7</sup> the bulk effects of dielectric films, unlike those in silicon microelectronics, have not been adequately studied.

The performance of dielectrics in ambient conditions and the influence of moisture on dielectrics are important considerations in their study as suitable dielectrics. The influence of moisture has been documented in dielectrics such as poly(4-vinylphenol) (PVP) and poly(vinyl alcohol) (PVA). The hydroxyl (-OH) groups within PVP/PVA films or moisture has been linked to its large hysteresis<sup>8,9</sup> and increase in drain currents related to polarization in the dielectric.<sup>10</sup> The influence of -OH groups and the effect of moisture have also been reported in inorganic<sup>11</sup>/organic-inorganic hybrid<sup>6</sup> gate dielectrics with high polarizability (or high dielectric constant,  $k$ ), that results in hysteresis and negative  $V_{th}$  shift.<sup>5</sup> Low temperature (60–100 °C), solution processed sol-gel deposited high  $k$  silica dielectrics with improved  $V_{th}$ , mobilities, high drain currents at low voltages have been recently reported.<sup>12</sup> In the polymer, inorganic, as well as the hybrid dielectric film based OFETs, hysteresis is believed to be re-

lated to electron injection from the gate to-OH groups; however, the extrinsic origin of charge trapping for an enlarged hysteresis,  $V_{th}$  instabilities, and higher off current in ambient air is far from understood.<sup>11,13,14</sup>

In this work, the effect of -OH groups and moisture on the electrical performances of pentacene OFETs with sol-gel (SG) silica film in single and bilayer dielectric systems are studied in vacuum/ambient conditions so as to investigate their charge trapping mechanism and ambient moisture effects.

SG silica solution was prepared by a two-step acid-base catalyst procedure by mixing tetraethylorthosilicate (TEOS), ethanol, water, and HCl in the following molar ratios: 1:10:3.5:0.003. After stirring at room temperature for 90 min, three drops of the base catalyst (0.1M NH<sub>4</sub>OH) was then added into the solution. The 3 day aged solution, under constant stirring at room temperature, was then spin coated (2000 rpm) to form ~330 nm thick film on blank  $n$ -type Si wafer as the single layer dielectric and on thermally grown SiO<sub>2</sub> (TOX) as the bilayer dielectric [Fig. 1(a)]. Sol-gel silica solution, diluted by 90% by  $w/w$  ethanol, was also used to deposit ~25 nm SG silica film in the bilayer dielectric structure. The SG silica films were dried at ambient conditions at 60 °C and were further heated at 100 °C, 10<sup>-7</sup> mbar prior to pentacene deposition. A 50 nm film of pentacene was evaporated at 0.5 Å/s under a vacuum of 10<sup>-7</sup> mbar at a substrate temperature of 100 °C. Gold source and drain layers were patterned using a shadow mask. All electrical measurements were done with a Keithley 4200 semiconductor parameter analyzer in a Desert Cryogenics probe station at a base pressure of 5 × 10<sup>-5</sup> mbar and were also characterized in ambient air (~23 °C and 70%–80% relative humidity).

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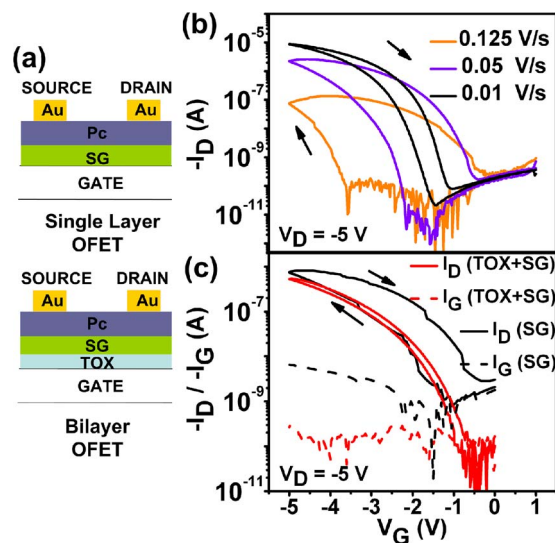


FIG. 1. (Color online) (a) Schematic structures of single and bilayer dielectric pentacene FETs. (b) The single layer (330 nm SG silica film) FET showed sweeping rate dependent hysteresis, lesser hysteresis with slower sweeping rates. (c) Transfer characteristics of FETs with and without 18 nm TOX as the blocking layer between gate and 330 nm SG silica film (measured with sweeping rate of 0.01 V/s).  $I_G$  was measured separately, while  $V_G$  was biased from 0 to  $-5$  V with  $V_D$  and  $V_S$  were grounded.

The transfer characteristics of the device with the 330 nm SG silica film (single layer dielectric), measured in vacuum, exhibit a metastable clockwise hysteresis [Fig. 1(b)]. The hysteresis and drain currents of the devices are significantly influenced by the sweeping rates. With the sweeping rate decreasing from 0.125 to 0.01 V/s, a significant decrease in hysteresis whereas an increase in the maximum drain current ( $I_{on}$ ) was observed. The origins of these observations may be related to trapping of electrons injected from the gate (space-charge electret)<sup>15</sup> or polarization of the dielectric (dipolar electret)<sup>16</sup>.

To confirm the mechanism responsible for the hysteresis and  $I_{on}$  change, a thermally grown  $\text{SiO}_2$  (TOX) layer was introduced underneath the 330 nm SG silica film to form the bilayer dielectric. If the origin of the hysteresis was related to dipolar electrets, the bilayer dielectric FET would still show the clockwise hysteresis because the TOX would not affect the interaction of the polarization field with the pentacene channel as it was located beneath the SG silica film. However, as evidenced by Fig. 1(c), the introduction of TOX all but suppresses the hysteresis in the bilayer FETs. This observation verifies that the cause of the clockwise hysteresis is related to space-charge electret creation as electrons from the Si gate are injected into the SG silica film; thus leading to charge storage within the SG silica bulk film.<sup>13,15</sup> The charge trapping mechanism was further examined by its capacitance-voltage ( $C_i$ -V) characteristics (not shown here) in the metal-insulator-semiconductor (MIS) configuration on  $n$ -type Si wafer. Similar to the observations in the  $I_D$ - $V_G$  characteristics [Figs. 1(b) and 1(c)], the single layer sol-gel dielectric displays a positive threshold voltage ( $V_{th}$ ) shift in the MIS  $C_i$ -V scans; further suggesting the existence of negative oxide charge present in the SG silica film. In contrast, the bilayer dielectric MIS capacitor exhibits negligible hysteresis, similar to the transfer characteristics, as seen in Fig. 1(c).

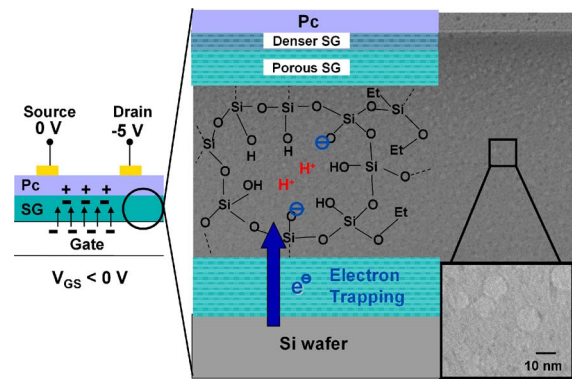


FIG. 2. (Color online) Schematic cross section of an organic thin film transistor with sol-gel silica as the dielectric. The minus signs represent volume charges injected and trapped into sol-gel silica from the gate. The plus signs represent the induced positive charges accumulated at the semiconductor interface. The electron trapping results in  $\text{H}^+$ . The upper part of sol-gel silica has denser structure, thus containing less moisture/ $-\text{OH}$  bonds.

Furthermore, Fig. 1(c) shows that the forward bias characteristics for both devices remain the same although the  $I_{on}/I_{off}$  increases with the bilayer dielectric, signifying a bulk rather than interface (dielectric-semiconductor) trap phenomenon.<sup>17</sup> The change in  $I_{on}/I_{off}$  could be attributed to the decrease in the gate leakage current ( $I_G$ ) with TOX as the blocking layer [Fig. 1(c)]. There is also slight decrease in the  $I_{on}$  of bilayer dielectric FET, thus the hole mobility ( $\mu_h = 0.67 \text{ cm}^2/\text{V s}$ ) for bilayer dielectric was calculated to be lower than that of the single layer dielectric ( $\mu_h = 2.08 \text{ cm}^2/\text{V s}$ ). However, its lower effective capacitance per unit area ( $C_i = 16.3 \text{ nF}/\text{cm}^2$  for bilayer dielectric, compared to  $C_i = 29.3 \text{ nF}/\text{cm}^2$  for single layer dielectric), due to absence of the space-charge electret field and thicker gate dielectric, along with the low gate leakage current, is recognized to make significant contribution to this reduced hole mobility.

Sol-gel silica films are known to trap moisture in nanopores inside its bulk<sup>18</sup> ensuing in higher  $k$  values compared with TOX.<sup>12</sup> Cross-sectional transmission electron microscopy (TEM) observations reveal the presence of these nanopores ( $\sim 10$ – $12$  nm in diameter) and also a denser silica layer on its surface (Fig. 2). The  $-\text{OH}$  groups contained in the nanopores near the Si substrate interact with the high electron density, resulting from the negative gate bias voltage, and form electron trapping centers creating charge electrets, as illustrated in Fig. 2. Similar to the mechanism in Si FETs, these charge traps, which may be referred to as border traps, are spatially separated from the Si/SG silica film interface but are close enough to exchange charge with the underlying Si gate. These respond slowly to the applied voltage sweep<sup>19</sup> and thus result in the sweep rate dependent transfer characteristics [Fig. 1(b)].

From the transfer characteristics measured under ambient conditions [Fig. 3(a)], the 330 nm SG silica bilayer dielectric device is always on and could not be turned off, even upon application of  $V_G$  up to  $+20$  V. This could be due to the moisture and hydrogenous species in the ambient, verified from dry/wet  $\text{N}_2$  ambient measurements (data not included here). Akin to the extrinsic source of the space-charge electret formation, moisture may lead to the formation of  $\text{SiOH}$  ( $\text{Si}-\text{O}-\text{Si}+\text{H}_2\text{O} \leftrightarrow 2\text{SiOH}$ ) species under the influence of an electric field.<sup>20</sup> These reversible moisture effects, which have

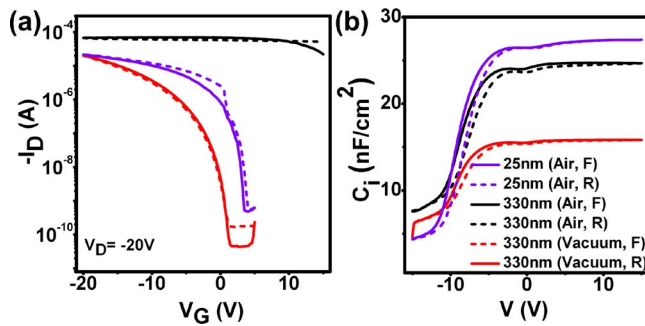


FIG. 3. (Color online) (a) Transfer characteristics of bilayer dielectric pentacene OFET in ambient and vacuum. This phenomenon is reversible upon repeated measurements between ambient and vacuum for thick SG silica film (330 nm) on 80 nm TOX. The ambient stability is improved with thinner SG silica film (25 nm). (b) Capacitance-voltage ( $C_i$ - $V$ ) characteristics of MIS on  $n$ -type Si wafer for bilayer structure with thick SG silica (330 nm) and thin SG silica (25 nm), measured at  $f=100$  kHz. (Note: F=forward, R=reverse.)

also been reported in the PVP film,<sup>8,10</sup> could be illustrated from its significantly higher capacitances of the 330 nm bilayer dielectric, in ambient conditions [Fig. 3(b)]. The increase in  $k$  of the SG silica film from  $k \sim 10$  in vacuum to  $k \sim 21.5$  in ambient likewise signifies that dipolar polarization of the water molecules in SG silica is very fast and responds readily to the measuring frequency. Moreover, the hysteresis of  $C_i$ - $V$  characteristics is negligible, suggesting that there are negligible interfacial traps or the traps are shallow in nature, responding very fast to the measuring frequency.

Standard transfer characteristics, including a high on/off ratio in ambient conditions, was brought about in the bilayer FETs by resorting to a SG silica thickness of 25 nm. Thinner SG silica results in a negligible nanoporous SG silica bulk layer while retaining the same denser silica skin layer on its surface, yielding a lower  $k$  value of  $\sim 4.5$ . However, it could also be observed that there is a slight increase in  $I_{on}$  and  $I_{off}$ ; and positive  $V_{th}$  shift, compared to the 330 nm SG silica bilayer FET measured in vacuum. This could be ascribed to the higher  $C_i$  ( $\propto 1/d$ ) and the reduced charge electrets in the thin nanoporous SG silica layer. The ability of these devices to operate in ambient also confirms a strong reversible hydrolysis and electrostatic charging effect rather than an electrochemical doping mechanism recently reported in polymer electrolytes.<sup>21</sup>

In summary, we have investigated the electret effect in SG silica dielectric films in pentacene FETs. Studies with cross-sectional TEM and with a blocking layer consisting of thermally grown oxide confirmed that the electret mechanism is related to electron injection into the hydroxyl groups

contained within the nanopores of the SG silica film. The SG silica bilayer film undergoes a reversible hydrolysis reaction in ambient and, as a result, there is an always on characteristics for these devices. Thin SG silica films (25 nm) eliminate the nanoporous hygroscopic regions of the films while facilitating the use of these dielectrics in printed electronic applications as interface layers or surface modifying layers to enable high mobilities coupled with low voltage applications in ambient environments.

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<sup>1</sup>G. Horowitz, *J. Mater. Res.* **19**, 1946 (2004).

<sup>2</sup>C. D. Dimitrakopoulos and P. R. L. Malenfant, *Adv. Mater. (Weinheim, Ger.)* **14**, 99 (2002).

<sup>3</sup>S. F. Nelson, Y.-Y. Lin, D. J. Gundlach, and T. N. Jackson, *Appl. Phys. Lett.* **72**, 1854 (1998).

<sup>4</sup>Z. Bao, V. Kuck, J. A. Rogers, and M. A. Paczkowski, *Adv. Funct. Mater.* **12**, 526 (2002).

<sup>5</sup>J. Veres, S. Ogier, and G. Llyod, *Chem. Mater.* **16**, 4543 (2004).

<sup>6</sup>H. E. Katz, X. M. Hong, A. Dodabalapur, and R. Sarpeshkar, *J. Appl. Phys.* **91**, 1572 (2002).

<sup>7</sup>J. Takeya, T. Nishikawa, T. Takenobu, S. Kobayashi, Y. Iwasa, T. Mitani, C. Goldmann, C. Krellner, and B. Batlogg, *Appl. Phys. Lett.* **85**, 5078 (2004).

<sup>8</sup>Y. H. Noh, S. Y. Park, S.-M. Seo, and H. H. Lee, *Org. Electron.* **7**, 271 (2006).

<sup>9</sup>S. C. Lim, S. H. Kim, J. B. Koo, J. H. Lee, C. H. Ku, S. Y. Yang, and T. Zyung, *Appl. Phys. Lett.* **90**, 173512 (2007).

<sup>10</sup>T. Jung, A. Dodabalapur, R. Wenz, and S. Mohapatra, *Appl. Phys. Lett.* **87**, 182109 (2005).

<sup>11</sup>J. B. Koo, C. H. Ku, S. C. Lim, S. H. Kim, and J. H. Lee, *Appl. Phys. Lett.* **90**, 133503 (2007).

<sup>12</sup>T. Cahyadi, J. N. Tey, S. G. Mhaisalkar, F. Boey, V. R. Rao, R. Lal, Z. H. Huang, G. J. Qi, Z. -K. Chen, and C. M. Ng, *Appl. Phys. Lett.* **90**, 122112 (2007).

<sup>13</sup>D.-W. Park, C. A. Lee, K.-D. Jung, B.-G. Park, H. Shin, and J. D. Lee, *Appl. Phys. Lett.* **89**, 263507 (2006).

<sup>14</sup>C. A. Lee, D. W. Park, S. H. Jin, I. H. Park, J. D. Lee, and B.-G. Park, *Appl. Phys. Lett.* **88**, 252102 (2006).

<sup>15</sup>C. Huang, J. E. West, and H. E. Katz, *Adv. Funct. Mater.* **17**, 142 (2007).

<sup>16</sup>A. Salleo, M. L. Chabinyc, M. S. Yang, and R. A. Street, *Appl. Phys. Lett.* **81**, 4383 (2002).

<sup>17</sup>M.-H. Yoon, C. Kim, A. Facchetti, and T. J. Marks, *J. Am. Chem. Soc.* **128**, 12851 (2006).

<sup>18</sup>L. L. Hench and J. K. West, *Chem. Rev. (Washington, D.C.)* **90**, 33 (1990).

<sup>19</sup>D. M. Fleetwood, P. S. Winokur, R. A. Reber, T. L. Meisenheimer, J. R. Schwank, M. R. Shaneyfelt, and L. C. Riewe, *J. Appl. Phys.* **73**, 5058 (1993).

<sup>20</sup>J. F. Shackelford and J. S. Masaryk, *J. Non-Cryst. Solids* **21**, 55 (1976).

<sup>21</sup>M. J. Panzer and C. D. Frisbie, *J. Am. Chem. Soc.* **129**, 6599 (2007).