J|A|C|S COMMUNICATIONS

Published on Web 06/27/2006

Electrical Characteristics and Chemical Stability of Non-Oxidized, Methyl-Terminated Silicon Nanowires

Hossam Haick,[†] Patrick T. Hurley,[†] Allon I. Hochbaum,[‡] Peidong Yang,*[,‡,§] and Nathan S. Lewis*[,†]

Division of Chemistry and Chemical Engineering, California Institute of Technology, MC 127-72, 1200 East California Boulevard, Pasadena, California 91125, Department of Chemistry, University of California, Berkeley, California 94720, and Materials Science Division, Lawrence Berkeley National Laboratory, Berkeley, California 94720

Received October 4, 2005; E-mail: nslewis@its.caltech.edu

The ability to manipulate the conductivity of nanowires (NWs) through chemical surface modification is important for the realization of NW-based electronic devices and chemical senors.[1−4] Oxide-coated Si NWs have been functionalized with amino siloxanes to impart pH sensitivity to the NW conductance.[3] Exposure of oxidized Si NW to 4-nitrophenyloctadecanoate or to tetraethylammonium bromide has also been shown to improve the NW conductance and to improve on−off ratios in Si NW-based field-effect transistors (FETs),[2] although the mechanism by which these treatments modify the interface state density at oxide-coated Si NWs is not clear. Oxide coating of a Si NW is thought to induce trap states at the SiO_2/Si interface.[5] In addition, oxide coating of a Si NW is thought to act as a dielectric that lowers, and ultimately can limit, the effect of gate voltage on manipulating the conductance between the source and drain of Si NW-based FETs.[2] Macroscopic, planar Si(111) devices that are not oxidized but H-terminated exhibit low interface state density, yet are relatively unstable to oxidation and defect formation in the presence of air.[6] We report herein that Si NWs modified by covalent Si−CH_3 functionality, with no intervening oxide, show atmospheric stability, high conductance values, low surface defect levels, and allow for the formation of air-stable Si NW FETs having on−off ratios in excess of 10^5 over a relatively small gate voltage swing (±2 V).[7]

The Si NWs investigated were prepared by vapor−liquid−solid growth techniques,[8] yielding p-type Si NWs doped with B to free-carrier densities of $(1-4) \times 10^{17}$ cm^{-3}. The NWs grew along the (111) direction. Transmission electron microscopy (TEM) data indicated that these NWs consisted almost entirely of smooth 62 ± 5 nm diameter Si cores coated with SiO_2. The SiO_2 sheath was relatively uniform on an individual wire, but the coating thickness varied in the range of 6−12 nm between different wires (cf. Figure 1S(a) and (b)). Some of these NWs were then terminated with H, by etching in buffered HF followed by exposure to NH_4F(aq).[6,9] TEM images for freshly prepared H-terminated Si NW samples showed a similar core diameter to the SiO_2-coated Si NWs but no detectable SiO_2 by energy dispersive spectroscopy (EDS) (cf. Figure 1S(c)). The outer surface of these H−Si NWs was nearly uniform and exhibited a low concentration of TEM-detectable defects. Some of these NWs were then methyl-terminated using a two-step chlorination/alkylation route.[10] TEM images of freshly prepared CH_3−Si NW samples showed features similar to those of H−Si NWs, except that the outer surface of the CH_3−Si NWs was less smooth (cf. Figure 1Sd) than that of the H−Si NWs.

Devices were fabricated by integrating an individual Si NW with four Al electrodes (each 5.0 ± 0.1 μm in length and 400 ± 20 nm in width) that were mutually separated by 800 ± 50 nm, on top of a 300 nm thermally oxidized degenerately doped p-Si (0.001 $\Omega \cdot cm^{-1}$ resistivity) substrate. For each device, the extrinsic conductivity (g_{ex}) was determined using two-point probe methods, and the intrinsic conductivity (g_{in}) was determined by four-point probe methods. Voltage-dependent back-gate measurements, to determine the performance of Si NWs as FETs, were also performed. Measurements were performed on 5−10 devices from each type and from different batches of Si NWs.

For all samples, the four-point $I-V$ data were linear and symmetric about zero bias and showed higher conductivities than those obtained using two-point methods (cf. Figure 2S). Comparison between $I-V$ curves of the different samples, taken at zero back-gate voltage (V_g), indicated that the average conductance of SiO_2−Si NWs ($g_{ex} = 20 \pm 9$ nS; $g_{in} = 41 \pm 15$ nS) was much less than that of H−Si NWs ($g_{ex} = 96 \pm 20$ nS; $g_{in} = 186 \pm 43$ nS), which, in turn, was less than that of CH_3−Si NWs ($g_{ex} = 120 \pm 21$ nS; $g_{in} = 279 \pm 38$ nS).

Figure 1 depicts the normalized average conductance at $V_g = 0$ V of the various Si NWs versus time in air, as determined by two-point ($\gamma_{ex} = g_{ex}/(g_{ex})_{t=0}$; Figure 1a) and four-point ($\gamma_{in} = g_{in}/(g_{in})_{t=0}$; Figure 1b) measurements. For SiO_2−Si NWs, γ_{ex} and γ_{in} remained constant, within experimental error, as a function of time. For both H−Si NWs and CH_3−Si NWs, the rate of decrease of γ_{ex} (i.e., $\Delta\gamma_{ex}/\Delta t$) and γ_{in} (i.e., $\Delta\gamma_{in}/\Delta t$) showed three main "time" regions, 0−3, 3−168, and 168−672 h: $[\Delta\gamma_{ex}/\Delta t]_{0-3\ h} \gg [\Delta\gamma_{ex}/\Delta t]_{3-168\ h} > [\Delta\gamma_{ex}/\Delta t]_{168-672\ h}$, $[\Delta\gamma_{in}/\Delta t]_{0-3\ h} \gg [\Delta\gamma_{in}/\Delta t]_{3-168\ h} > [\Delta\gamma_{in}/\Delta t]_{168-672\ h}$, and, mostly, at each time region, $\Delta\gamma_{ex}/\Delta t > \Delta\gamma_{in}/\Delta t$. γ_{ex} and γ_{in} of the H−Si NWs continued to decrease even after 672 h (4 weeks) of exposure to air, whereas after 168 h in air, γ_{ex} and γ_{in} of CH_3−Si NWs stabilized to within 80% and 85% of their initial values, respectively. The electrical and chemical passivation of Si NWs by alkyl termination is in accord with the behavior of alkylated (111)- and (100)-oriented crystalline Si surfaces, which show surface recombination velocities of <100 cm s^{-1} for over 1 month in air and substantial resistance to air oxidation for a period of months.[6]

As shown in Figure 2, in a typical SiO_2−Si NW device, g_{in} responded weakly to the applied gate voltage, V_g, with g_{in} decreasing from 255 nS at $V_g = -5$ V to 4 nS at $V_g = +5$ V, and showing no significant on−off state transition within this gate-bias region. This behavior is in accord with prior work showing that SiO_2/Si interface and SiO_2 surface defects on oxidized Si NW compensate V_g and also trap and scatter carriers.[11] In contrast, the average conductance of freshly prepared H−Si NWs and of CH_3−Si NWs was extremely sensitive to V_g and could be shut off at $V_g \sim 2.6$ and 2.4 V, respectively, with an on/off ratio of 3.9×10^4 and 1.3×10^5. The average conductance of H−Si NWs and CH_3−Si NWs at $V_g = 0$ V was ca. 4- and 7-fold higher, respectively, than that of the SiO_2−Si NWs. Using a cylinder on an infinite plate model[12] yielded

[†] California Institute of Technology.
[‡] University of California, Berkeley.
[§] Lawrence Berkeley National Laboratory.

10.1021/ja056785w CCC: $33.50

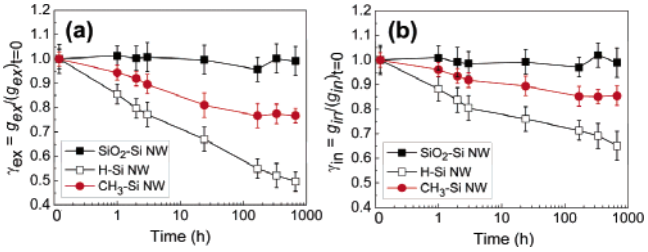

Figure 1. Normalized average conductance at $V_g = 0$ V of SiO_2-Si NW, H−Si NW, and CH_3-Si NW samples versus exposure time to air, as determined by (a) two-probe ($\gamma_{ex} = g_{ex}/(g_{ex})_{t=0}$) and (b) four-probe ($\gamma_{in} = g_{in}/(g_{in})_{t=0}$) measurements. Here, g_{ex} and g_{in} are the average extrinsic and intrinsic conductances of the Si NW at a given exposure time to air, and $(g_{ex})_{t=0}$ and $(g_{in})_{t=0}$ are the average extrinsic and intrinsic conductance, respectively, of freshly prepared samples (i.e., at $t = 0$ h). For SiO_2-Si NWs, H−Si NWs, and CH_3-Si NWs, $(g_{ex})_{t=0} = 20$, 96, and 120 nS, respectively, and $(g_{in})_{t=0} = 41$, 186, and 279 nS.

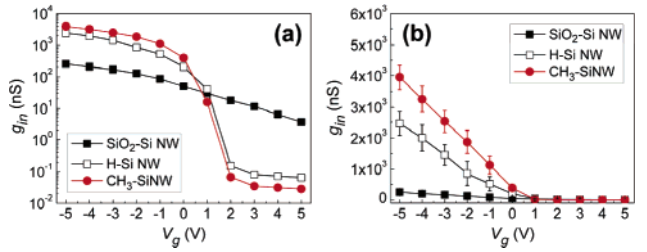

Figure 2. Average intrinsic conductance (g_{in}) versus back-gate voltage for SiO_2-Si NW, H−Si NW, and CH_3-Si NW samples in (a) semilogarithmic and (b) linear scales.

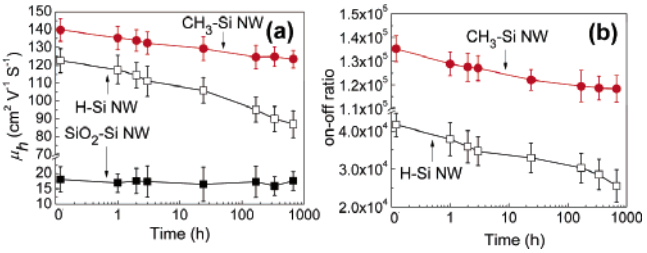

Figure 3. (a) Average hole mobility (μ_h) of SiO_2-Si NW, H−Si NW, and CH_3-Si NW samples versus exposure time to air. For clarity, a break in the *y*-scale, at $\mu_h = 25-70$ cm^2 V^{-1} s^{-1}, was introduced. (b) On−off ratio of H−Si NW and CH_3-Si NW field-effect transistors (FETs) versus exposure time to air. For clarity, a break in the *y*-scale, at an on−off ratio between 4500 and 11000, was introduced. For SiO_2-Si NW, on−off ratios were undetectable for -5 V $< V_g <$ +5 V.

estimates for the hole mobility, μ_h, of 18 ± 4 cm^2 V^{-1} s^{-1} for SiO_2-Si NW, 123 ± 3 cm^2 V^{-1} s^{-1} for H−Si NWs, and 140 ± 2 cm^2 V^{-1} s^{-1} for CH_3-Si NWs.

Voltage-dependent back-gate voltage measurements as a function of time in air revealed substantial differences between SiO_2-Si NWs, H−Si NWs, and CH_3-Si NWs (Figure 3). The mobility of SiO_2-Si NWs did not change, within experimental error, as a function of time in air. In contrast, the mobility of H−Si NWs decreased continuously, dropping from 123 to 87 cm^2 V^{-1} s^{-1} after 4 weeks (672 h) exposure to air, with the highest rate of degradation during the first 3 h of exposure to air. For CH_3-Si NWs, the mobility decreased upon exposure during the first week (=164 h) by ca. 11%, from 140 to 124 cm^2 V^{-1} s^{-1}, after which time it stabilized at a level that was comparable to the initial value of the H−Si NW hole mobility (i.e., at $t = 0$).

The trend in mobilities and on−off ratios, with CH_3-Si NWs > H−Si NWs ≫ SiO_2-Si NWs, can be attributed different densities of surface states. Passivation of surface states via H-termination or Si−C bonds on the Si NW surfaces decreases the probability of electron−hole recombination[13] and, thus, increases the carrier mobilities. In response to changes in gate voltage, the same passivation of surface states allows for more effective movement of band edges in the channel, compared to channels with SiO_2/Si interface or SiO_2 surface states and, thus, increases the on−off ratio of FETs (cf. ref 13). The presence of hysteresis, that is, "memory" effects,[1] in fresh samples of SiO_2-Si NWs, but not in fresh samples of H−Si NWs or CH_3-Si NWs, and the observation of the gradual development of hysteresis in H−Si NWs upon increasing exposure time to air support the effects of surface states on the electrical properties of Si NW FETs.

The stable CH_3-Si NW mobility and high on−off ratio of CH_3-Si NW FETs may make this approach of significant technological interest. The carrier mobility could likely be further improved by, for example, decreasing the doping level, decreasing the nanowire diameter,[14] and/or minimizing the "bending" sites and surface roughness along the Si NW.[14] Alkylation of crystalline Si using the two-step chlorination/alkylation method has been shown to proceed with minimal surface recombination using a variety of alkyl groups that allow molecular level control and positioning of the functionality and insulating dielectric properties,[6] to allow for the introduction of double bonds that facilitate elaboration of the surface by further chemical functionalization, such as polymerization and other organic reactions,[15] and to introduce or eliminate the pH dependence of the flat-band potential of Si surfaces in aqueous solutions,[16] suggesting that surface alkylation can be of utility in forming Si NW electrical devices and Si NW chemical and biological sensors with highly desirable properties under molecular level control.

Acknowledgment. We acknowledge the NSF, Grant CHE-0213589, for support of this work (N.S.L.), and DARPA-MARCO (P.Y.). H.H. thanks the Fulbright foundation for his postdoctoral fellowship, and A.H. thanks NSF for an IGERT fellowship.

Supporting Information Available: Procedure for producing H−Si and CH_3-Si NWs, TEM images of the various Si NWs, and electrical measurements. This material is available free of charge via the Internet at http://pubs.acs.org.

References

(1) Duan, X.; Huang, Y.; Lieber, C. M. *Nano. Lett.* **2002**, *2*, 487−490.
(2) Cui, Y.; Zhong, Z.; Wang, D.; Wang, W. U.; Lieber, C. M. *Nano. Lett.* **2003**, *3*, 149−152.
(3) Patolsky, F.; Lieber, C. M. *Mater. Today* **2005**, *8*, 20−28.
(4) Goldberger, J.; Sirbuly, D. J.; Law, M.; Yang, P. *J. Phys. Chem. B* **2005**, *109*, 9−14.
(5) Sham, T. K.; Naftel, S. J.; Kim, P.-S. G.; Sammynaiken, R.; Tang, Y. H.; Coulthard, I.; Moewes, A.; Freeland, J. W.; Hu, Y.-F.; Lee, S. T. *Phys. Rev. B* **2004**, *70*, 045313/1−045313/8.
(6) Webb, L. J.; Lewis, N. S. *J. Phys. Chem. B* **2003**, *107*, 5404−5412.
(7) For our devices, a gate voltage swing between −2 and +2 V is equivalent to a swing in the applied electric field of between 4 and 8 V/μm (at a source-drain bias of 0.1 V).
(8) Hochbaum, A. I.; Fan, R.; He, R.; Yang, P. *Nano. Lett.* **2005**, *5*, 457−460.
(9) Ma, D. D. D.; Lee, C. S.; Au, F. C. K.; Tong, S. Y.; Lee, S. T. *Science* **2003**, *299*, 1874−1877.
(10) Bansal, A.; Li, X.; Lauermann, I.; Yi, S.; Weinberg, W. H.; Lewis, N. S. *J. Am. Chem. Soc.* **1996**, *118*, 7225−7226.
(11) Lupke, G. *Surf. Sci. Rep.* **1999**, *35*, 75−161.
(12) Martel, R.; Schmidt, T.; Shea, H. R.; Hertel, T.; Avouris, P. *Appl. Phys. Lett.* **1998**, *73*, 2447−2449.
(13) Wolf, S.; Tauber, R. N. *Silicon Processing for the VLSI Era*; Lattice Press: Sunset Beach, CA, 1986.
(14) Wang, J.; Polizzi, E.; Ghosh, A.; Datta, S.; Lundstrom, M. *Appl. Phys. Lett.* **2005**, *87*, 043101-1−043101-3.
(15) Juang, A.; Scherman, O. A.; Grubbs, R. H.; Lewis, N. S. *Langmuir* **2001**, *17*, 1321−1323.
(16) Hamann, T. W.; Lewis, N. S. To be submitted.

JA056785W