Electrical Characterization of a Pressed Contact Between a Power Chip and a Metal Electrode

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***Abstract*—This study deals with the power electronics packaging and the needs for additional knowledge about electrical pressed contact behavior. For this, a measure bench has been realized. It is able to characterize the pressed interface between a metal electrode and a power chip as a function of the clamping force (0-8000N) and the temperature (up to 100°C). First measurement results show that the electrical contact resistance is negligible compared to the chip on-state voltage. Second measurement results show that the high value of the chip metallization resistance masks also the contact resistance. Finally, it appears that it is necessary to estimate the chip contact zone influences on the current repartition. Then a method based on both, the use of a chip model and the measurements directly on the chip, has been developed. It is able to look for the steady state current repartition in the chip as a function of the contact zone and the chip metallization physical parameters.**

Keywords-component; Pressed contact, Electrical contact resistance measurement, power chip.

I. INTRODUCTION

This study is a part of a research work looking for new power electronics packaging [1][2]. It concerns the electro-thermo-mechanical contacts of the vertical power chips.

The packaging of power electronics chips must fulfill some tasks and requirements [3]: the electrical interconnections of power and control between the components, the external electrical circuits and the environment; the thermal and mechanical interconnections; the chemical and radiation protections; the correct matching between the cost of production and supply business; and finally the global reliability of the module.

The electro-thermo-mechanical contacts are usually based on backside soldering and front side wire bonding. Widely used for small and medium power levels, back side soldering technique is well known and established. It presents very low thermal and electrical resistances. However the thermo-mechanical aging of solders causes reliability problems [3]. The electrical interconnections on the front side of the chip are usually realized thanks to wire bond technology [4]. This technique relaxes the thermo-electrical stresses but the reliability is still a question [5]. Besides, the wires introduce some undesired parasitic inductances [6] and they can not be considered for heat exchange or removal.

Double sided solder packages with bumps [7][8] improve the heat transfers but amplify the thermo-mechanical stress leading to reduced reliability and robustness. Moreover, the temperature limitations of regular soldering techniques and materials prohibit their use for high temperature applications like SiC applications.

From medium up to high and very high power levels, pressed contacts are often considered. Mainly used in the past for chips with large surfaces, products are now available with IGBT in the range of 1cm² and contacted by pressure. The reasons for this technique to remain limited are related to its implementation cost. It presents a good reliability over the time but its implementation is quite difficult: the pressure on the components must be set between 3.10^6 Pa and 10^7 Pa [9], which corresponds to a clamping force up to 135 kN (for 12cm²) and more as the contact surfaces increase.

In a previous paper [1] we have evaluated the feasibility of a low force press-pack module for the medium power applications (from hundreds of W to several kW). Now, we need to make the electrical and thermal characterizations of the pressed contact between the chip metallization and the metal electrodes (Fig.1). In this paper, we show the experimental setup for the electrical contact resistance and direct voltage drop measurements in a chip as a function of pressure and temperature. This work is notably important to find the best metal interface to improve the contact behavior.

Moreover, an experimental method coupled with simulations is developed to anticipate the current repartition in a chip as a function of the contact zones between the electrode and the chip metallization. This method is based on a both use of a chip model and measurements.

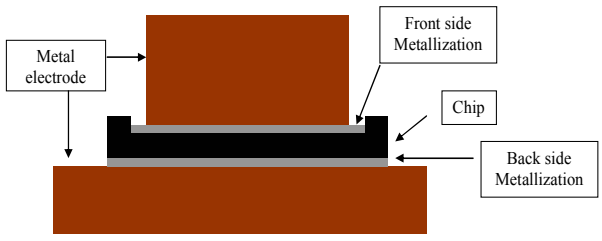

Figure 1. The chip and the pressed contact zone

II. DESCRIPTION OF THE MEASURE BENCH.

A measurement bench has been realized (Fig.2). A chip, diode or IGBT is griped between two copper jaws up to 8000N. The chip surface is around 1cm². A special care has been paid on the mechanical structure design to achieve high clamping forces without chip destruction. A force sensor indicates continuously the clamping force value. Below the inferior copper jaw, there is a heat exchanger to regulate the chip temperature. It is based on heat carrier oil that circulates and regulates the temperature of the device under test. The maximum oil temperature is 150°C. The temperature is measured with a thermocouple close to the chip.

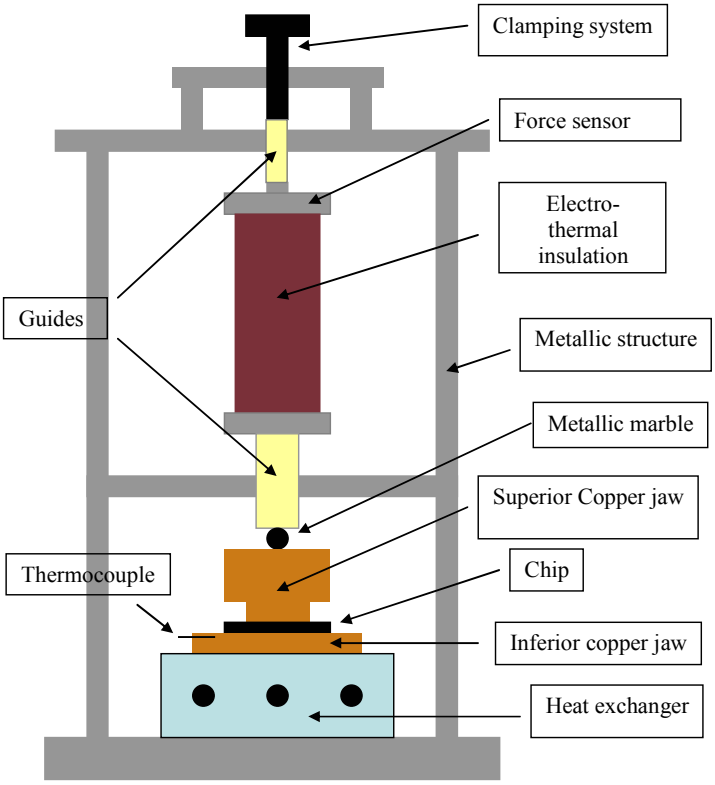

Figure 2. Electrical contact resistance measurement device

The experimental device allows the characterization of two different chip types: diodes and IGBT. For this, two kinds of superior jaws have been designed to be adapted to the chip front side layout (Fig.3). Moreover, for the IGBT case, the command signal (gate contact) is integrated in the jaw to allow its conduction mode and the current circulation in the device.

The electrical contact resistance measurement is based on the four points method. A current is injected in the device and the voltage drop is measured closest to the contact region. As the expected electrical contact resistance value is small, the current must be large enough to guarantee the quality of the measurements. In our case, about 100A/cm² current density was injected. To avoid the temperature rise during the measurements, the current injection is made only for a small time: the pulse duration is 300µs and the period 80ms. Moreover, the experiments have been designed to allow two different types of measurements. The first available measure is the electrical contact resistance between the chip and an electrode made by a solid copper jaw (Fig.4):

$$\Delta V_c = \Delta V_{R\ contact} + \Delta V_{solid\ copper} \quad (1)$$

Knowing the injected current value, we can deduce the electrical resistance with a voltage measure. This measure is possible on both sides of the chip (Fig.3 and 4).

The second one is the global voltage drop when the chip is in conduction:

$$\Delta V_{global} = \Delta V_{R\ contact\ front\ side} + \Delta V_{R\ contact\ back\ side} + \Delta V_{chip} + \Delta V_{upper\ solid\ copper} + \Delta V_{lower\ solid\ copper} \quad (2)$$

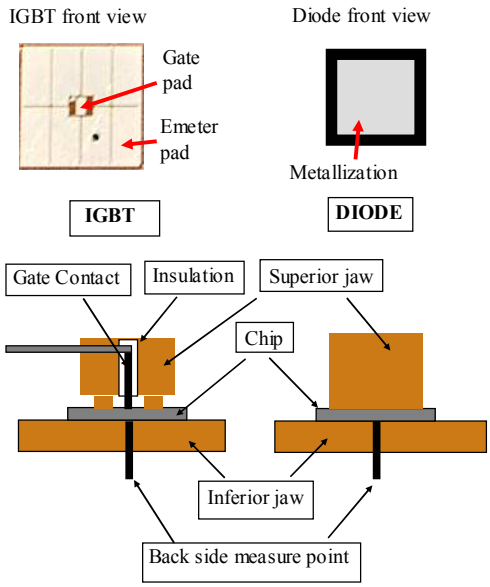

Figure 3. Integration of the command signal in the device for the IGBT characterization

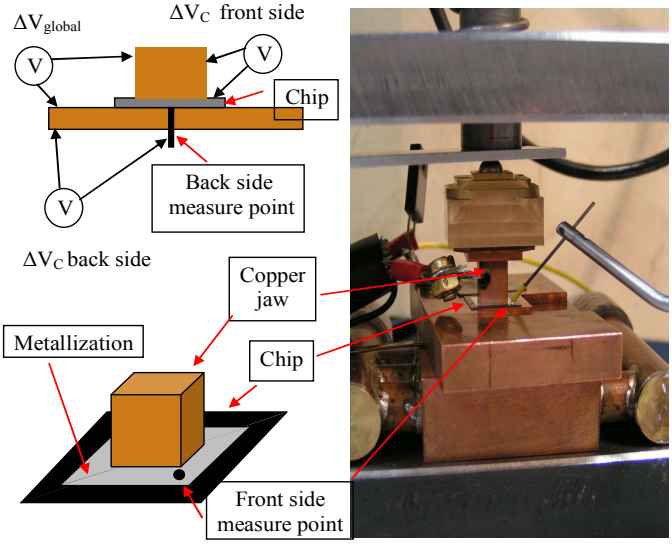

Figure 4. Measurement possibilities

About the current pulses generation and the measuring chain.

The current pulses are created by a Tektronix Sony High Power Curve Tracer (371A). It has been necessary to shield the wires to avoid electromagnetic disturbances on the measuring chain (Fig.5).

For the voltage measurements, the input signal is amplified by a differential amplifier (AD 622AN) and displayed on the oscilloscope. A 0.05Ohm shunt is used to visualize the current.

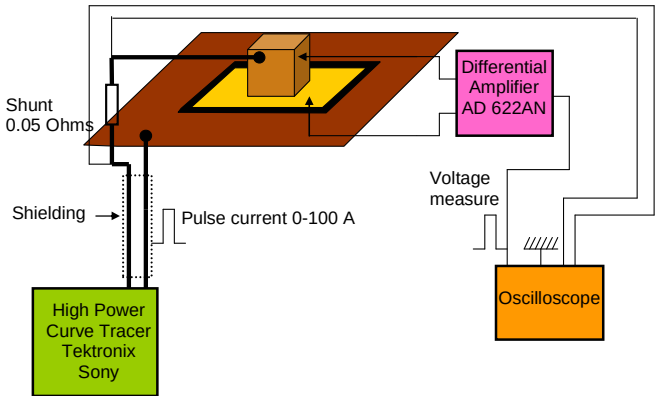

Figure 5. Current pulse generation and mesuring chain

III. RESULTS.

A. Global voltage drop

In Fig.6 we can see the global voltage drop ΔV_{global} of a diode Eupec 3.3kV – 50A for a 70A current injection during 300µs and for two different clamping forces: 250N and 5000N at the ambient temperature.

We can observe the same global voltage drop for both clamping forces, so it shows that the electrical contact resistance is negligible compared with the on-state voltage drop of the chip.

Moreover, to evaluate the solid copper contribution $\Delta V_{solid\ copper}$ on the global voltage drop ΔV_{global} we have moved the measure point positions on the copper jaws. We noticed that these displacements have no consequences on the results. As a result, it could be stated that the resistance voltage drop of the solid copper is negligible with regards to the voltage drop across the device while it is in the on-state carrying large current levels.

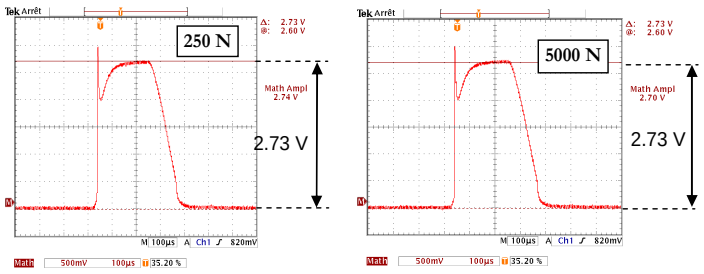

Figure 6. Global voltage drop for 250N and 5000N clamped force at ambiant temperature

Finally we can say that $\Delta V_{global} = \Delta V_{chip}$.

That is a very interesting and important conclusion for the packaging manufacturers: **the value of the electrical contact resistance between the chip and the metal electrode is negligible in a pressed contact implementation.** On the other hand, it is necessary to improve our knowledge of the interface contribution to the chip on-state behavior. That's why we tried to measure the contact resistance of the interface $\Delta V_{R\ contact}$.

B. Contact resistance measurement

To allow the measurement of the contact resistance we have separated the measures carried out on each face of the chip (Fig.4). Moreover, on the front side of the chip we have localized four measure points on different places of the chip metallization. That was possible for both IGBT and diode (Fig.7). Like in III.A we make the verification that $\Delta V_{solid\ copper}$ was negligible. Then (1) can be write $\Delta V_c = \Delta V_{R\ contact}$.

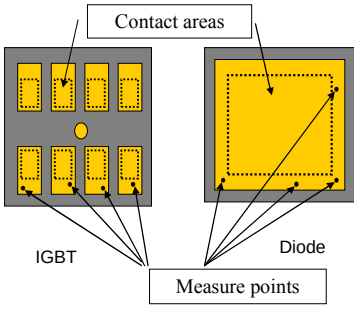

Figure 7. Different places for the electrical contact resistance measurements

In Fig 8, we can see the evolution of the electrical contact resistance between the copper jaw and a Diode metallization as a function of the clamping force for four measure points (diode Eupec 3.3kV – 50A). Even if the global evolution is a decrease of the resistance value for clamping force increase, it is very surprising that the results depend on the measure point position. **It means that the chip metallization can not be considered as an equipotential.**

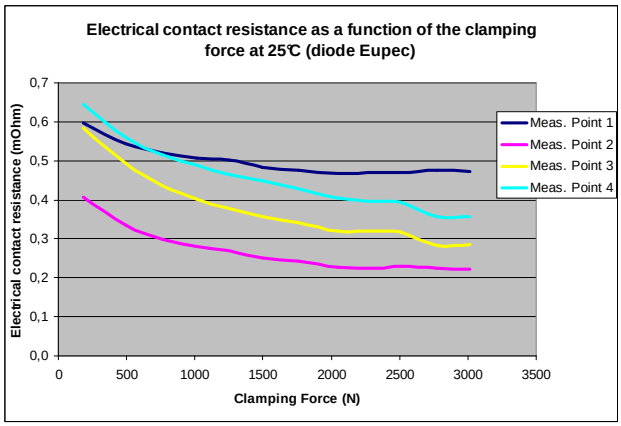

Figure 8. Electrical contact resistance as a function of the clamping force at 25°C (diode Eupec 3.3kV – 50A)

The non equipotentiality of the metallization leads us to measure the surface resistance of a chip metallization (Fig.9).

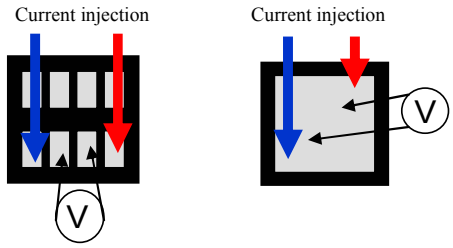

Figure 9. Measure of the surface resistance of the chip metallization

The results are about 3mΩ for the diode and 20mΩ for the IGBT.

That shows that the electrical contact resistance between a metal electrode and a chip metallization is hidden by the characteristics of the metal layer deposited at the surface of the power chip. In fact, the metallization resistance masks the contact resistance.

Finally the value of the contact resistance is not the key point; and it becomes necessary to evaluate the interactions between the contact zones location and the metallization physical parameters on the chip current repartition.

IV. THE CURRENT REPARTITION IN A CHIP AS A FUNCTION OF THE CONTACT ZONES.

A non homogeneous current repartition in the chip could create some hot points in the chip [10][11]. An extreme consequence could be the destruction of the chip. Then it is very important to study the influence of the contact zone on the current repartition.

The resistivity and the thickness of the metallization are not given by the chip manufacturers. Then we developed a measure method for the physical characterization of the chip metallization. After that, using a semiconductor chip model, it was possible to predict the current repartition as a function of the contact zones surface and locations and the physical characteristics of the metallization.

A. Realization of a numerical model of the chip metallization.

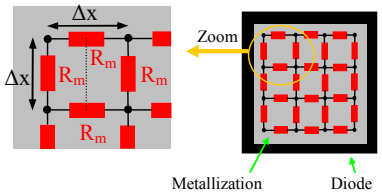

Figure 10. Numerical model of the metallization

Diode metallization is modeled by a resistance network in accordance to Fig.10. R_m is the elementary metal resistance:

$$R_m = \frac{\rho.L}{S} = \rho\frac{\Delta x}{\Delta x \cdot e} = \frac{\rho}{e} \qquad (3)$$

With e the metallization thickness and ρ the resistivity.

Finally the Ohm's law applied to the metallization can be written [12]:

$$I = \frac{e}{\rho}.G.V \qquad (4)$$

with I the nodes current matrix, V the nodes voltage matrix and G the conductance matrix. It is interesting to notice that G is a coefficient matrix depending only on the nodes positions and not on the physical parameters of the metallization (e and ρ).

B. Identification between the model results and the measures to find the physical characteristics of the metallization (electrical resistivity and thickness).

Based on the same measurement principle as depicted Fig.9, a current is injected in the corner of the metallization. From the surface voltage measures and a comparison with a normalized model it is possible to calculate the ratio ρ/e of the metallization:

$$\frac{V_{Measure}}{V_{Model}} = \frac{\frac{\rho}{e}\cdot G^{-1}\cdot I}{G^{-1}\cdot I} = \frac{\rho}{e} \qquad (5)$$

To guarantee the X,Y locations of the measure points and the injection current points, we have developed a Plexiglas footprint situated on the top of the chip (Fig.11). The surface metallization is 9*9mm². Then we placed on the footprint a 0.3mm diameter hole each millimeter. These holes create a 64 holes network making possible the current injection or the voltage measure in many different conditions. The current injection and tools used for the measurements are the same as those depicted Fig.5. The measurement device allows two kinds of measures. The two current electrodes can be first contacted on the front side of the chip; method used to find the physical parameters of the metallization (Fig11). Or one electrode current in the chip front side, and the second one contacted on the back side of the chip by a connection to the Cu plate: method used for the surface voltage observation.

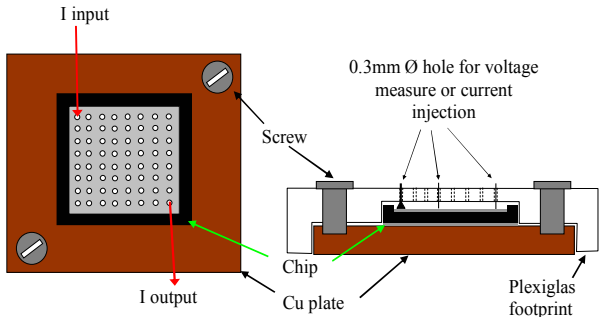

Figure 11. Top view and side view of the measurement bench

This step has been validated by an experimental test with a well known and simple to characterize metal layer, a patterned copper layer on a PCB.

For the diode metallization characterization we obtained a value **ρ/e = 3mΩ** with measures realized on a Dynex diode 1.7kV–50A Ti/Ni/Ag.

In Fig12 we can see the surface voltage distribution measured with the second method for an injected current

I=43A in a corner and exit by the chip back side. For the voltage measure, the opposite corner of the current injection is considered as for the voltage reference. The voltage values observed are the difference between this point and all the other meshed points (nodes) of the network. We can see that ΔVmax is close to 1.5V. It clearly demonstrates that when the power diode is forward biased, its metallization is not an equipotential.

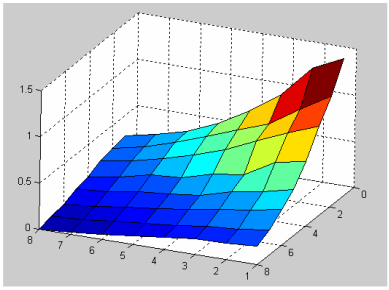

Figure 12. Surface voltage repartition with I=43A injected in a corner

Although this experiment is carried out in extreme testing conditions, it seems now interesting to analyze the consequences of this non homogeneous voltage distribution on the chip current repartition inside the power device. As the current measures in different regions of the chip are impossible, it was necessary to fall back to simulation in order to estimate the impact of the metallization and the electrical contact regions on the current distribution inside the power device. Of course, this is an important issue since a non homogeneous current repartition would lead to poor performances but it would also lead to inhomogeneous temperatures and greater current concentrations. Soon, the device may fail due to this phenomenon.

The goal of the simulation is to create a model representing the metallization and the behavior of the power diode by a full descretization of the metal layer but also the vertical device. Reproducing a comparable surface voltage profile could help us understanding and estimating the current distribution inside the power device. The exact comparison between measure and simulation is not possible at the time of this paper due to the differences observed between the semiconductor model and the real chip. However, it can be used to analyze the tendencies of the electrical magnitudes.

C. *Current repartition simulations*

In Fig.13 we can see the geometrical structure simulated with R_m the metal resistance (defined in IV.1), R_{ci} contact resistance between metal and silicon ($10^{-4}>R_c>10^{-6}$ Ω.cm² [3]).

Diode model

The diode model is a VHDL-AMS model taking into account the semi-conductor behavior. Physical parameters and concentrations are those of a classical power diode 600V-100A. The electrical equation of the diode is $V_d=Vj + R_{on}.I_d$ in which all the parameters depends on the carrier concentration, also dependent on the current density. Vj represents the forward bias of the PN junction and Ron represents the conduction voltage drop as a function of the injected carrier "n" and "p" concentration injected in the drift region of the power diode. This simple model has been derived based on [13] For example for I_d = 100A, R_{on}=0.23mΩ, V_j=0.653V and V_d=0.677V. The surface of each elementary diode depends on the number of nodes chosen for the simulation. In the model, the lateral conduction and diffusion currents due to the carriers concentrations and voltage gradients are not considered. However, for each simulation, we have estimated the current value neglected by making this approximation.

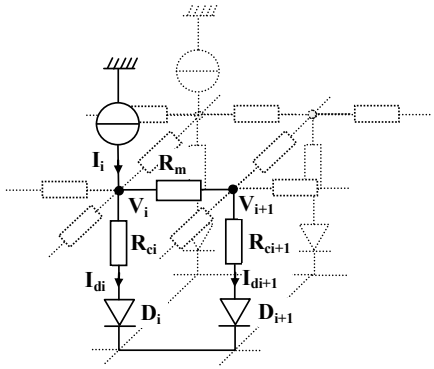

Figure 13. Geometry of the simulated structure

Current sources

An electrical contact between a copper electrode and the chip is represented by a limited number of current sources connected to a comparable number of nodes N_i. The number of nodes and their locations depend on the electrode geometry and the contact surface. The total current injected is always the same to simplify the simulation comparisons. Then $\sum I_i = 100\text{A}$.

Simulation conditions

We considered that the power chip simulated is a 1cm² power diode. The surface contact of the chip has been discretized in 20*20 = 400 elementary contacts represented by nodes. The number of nodes is lower than 400 in order to limit the computation time.

A program generates automatically the netlist used to describe the simulation schematic and parameters as a function of the nodes number, the current injection zones and the physical parameters (metallization resistivity, contact resistance between metal and silicon, drift and anode region characteristics, carrier lifetime, diffusion potential…).

Only the steady state forward bias conduction mode is simulated with Simplorer Software. As a result, the power diode model doesn't have to be implemented to represent dynamic behavior.

D. *Results and discussion*

In Fig.14 we can see the current repartition in the diode (I_{di}) and the chip surface voltage (V_i) for three different values of the metallization resistance: 30mΩ, 3mΩ and 0.3mΩ. The chip surface is 1cm² and the injection current zone is 4mm² located in a corner.

As it could be expected, in each case, the voltage gradients of the metallization can be observed and they impact on the current distribution in the power device. As expected, the current density is maximum below the contact zone. When the value of the resistance increases, the difference between the

highest and the lowest current increases (Fig.14): the metallization parasitic resistance impacts on the current repartition and focuses the current way below the contact zone.

About the diode lateral diffusion current

For each simulation we notice that lateral diffusion currents among elementary diodes were lower than 5% of the average current flowing through each of them. The maximum value is obtained for the highest metal resistance. If greater, the diffusion currents would equalize the current distribution among the elementary diodes but it seems that it is a second order phenomena that is not enough important to impact on the current repartition. Then the approximation of the current repartition is still correct.

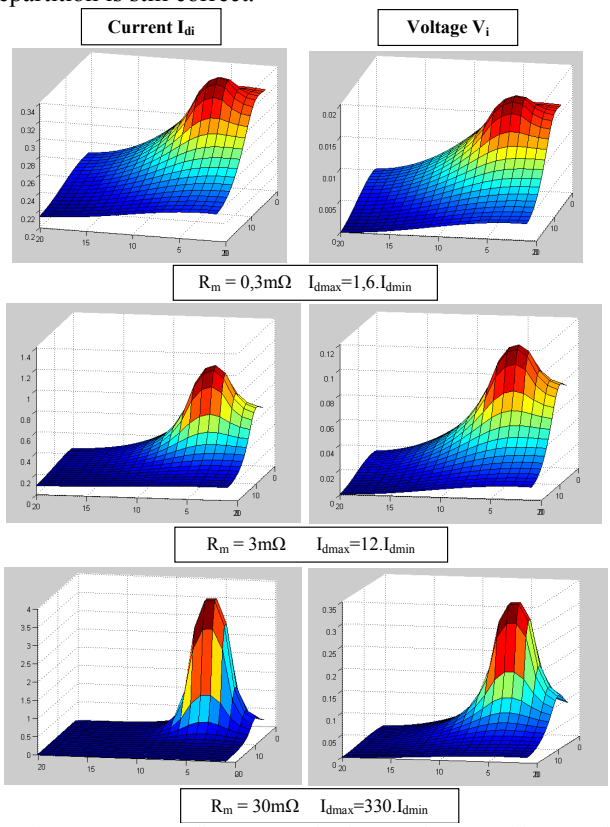

Figure 14. Current diodes (I_{di}) and voltage surface repartitions (V_i) for different values of the metallization resistance

Finally, the influence of the metallization in the chip current repartition is illustrated. A special care to a regular contact zone repartition on the chip surface is necessary to ensure an homogeneous current repartition in the chip. Fig.15 shows the current repartition with four contact zones correctly spreadon the surface of the chip metallization. We notice that I_{dmax}=1,77.I_{dmin}.

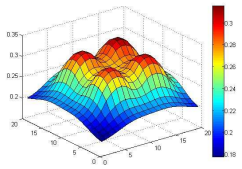

Figure 15. Current repartition with four contact zones. R_m = 3mΩ

V. CONCLUSION

The need to better know the electrical pressed contact behavior induced us to realize a measure bench able to characterize the pressed interface between a metal electrode and a power chip as a function of the clamping force (0-8000N) and the temperature (up to 100°C). The measures shown that the electrical contact resistance is negligible compared to the chip on-state voltage and that the important value of the chip metallization resistance masks the contact resistance. Finally, it appeared that it was necessary to estimate the chip contact zone influences on the current repartition. Then a method based on both use of a chip model and a specific measurement technique has been developed. It was able to estimate the current repartition in a diode as a function of the contact zone, the metallization physical properties and the semiconductor properties.

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