Electrical Modeling and Characterization of 3-D Vias

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Abstract— **Electrical characterization of the resistance, capacitance, and inductance of inter-plane 3-D vias is presented in this paper. Both capacitive and inductive coupling between multiple 3-D vias is described as a function of the separation distance and plane location. The effects of placing a third shield via between two signal vias is investigated as a means to limit the capacitive coupling. The location of the return path is examined to determine the best placement of a 3-D via to reduce the overall loop inductance. Based on the extracted resistance, capacitance, and inductance, the *L/R* time constant is shown to be much larger than the *RC* time constant, demonstrating that the 3-D via structure investigated in this paper is inductively limited rather than capacitively limited.**

I. INTRODUCTION

Three-dimensional integration is a novel technology of growing importance that has the potential to offer significant performance and functional benefits as compared to 2-D ICs. 3-D integration provides enhanced inter-connectivity, high device integration density, a reduction in the number and length of the long global wires, and the potential to combine disparate heterogenous technologies [1]. The primary technological innovation required to exploit the benefits of 3-D integration is the development of a through silicon 3-D via. Much work is needed to properly characterize and model these interplane through silicon vias.

Most previous work characterizing 3-D vias has focused on bulk silicon and emphasized the experimental extraction of the via resistance and capacitance. Due to the large variation in the 3-D via diameter, length, dielectric thickness, and fill material, a wide range of measured resistances, capacitances, and inductances have been reported in the literature. Single 3-D via resistance values vary from 20 mΩ to as high as 350 Ω [2]–[6], while reported capacitances vary from 40 fF to over 1 pF [7], [8]. A few researchers have reported measured via inductances that range from as low as 42 pH to as high as 255 pH [3], [9]. Alternatively, 3-D via modeling has primarily been applied to simple structures to verify the measured *RLC* values while providing some insight into 3-D via to 3-D via capacitive coupling [2], [7]. This paper expands on this early work, and adds new insight towards shielding both capacitive and inductive coupling. In addition, vias in 3-D SOI processes are shown to be inductively limited, similar to the much larger 3-D vias in bulk silicon processes.

The work reported in this paper examines the *RLC* impedances of a 3-D via based on the MIT Lincoln Lab 3-D integration process [10], [11]. Background information describing the MIT process and the Ansoft Quick 3-D toolset used in the via analysis is presented in Section II. The extracted resistance, capacitance, and inductance of a single via are presented in Section III. Capacitive and inductive coupling between two 3-D vias is examined in Section IV for different separation distances and structural topologies. Inter-plane coupling is also analyzed in Section IV. This analysis is followed in Section V by an examination of the effects of placing a 3-D shielding via between two signal vias. The effect on inductive coupling and the loop inductance as a result of the via placement is discussed in Section VI. A few concluding remarks are provided in the final section of the paper.

II. BACKGROUND INFORMATION

A basic understanding of the MIT Lincoln Lab 3-D integration process is provided as a means to understand the via topologies being evaluated. Lincoln Labs has established a 0.18 μm low power, fully depleted silicon on insulator (FDSOI) CMOS process where three independently patterned wafers are physically bonded together to form a 3-D integrated structure [10], [11]. Each wafer, described as either a plane or tier, has three metallization layers for routing. The top two planes have an additional backside metal used for both routing and to form the 3-D vias. The critical dimensions of a 3-D via are depicted in Fig. 1 [11]. Note that there are two inter-plane 3-D vias present in the figure, one that passes from Tier 1 (T1) to Tier 2 (T2) while the other passes from T2 to Tier 3 (T3). By overlaying the 3-D vias in this fashion, a signal may propagate from the bottom plane to the top plane. It is also acceptable for either the top via (T2 to T3) or bottom via (T1 to T2) to propagate a signal. Note also that the bottom plane (T1) includes a 675 $\pm$ 25 μm thick silicon substrate not shown in the figure which is used for wafer handling after the top two planes are bonded to T1. As a final note, the total length of a 3-D via starting from plane T1 and terminating on plane T3 is 17.94 μm, implying wafer thinning of planes T2 and T3 to approximately 10 μm [11]. Each 3-D via is surrounded by a combination of two dielectric layers, SiO_2 and tetraethylorthosilicate (TEOS). Both of these dielectric layers have similar relative permittivities, 3.9 and 4.0, respectively.

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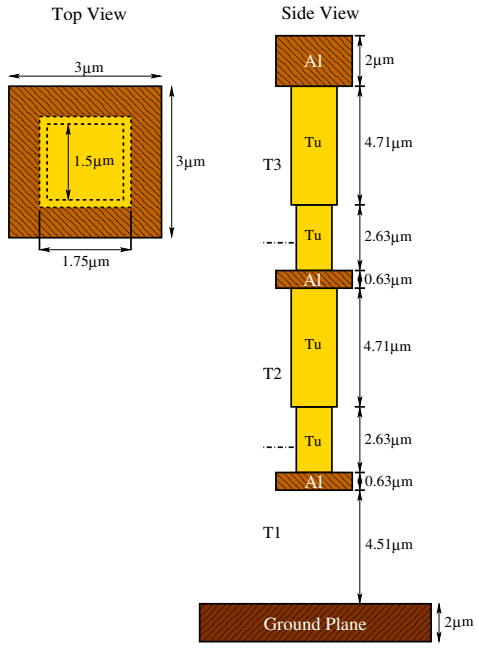

Fig. 1. Top and side view of a 3-D inter-plane via.

For simulation purposes, the average of the two permittivities is used in the Ansoft Quick 3-D toolset.

Ansoft Quick 3-D software is used to examine the *RLC* impedances, coupling, and shielding [12]. Quick 3-D is a 3-D/2-D quasi-static electromagnetic-field simulator used to extract the parasitic impedances and electrical parameters. The tool solves Maxwell's equations by utilizing the Finite Element Method (FEM) and the Method of Moments (MOM) to compute the 3-D *RLC* or 2-D *RLCG* parameters of a structure.

III. *RLC* EXTRACTION OF A SINGLE 3-D VIA

Multiple 3-D via configurations have been simulated with and without the ground plane as illustrated in Fig. 1. These configurations include signal propagation from T1 to T2, T2 to T3, and T1 to T3. The 2 μm thick aluminum ground plane is located at the top of the silicon substrate. Results from these simulations are listed in Table I.

Tabulated results indicate that, in all cases, the *L/R* time constant is approximately four orders of magnitude greater than the *RC* time constant. In addition, the ground plane does not affect both the resistance and inductance, but the total via capacitance is significantly affected, with the capacitance increasing by as much as 37%. For this reason, the *L/R* time constant remains relatively unchanged with a maximum variation of 1.4%, whereas the *RC* time constant varies by as much as 37%.

IV. *RLC* COUPLING BETWEEN TWO 3-D VIAS

Once a single 3-D via is electrically characterized, the capacitive and inductive coupling between two 3-D vias can be investigated. This analysis has been performed on various configurations with increasing separation between the two 3-D vias. A ground plane is present in all cases. A graphical depiction of the simulation setup and the extracted *RLC* impedances are illustrated in Fig. 2a. Extracted impedances for varying separation between the two 3-D vias are listed in Table II.

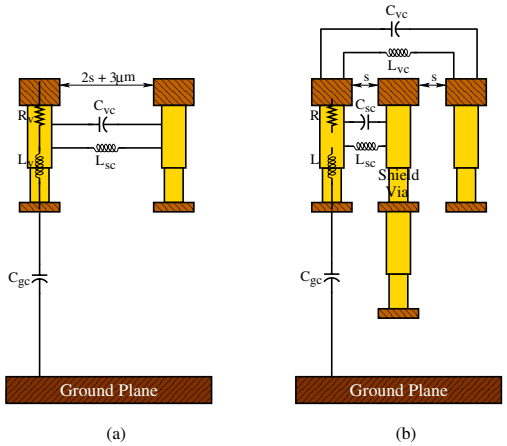

Fig. 2. Circuit model for *RLC* extraction of a) two 3-D vias and b) two 3-D vias with a shield via between the two signal vias.

The tabulated results reveal several interesting characteristics in addition to the expected trend of decreasing coupling capacitance (C_{vc}) and inductance (L_{vc}) with increasing via separation. As the separation between the two 3-D vias increases, the AC resistance, AC self inductance (L_v), and capacitance of the vias approaches the extracted values listed in Table I for a single 3-D via. The DC resistance and self inductance (L_v) are not affected by the physical separation, and are therefore equivalent to a single 3-D via. Simulations of the inter-plane coupling reveal a similar characteristic where the *RLC* impedance approaches the values extracted for a single 3-D via with increasing spacing. Assuming an ideal oxide-to-oxide bond between wafers, the inter-plane coupling (the row labeled as T2T3-T1T2 in Table II) indicates that this form of coupling can not be neglected. Comparing the results for T2T3-T2T3 with T2T3-T1T2, the extracted electrical parameters converge to a similar value with increasing spacing, which supports the need to properly model the inter-plane coupling.

The loop inductance is also included in Table II. The loop inductance is,

$$L_{loop} = L_{11} + L_{22} - 2 \times L_{21}, \tag{1}$$

where L_{11} and L_{21} are, respectively, L_v and L_{vc} from Table II. The self-inductance of the second via L_{22} is not included in either Fig. 2 or Table II, but can be determined from (1). If the two 3-D vias connect the same two planes, (1) reduces to

$$L_{loop} = 2 \times L_{11} - 2 \times L_{21}, \tag{2}$$

since both vias have approximately the same self-inductance.

V. EFFECTS OF 3-D VIA PLACEMENT ON SHIELDING

A primary focus of section IV is to examine the extracted coupling capacitance and inductance between two 3-D vias as a function of the physical spacing. The effect of inserting a

TABLE I

EXTRACTION OF *RLC* IMPEDANCES AND RELATED TIME CONSTANTS FOR A SINGLE 3-D VIA.

				DC *RL*		AC *RL* (1 GHz)		DC time constants		AC time constants	
	Configuration	C_t (fF)	C_{gc} (fF)	R (mΩ)	L (pH)	R (mΩ)	L (pH)	τ_{RC} (fsec)	$\tau_{L/R}$ (psec)	τ_{RC} (fsec)	$\tau_{L/R}$ (psec)
With ground plane	T1T2	1.43	1.28	147.55	3.93	165.92	2.93	0.21	26.62	0.24	17.68
	T2T3	1.34	1.39	152.14	4.68	171.69	3.52	0.20	30.74	0.23	20.52
	T1T3	2.04	1.89	296.17	10.6	335.10	8.51	0.60	35.87	0.68	25.38
Without ground plane	T1T2	1.15	-	147.62	3.92	165.85	2.92	0.17	26.56	0.19	17.58
	T2T3	1.16	-	151.35	4.69	170.33	3.45	0.18	31.01	0.20	20.25
	T1T3	1.49	-	296.44	10.7	335.21	8.45	0.44	35.92	0.50	25.22

TABLE II

EXTRACTION OF *RLC* PARAMETERS FOR INCREASING SEPARATION BETWEEN TWO 3-D VIAS.

					DC *RL*				AC *RL* (1 GHz)			
Configuration	Separation (μm)	C_t (fF)	C_{vc} (fF)	C_{gc} (fF)	R (mΩ)	L_v (pH)	L_{vc} (pH)	L_{loop} (pH)	R (mΩ)	L_v (pH)	L_{vc} (pH)	L_{loop} (pH)
T2T3-T2T3	1	2.05	1.16	0.87	152.36	4.69	2.05	5.27	173.71	3.40	1.63	3.55
	3	1.58	0.60	0.97	152.12	4.70	1.52	6.35	172.12	3.49	1.22	4.54
	5	1.45	0.42	1.05	152.23	4.69	1.20	6.99	171.93	3.51	0.97	5.08
	7	1.40	0.31	1.04	152.03	4.69	0.98	7.41	171.88	3.52	0.80	5.44
	9	1.34	0.25	1.04	152.04	4.69	0.84	7.71	171.58	3.53	0.68	5.68
	11	1.32	0.20	1.10	152.31	4.69	0.72	7.94	171.89	3.53	0.59	5.88
	13	1.31	0.17	1.11	152.10	4.70	0.64	8.12	171.73	3.53	0.52	6.01
T2T3-T1T2	1	1.57	0.51	1.02	152.27	4.69	1.07	6.49	171.91	3.52	0.90	4.68
	3	1.43	0.33	1.06	152.31	4.69	0.91	6.80	171.88	3.52	0.76	4.95
	5	1.39	0.26	1.12	152.20	4.69	0.79	7.04	171.77	3.52	0.65	5.16
	7	1.37	0.20	1.14	152.17	4.70	0.69	7.24	171.69	3.52	0.57	5.33
	9	1.37	0.16	1.16	152.28	4.70	0.62	7.39	171.79	3.52	0.51	5.46
	11	1.28	0.14	1.10	152.14	4.70	0.55	7.52	171.65	3.52	0.45	5.57
	13	1.35	0.11	1.22	152.32	4.69	0.50	7.62	171.85	3.53	0.41	5.66

shield via between two signal vias on the coupling capacitance and inductance is discussed in this section. The simulation setup is depicted in Fig. 2b, and the resulting extracted parameters are listed in Table III.

The reduction in capacitance is determined by noting the difference in coupling capacitance between two 3-D vias without the shield and two equally spaced vias but with a shield via placed between the two 3-D vias. This quantity is compared to the coupling capacitance between the two vias without the shield. The coupling capacitance of a 1 μm space with a shield is compared to a 5 μm space with no shielding (see Table II). The capacitive coupling (C_{vc}) between two signal vias is reduced by as much as 77% by including a third shield via. In addition, the effectiveness of the shield diminishes with increasing spacing, as additional electrical field lines terminate on the second signal line. Alternatively, the inductive coupling (L_{vc}) between the two signal lines increases due to the high mutual inductance between the shield and signal vias. The negative inductance values listed in Table III indicate this increase in inductive coupling. Note that the increase in inductance when a shield via is inserted only applies to the AC inductance, and that the maximum rise in inductive coupling is about 4.3%. As mentioned previously, an increase in the mutual inductance produces a decrease in the loop inductance. The effect of the return path on both the DC and AC inductance is described in the following section.

VI. EFFECT OF THE RETURN PATH ON THE 3-D VIA INDUCTANCE

The return path can significantly affect the induced loop inductance. In addition, the distance between the signal via and the return path also contributes to the loop inductance. As the space between the signal and return path increases, the mutual inductance (L_{21}) decreases. From (1), a decrease in the mutual inductance increases the loop inductance. An analysis of a three T2T3 3-D via structure illustrates the effect of the return path: with the return path through the middle via (see Fig. 3a) and with the return path through a side via (see Fig. 3b). The inductance listed in Table IV only includes a single row of the 3x3 matrix formed with these three conductors, corresponding to the self (L_{11}) and mutual (L_{12} and L_{13}) inductance of conductor 1 shown in Fig. 3. The remaining two rows are the self and mutual inductances of the other two conductors.

These results are listed in Table IV, and are briefly addressed here. Placing the return path between the other two 3-D vias induces two symmetric inductance loops as indicated by the similar loop inductances in the row labeled, "return path conductor 2" in Table IV. Alternatively, placing the return path on either side of the three 3-D via system produces a 32% increase in the loop inductance between the two side vias. The mutual loop inductance between the two loops (L_{loop21}) increases by as much as 96% when the return path is placed on a side via rather than the central via. Based on these results, proper placement of the return paths is critical in minimizing the loop inductance of a 3-D via.

VII. CONCLUDING REMARKS

Electrical characterization of a single via for several 3-D via configurations is described in this paper. The *L/R* time constant is shown to dominate the *RC* time constant, implying that a 3-D via is inductively limited. Analysis of a two 3-D via system reveals that with increasing spacing between the two vias, the *RLC* impedances approach those of a single 3-D via. In addition, the analysis of two 3-D via systems verifies that inter-plane coupling must be considered when properly modeling 3-D integrated structures. The effects of placing a shield via between two signal vias on both the

TABLE III

L AND C SHIELDING WITH THE ADDITION OF A THIRD SHIELD VIA.

Configuration	Separation (μm)	C_t (fF)	C_{vc} (fF)	% C_{vc} shielded	DC L			AC L		
					L_v (pH)	L_{vc} (pH)	% L_{vc} reduced	L_v (pH)	L_{vc} (pH)	% L_{vc} reduced
T2T3-T1T3-T2T3	1	2.07	0.107	74.39%	4.68	1.19	0.63%	3.40	1.01	-4.30%
	2	1.73	0.093	70.29%	4.69	0.98	0.17%	3.46	0.82	-2.52%
	3	1.58	0.079	68.94%	4.68	0.83	0.40%	3.50	0.69	-1.33%
	4	1.50	0.069	65.79%	4.68	0.72	-0.01%	3.51	0.59	-1.05%
	5	1.39	0.056	66.13%	4.69	0.64	-0.16%	3.52	0.52	-0.39%
T2T3-T1T3-T1T3	1	2.07	0.059	76.92%	4.69	0.79	0.37%	3.41	0.67	-2.74%
	2	1.74	0.054	73.35%	4.69	0.69	0.40%	3.47	0.58	-2.00%
	3	1.59	0.049	69.58%	4.69	0.61	0.24%	3.50	0.51	-1.08%
	4	1.51	0.044	67.68%	4.69	0.55	0.19%	3.51	0.46	-1.00%
	5	1.42	0.037	66.71%	4.68	0.50	0.23%	3.52	0.41	-0.43%

TABLE IV

INDUCTIVE COUPLING AND LOOP INDUCTANCE FOR THREE T2T3 3-D VIAS.

	Separation (μm)	DC L			AC L (1 GHz)		
		L_{11} (pH)	L_{21} (pH)	L_{31} (pH)	L_{11} (pH)	L_{21} (pH)	L_{31} (pH)
Partial inductances	1	4.69	2.05	1.20	3.36	1.57	0.99
	2	4.69	1.75	0.98	3.44	1.36	0.81
	3	4.69	1.51	0.84	3.47	1.19	0.68
	4	4.69	1.34	0.72	3.49	1.06	0.59
	5	4.69	1.19	0.65	3.50	0.95	0.52
	Separation (μm)	DC L			AC L		
		L_{loop1} (pH)	L_{loop2} (pH)	L_{loop21} (pH)	L_{loop1} (pH)	L_{loop2} (pH)	L_{loop21} (pH)
Return path conductor 2	1	5.28	5.28	1.79	3.51	3.51	1.13
	2	5.90	5.89	2.19	4.11	4.10	1.48
	3	6.36	6.36	2.50	4.52	4.52	1.74
	4	6.71	6.71	2.75	4.82	4.84	1.93
	5	6.99	6.99	2.94	5.07	5.07	2.09
Return path conductor 3	1	6.70	5.28	3.50	4.75	3.51	2.37
	2	7.41	5.89	3.70	5.25	4.10	2.62
	3	7.71	6.36	3.86	5.57	4.53	2.79
	4	7.93	6.71	3.97	5.80	4.84	2.91
	5	8.11	6.99	4.05	5.97	5.07	2.98

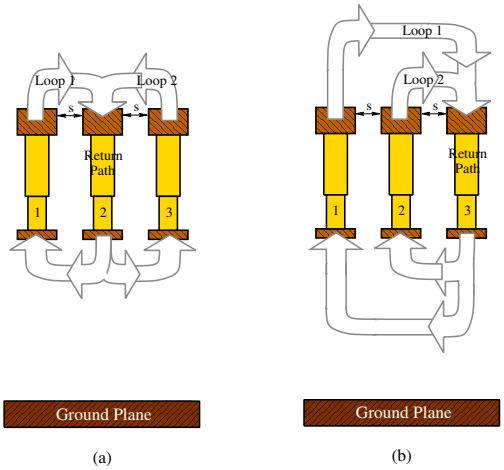

Fig. 3. Effect of return path on the loop inductance for a) a return path placed on 3-D via 2 and b) a return path placed on 3-D via 3.

coupling capacitance and mutual inductance has also been investigated. A shield via decreases the capacitive coupling by as much as 77%, while producing an increase in the inductive coupling by approximately 4.3%. Properly placing the return path reduces both the loop inductance and the mutual loop-to-loop inductance.

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