Electrical Performance and Reliability Characterization of a SiC MOSFET Power Module With Embedded Decoupling Capacitors

Li Yang, Ke Li, Jingru Dai, Martin Corfield, Anne Harris, Krzysztof Paciura, John O'Brien, and C. Mark Johnson

***Abstract*—Integration of decoupling capacitors into silicon carbide (SiC) metal oxide semiconductor field effect transistor (MOSFET) modules is an advanced solution to mitigate the effect of parasitic inductance induced by module assembly interconnects. In this paper, the switching transient behavior is reported for a 1.2-kV SiC MOSFET module with embedded dc-link capacitors. It shows faster switching transition and less overshoot voltage compared to a module using an identical package but without capacitors. Active power cycling and passive temperature cycling are carried out for package reliability characterization and comparisons are made with commercial Si and SiC power modules. Scanning acoustic microscopy images and thermal structure functions are presented to quantify the effects of package degradation. The results demonstrate that the SiC modules with embedded capacitors have similar reliability performance to commercial modules and that the reliability is not adversely affected by the presence of the decoupling capacitors.**

***Index Terms*—Embedded capacitor, metal oxide semiconductor field effect transistor (MOSFET) module, silicon carbide, switching performance, thermo-mechanical reliability.**

I. Introduction

In RECENT years, silicon carbide (SiC) metal oxide semiconductor field effect transistor (MOSFET) power modules have been developing rapidly due to the increasing demand for hybrid electric vehicles/electric vehicles as well as compact solutions for solar inverters, industrial drives, and high-frequency power supplies. SiC MOSFETs have lower power losses compared to insulated gate bipolar transistors (IGBTs). Hence, they offer the potential to increase converter efficiency. As a result, the capacity and cost of the cooling system can be reduced [1]. The improved switching losses enable operation at very high switching frequencies. This allows a reduction in the physical size of magnetic components used in the input/output filter, which in turn reduces the volume and increases the power density of the converter [2]. In addition, the intrinsic body diode can provide the function of an antiparallel diode making it possible to reduce the assembly part, which cuts costs and mitigates implied reliability concerns from additional interconnects such as wire bonds and die attach. In order to fully exert potential benefits proffered by wide band-gap semiconductors, integration techniques, commutation process, and packaging reliability need to be compatible with the device development.

With fast switching speed, the stray inductance induced by the bond wires or connection pins could cause overshoot and high-frequency parasitic ringing oscillation on the drain–source voltage or gate–source voltage [3]–[5]. Various solutions have been proposed in an effort to reduce the switching parasitic inductance in the current commutation pass. These include rearranging substrate copper trace layout and wire pattern, optimizing packaging design with low dc-link inductance, or replacement of bond wires and bus bars [5]–[9]. The other solution is the integration of dc capacitors inside the power module. This configuration provides a low loop inductance for the current commutation loop and thus minimizes the dc-side parasitic inductance [10], [11]. A few recent studies reporting on integrating capacitors in a SiC MOSFET module mainly focused on module design and electrical characterization [12]–[15]. Thermo-mechanical reliability with respect to module integration was not addressed.

In this work, electrical performance and assembly integration reliability of a 1.2-kV SiC MOSFET module with embedded decoupling capacitors are investigated. Switching transient behavior is compared between two modules in the identical package, one with embedded capacitors and the other one without. Active power cycling and passive temperature cycling, supported by transient thermal impedance characterization and scanning acoustic microscopy (SAM), are used to evaluate key degradation mechanisms. The thermal structure function is analyzed to elucidate the degradation in the heat flow path inside the module. In addition, the capacitance of the integrated capacitor is characterized before and after cyclic stress.

Manuscript received August 24, 2017; revised December 29, 2017; accepted February 12, 2018. Date of publication March 15, 2018; date of current version September 28, 2018. Recommended for publication by Associate Editor Simon S Ang. *(Corresponding author: Li Yang.)*

L. Yang, K. Li, J. Dai, M. Corfield, and C. M. Johnson are with the Electrical and Electronic Engineering Department, University of Nottingham, Nottingham NG7 2RD, U.K. (e-mail: li.yang@nottingham.ac.uk; ke.li@nottingham.ac.uk; eexjd11@nottingham.ac.uk; martin.corfield@nottingham.ac.uk; mark.johnson@nottingham.ac.uk).

A. Harris is with Dynex Semiconductor Limited, Lincoln LN6 3LF, U.K. (e-mail: anne.harris@dynexsemi.com).

K. Paciura and J. O'Brien are with Cummins Power Generation, Stamford PE9 2NB, U.K. (e-mail: krzysztof.paciura@cummins.com; john.obrien@cummins.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2018.2809923

This work is licensed under a Creative Commons Attribution 3.0 License. For more information, see http://creativecommons.org/licenses/by/3.0/

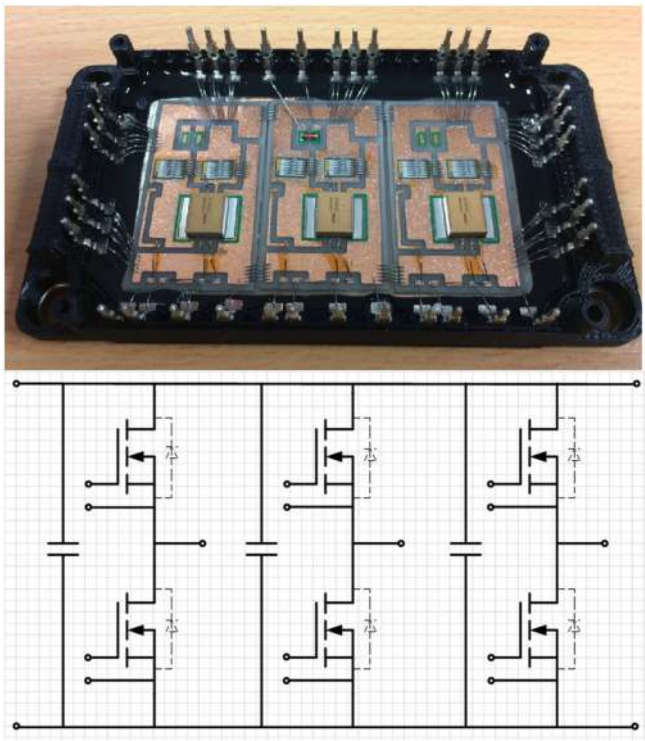


Fig. 1. Photo and electrical circuit diagram of the SiC MOSFET module under study.

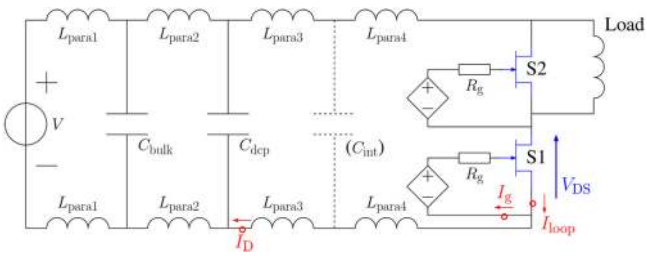


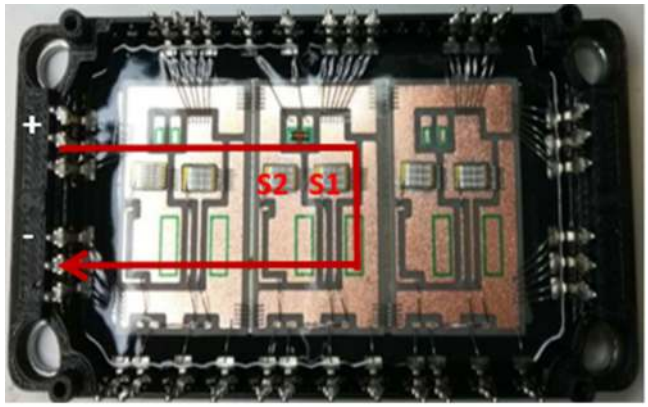
Fig. 2. Electrical circuit to measure device switching current and voltage.

II. Electrical Performance

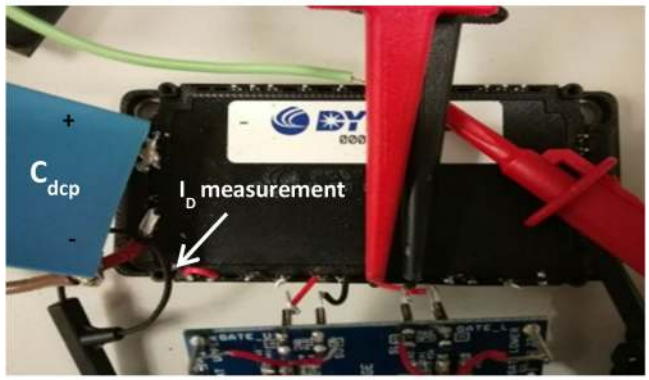
A. Switching Characterization Test Setup

The module under study incorporates a three-phase inverter in a single package with a full-bridge configuration and is equipped with integrated dc ceramic capacitors (CeraLink, 0.25 μF, 900 V) across each phase leg [16]. Each switch is composed of one CREE CPM2-1200-0025B SiC chip (1200 V, 98 A). Six chips are soldered onto three direct bonded copper (DBC) substrates, which are soldered down onto a copper baseplate. There are no antiparallel diodes enclosed in the module. Dimension of the baseplate is 113 mm $\times$ 55 mm. A photo and electrical circuit diagram of the module are presented in Fig. 1.

The switching transient characterization is carried out for two modules, labeled as PM_1, the module without capacitors, and PM_2_C_{int} that has integrated capacitors. They are assembled with the identical packaging. Fig. 2 shows the electrical circuit for the measurement of switching current and voltage waveforms. It is mainly constituted by a half-bridge with two



(a)



(b)

Fig. 3. (a) Module without capacitor. (b) Measurement circuit.

SiC MOSFET switches S1 and S2, an inductive load, an external decoupling capacitor (C_{dcp}) and a bulk capacitor (C_{bulk}) linking the power supply and C_{dcp}. Switching characterization is carried out on switch S1, and S2 is switched OFF.

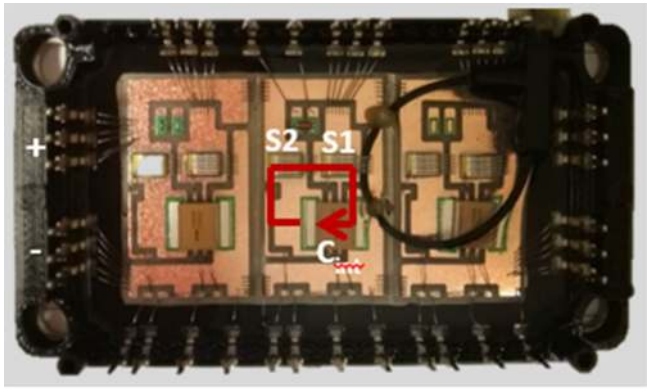
Fig. 3(a) shows the internal layout of prototype PM_1. As the decoupling capacitor C_{dcp} is connected externally to the module, a Rogowski coil is attached through the module terminal pins to measure the device switching current I_D [see Fig. 3(b)], where the measurement position is indicated as I_D in Fig. 2.

Fig. 4(a) shows the internal layout of prototype PM_2_C_{int}. A Rogowski coil is wound around the bonding wires of device S1 in order to measure its switching current. Under this condition, the measurement position is indicated as I_{loop} in Fig. 2, which shows that the current i_{loop} measured by the Rogowski coil in the module includes device gate loop current i_g. In order to obtain the device switching current i_D ($i_D = i_{\text{loop}} - i_g$) and compare it with the above-mentioned condition, i_g is measured by another identical Rogowski coil, as shown in Fig. 4(b).

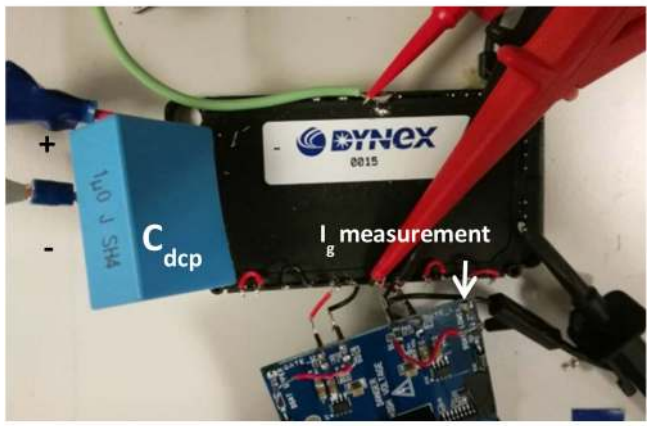
In Figs. 3(a) and 4(a), the device switching loop is marked with red lines, and it can be seen that the switching loop in the power module that has the integrated capacitors is smaller than the one without capacitors.

B. Comparison in Switching Transients

The used Rogowski coil (CWTUM/06/R) has a bandwidth of 30 MHz and the peak *di/dt* measurement rate of 70 kA/μs,



(a)



(b)

Fig. 4. (a) Module with the integrated capacitors. (b) Measurement circuit.

TABLE I
COMPARISON OF E_{ON} AND E_{OFF} OF TWO POWER MODULES

	PM_1 without C_{int}	PM_2 with C_{int}
E_{ON} (μJ)	90	450
E_{OFF} (μJ)	607	539

while the oscilloscope (DPO4104B) has a bandwidth of 1 GHz. The switching waveforms of drain current i_D and drain–source voltage V_{DS} are recorded at 600 V and 30 A, which are displayed in Fig. 5. From the turn-ON waveforms [see Fig. 5(a)], it can be seen that the drain current i_D of PM_2_C_{int} shows faster damping compared to PM_1. Also, PM_2_C_{int} has a current transition rate of 2.5 A/ns, which is faster than that of PM_1 (2 A/ns).

The turn-OFF waveforms for both modules are presented in Fig. 5(b). Comparing with PM_1, the overshoot voltage of PM_2_C_{int} is 108 V less. Meanwhile, the resonance frequency at the end of the switching is around 25 MHz for PM_1 and 100 MHz for PM_2_C_{int}.

Based on device switching waveforms shown in Fig. 5, device switching losses (E_{ON} and E_{OFF}) are obtained for the two power modules and they are listed in Table I.

It is found that E_{OFF} of PM_1 is higher than that of PM_2, because of higher overshoot V_{DS} voltage during device turn-OFF transition. However, E_{ON} of PM_1 is much lower than that of PM_2. This is supposedly due to the snubber effect of increased

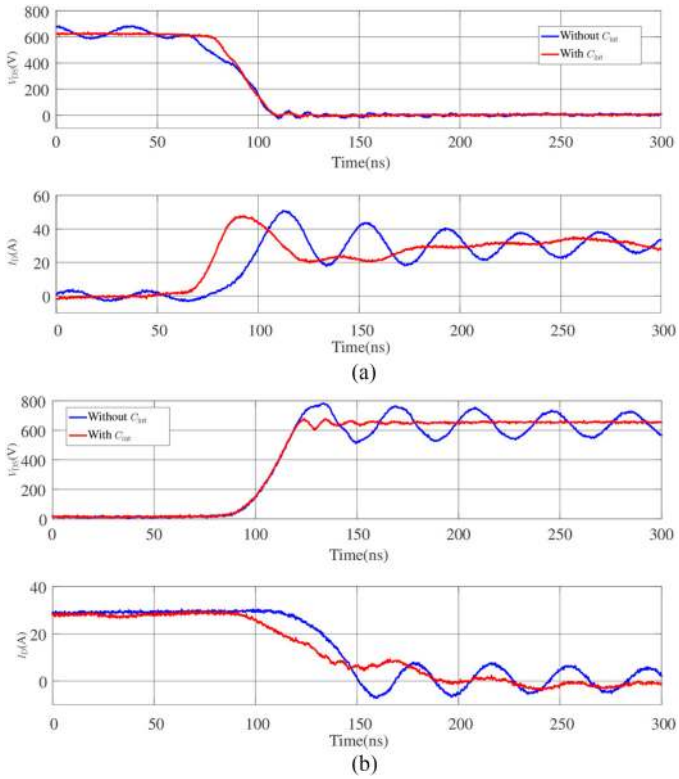


Fig. 5. (a) Turn-ON transient waveforms. (b) Turn-OFF transient waveforms.

L_{para} value in the power loop of PM_1. At turn-ON switching, during the rise of I_D, bigger value of L_{para} gives rise to a higher voltage drop $L_{para}\frac{di}{dt}$ of device V_{DS} voltage, which decreases I_D, V_{DS} overlapping surface and time. This result corresponds with the results among E_{ON}, E_{OFF}, and L_{para} presented by Wang *et al*. [17] for SiC MOSFET. The comparison of device switching losses shows that there might be less switching losses of devices in PM_1. However, as device switching loop increases in PM_1, parasitic resistance value is bigger in PM_1 than that in PM_2, which causes more losses of the whole current conduction loop in PM_1 than those in PM_2.

It needs to be noted that even though PM_2_C_{int} encloses decoupling capacitors, C_{dcp} is still necessary for the measurement in order to avoid a lower resonance frequency between C_{int} and the lumped parasitic inductance C_{bulk} in the loop (L_{para2} + L_{para3} shown in Fig. 2), which may be observed if loop resistance is inferior to $\sqrt{(L_{para2}+L_{para3})/C_{int}}$. This lower frequency resonance ($f=\frac{1}{2*\pi*\sqrt{(L_{para2}+L_{para3})*C_{int}}}$) may lead to another V_{DS} overshoot voltage. More discussions on different resonance frequencies observed in device switching can be found in [18]. A comparison of the V_{DS} switching waveform in the PM_2_C_{int} module with and without C_{dcp} is shown in Fig. 6. It can be seen that using 1 μF C_{dcp} helps to damp the 793-kHz lower frequency resonance.

In summary, the module with integrated capacitors suppresses the parasitic inductance within the device switching loop, which results in faster switching transition and less overshoot voltage. It is worth pointing out that the Ceralink capacitors, which employ an antiferroelectric dielectric, have strong voltage and

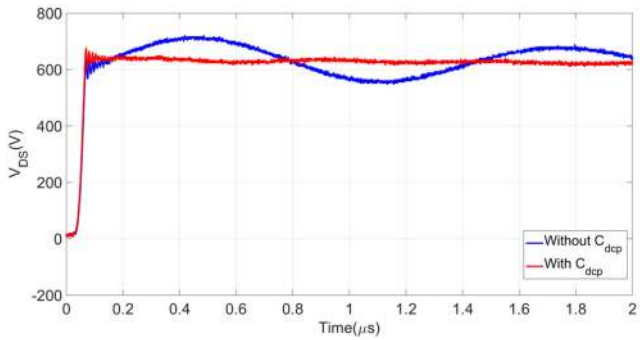


Fig. 6. Device V_{DS} waveform comparison in the PM_2_C_{int} module with and without C_{dcp}.

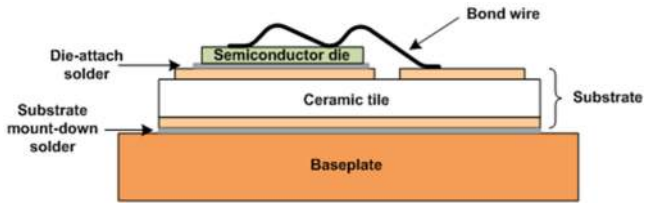


Fig. 7. Schematic cross section of the module assembly structure.

TABLE II
MATERIALS AND THICKNESS OF THE SUBSTRATE MOUNT-DOWN LAYERS FOR THE IGBT AND MOSFET MODULES

	Commercial Si IGBT module	SiC MOSFET module prototype
Substrate	Al_2O_3 (1 mm)	AlN (1 mm)
Substrate mount-down solder	Eutectic SnAg (0.4 mm)	SnSb5 (0.2 mm)
Baseplate	Copper (3 mm)	Copper (2.8 mm)

temperature capacitance sensitivities. However, in this decoupling application, the primary function is to provide a low-impedance, high-frequency return path for the commutation loop, so the actual capacitance value has a relatively small effect on the measured response.

III. RELIABILITY CHARACTERIZATION

A. Passive Temperature Cycling Test

1) Passive Cycling Experimental Setup: The two modules PM_1 and PM_2_C_{int} were placed in an ESPEC three-zone environmental thermal shock test chamber. The baseplate temperature ranges from –55 °C to +90 °C. Each cycle had a period of 20 min with a heating time and cooling time at 10 min.

SAM characterization was carried out using PVA TePla AM300. C-mode scanning (interface scan) was conducted with a 35-MHz transducer to provide a planar view on several focused depths corresponding to specific internal layers. This creates two-dimensional grayscale images from the reflected ultrasonic echoes, in which discontinuities show different brightness from the intact area. The modules were imaged prior to cycling (under as-received condition) in order to provide a basis for comparison. The same samples were subsequently imaged at 1000, 1490, 2516, 5750, and 9317 cycles.

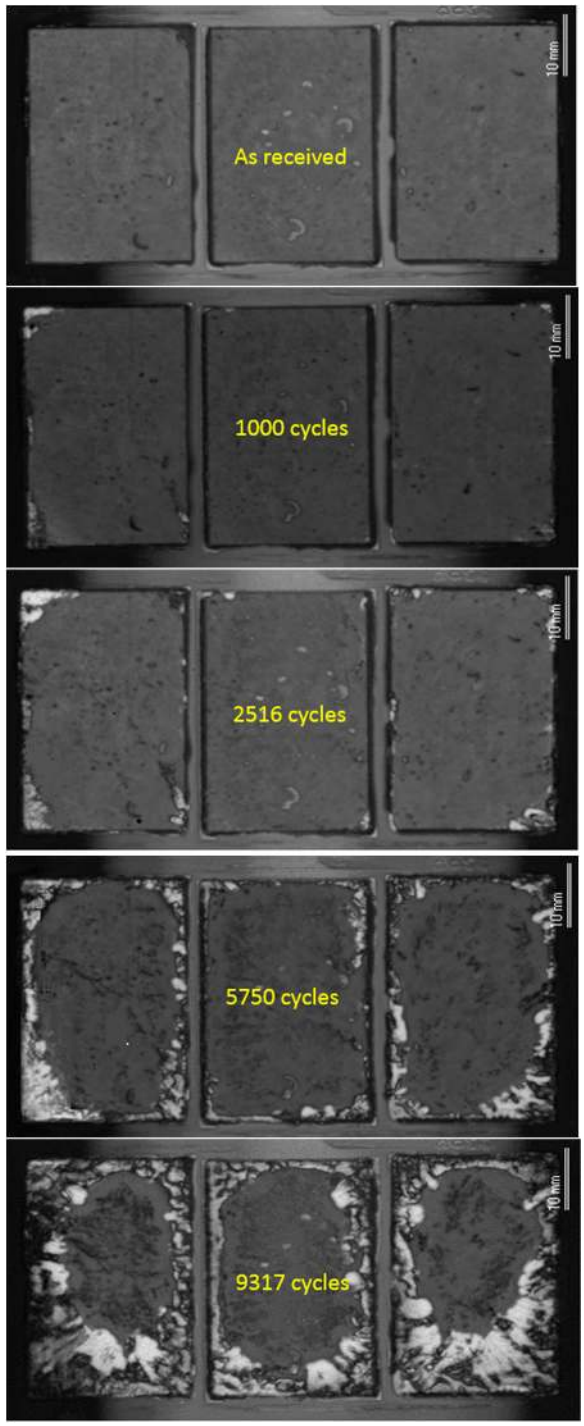


Fig. 8. SAM images showing delamination of the substrate mount-down solder layer for the SiC module with embedded capacitors during the passive temperature cycling test.

2) SAM Tomography Images and Comparisons: A schematic cross section of the module assembly structure is presented in Fig. 7. In Fig. 8, SAM images for the substrate ceramic layer are displayed for PM_2_C_{int}. A growing white area indicates delamination in the module substrate mount-down solder as the temperature cycling progressed. It initiated

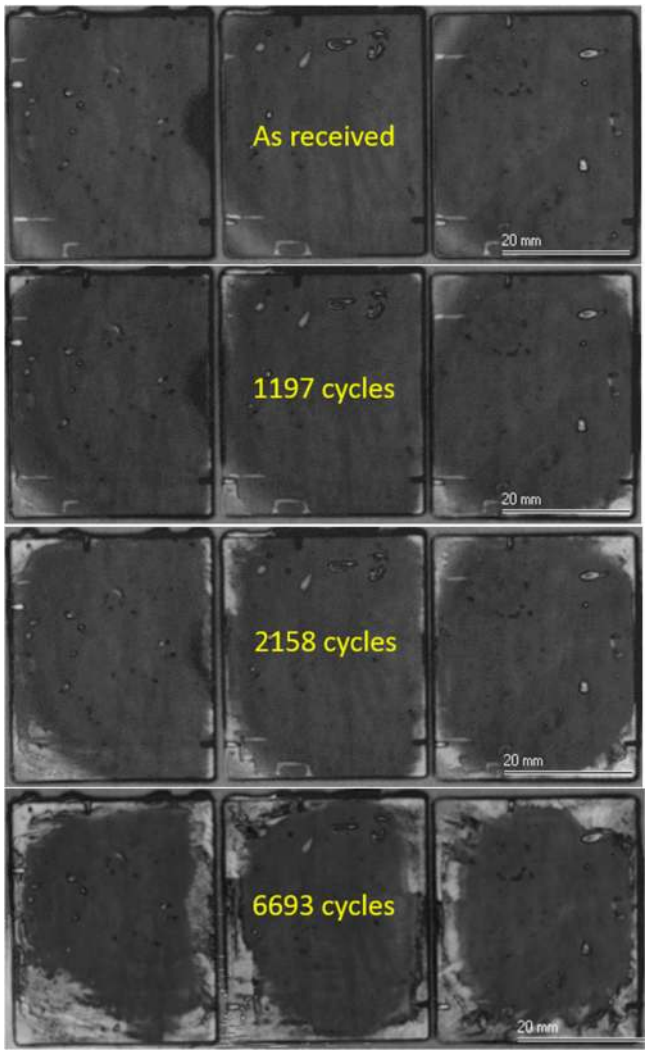


Fig. 9. SAM images showing delamination of the substrate mount-down solder layer for commercial IGBT1 during the passive temperature cycling test.

from the edge of the solder layer and propagated toward the center.

For comparison, two commercial three-phase Si IGBT modules with a similar substrate mount-down structure were subjected to passive cycling over the same temperature regime. Materials and layer thickness of the substrate mount-down layers for Si IGBT and SiC MOSFET prototype modules are listed in Table II. The SAM images for the substrate ceramic layer are presented in Fig. 9 for one of the commercial IGBT modules.

The SAM images are transformed into a binary image in MATLAB where the white pixels indicate the attached area on the substrate tile and the black pixels indicate the cracked area. In this way, the attached area of the substrate tile mount-down solder can be estimated as a percentage of the total area. Fig. 10 shows the estimated percentage of the attached area of the solder layer at different cycle numbers for the two modules during the cycling test assuming that three substrate tiles are completely attached onto the baseplate before cycling. After 9317 cycles, approximately 57% and 50% solder area remains attached for PM_1 and PM_2_C_{int}, respectively. The evolution of the attached

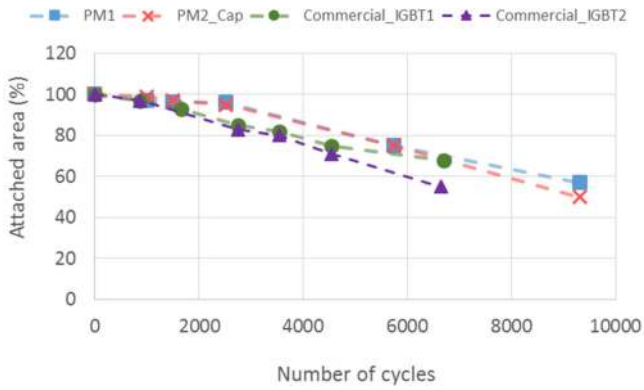


Fig. 10. Estimated attached area of the substrate mount-down solder as a percentage of the total area during temperature cycling of –50 °C to 90 °C.

area of the substrate mount-down solder for the two commercial IGBT modules shows a similar degradation rate to the two SiC MOSFET module prototypes.

3) Characterization of the Embedded Capacitors: To verify the integrity of the embedded decoupling capacitor, the capacitance value was measured before and after cycling using an impedance analyzer at 1 kHz and with a dc bias voltage of 0 V. Before cycling, the measured capacitance is around 137 nF and it remained unchanged after 9317 temperature cycles.

B. Active Power Cycling Test

1) Power Cycling Experimental Setup: To further investigate the module packaging reliability, the SiC MOSFET module with embedded capacitors is undertaken power cycling test using a "MentorGraphics" Power Tester 1500 A [13]. During cycling, the module was mounted on a water-cooled cold plate with a 50-μm-thick Kapton film as the thermal interface between the cold plate and the baseplate. The use of the Kapton film increases the case-to-ambient thermal resistance in order to achieve a larger temperature swing at the substrate–case interface accelerating degradation of the internal thermal path. Forward voltage drop of the body diode V_f was used as a thermosensitive electrical parameter to estimate the module junction temperature. A calibration of V_f as a function of temperature was prepared in advance.

At the heating stage, all six MOSFETs are switched ON with a +15 V gate bias voltage and a constant total heating current of 153 A flows through all six devices (in three parallel branches), generating a power dissipation of 890 W. At the end of the heating phase, the MOSFETs are switched OFF with a –5 V gate bias and the heating current is removed. The heating time and cooling time are fixed at 8 and 22 s, respectively. During cycling, the ON-state voltage and maximum/minimum junction temperature of the six MOSFET devices are monitored individually. The maximum temperature for the six MOSFETs varies between 137 °C and 154 °C, while cold plate temperature was maintained at 10 °C. An average junction temperature swing from 21 °C to 147 °C ($\Delta T = 126$ °C) was achieved across the six devices.

The power cycling test was terminated at 4728 cycles when the ON-state voltage increased by 16%. Fig. 11 shows the record of ON-state voltage and maximum junction temperature for one

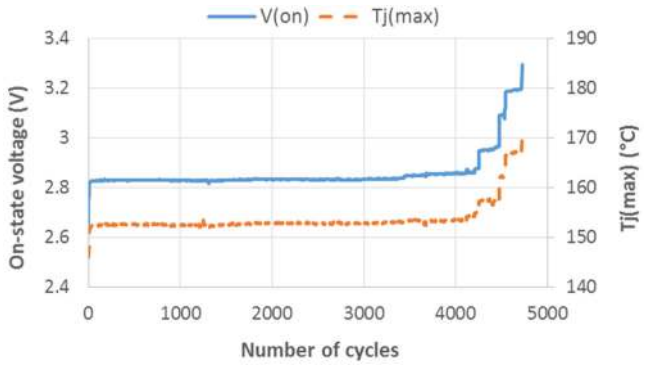


Fig. 11. Development of one MOSFET ON-state voltage during power cycling.

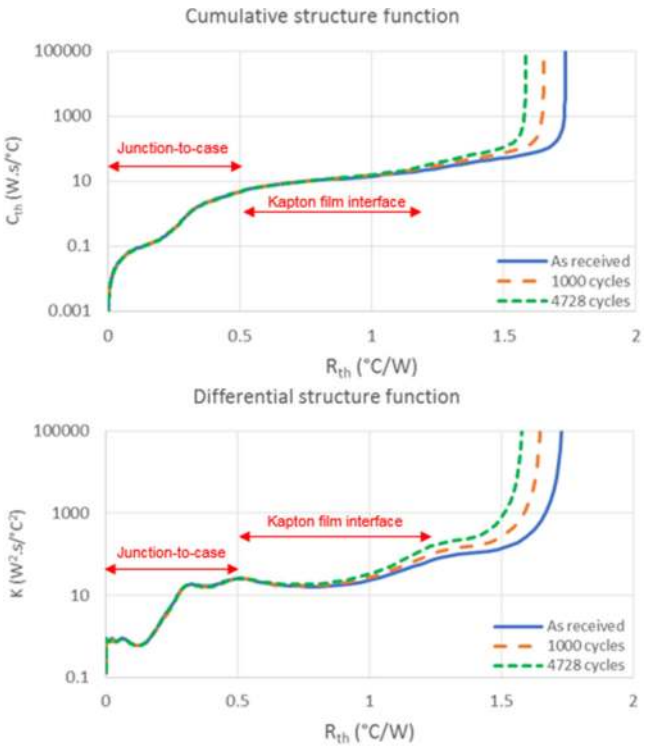


Fig. 12. Structure functions of PM_2_C_{int} during power cycling.

of the devices throughout the cycling. They kept unchanged until around 3400 cycles. Significant incremental steps started from 4200 cycles. And the staircase nature is known to be the result of wire bond lift-offs [20], [21]. Increase of the ON-state voltage leads to an increase of power loss and therefore a rise in the junction temperature.

2) Thermal Structure Function and SAM Tomography Imaging: Transient thermal impedance measurements and SAM were performed at as-received condition, at 1000 and 4728 power cycles. A total of six chips are heated up together and the thermal characterization is recorded for each chip individually. Cumulative and differential structure functions are extracted for one chip and displayed in Fig. 12. They provide a map of the heat conduction path from junction (at the origin of the resistance axis) to ambient (water), which appears as vertical lines at the right-hand side indicating infinite heat

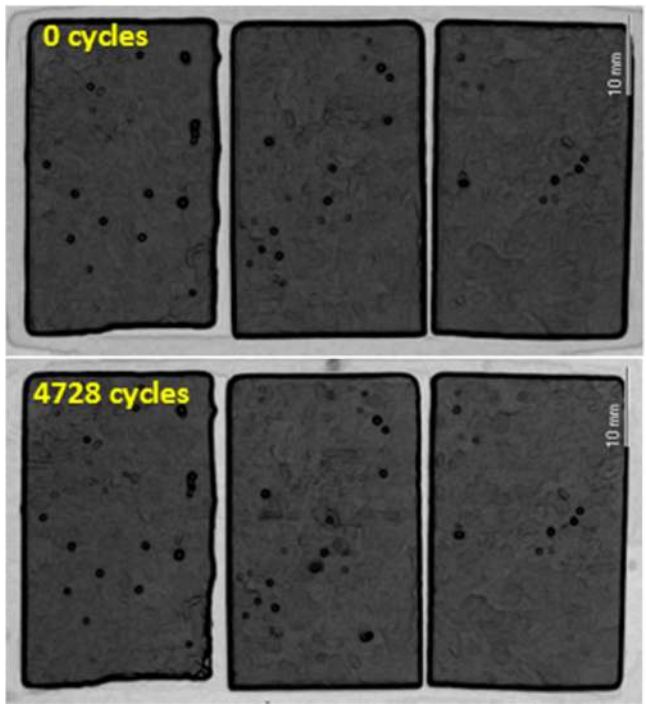


Fig. 13. SAM tomography images of the substrate mount-down solder in PM_2_C_{int}.

capacitance. The wide flat region is the thermal interface, i.e., Kapton film, which has a large thermal resistance. The variability of the junction-to-ambient thermal resistant is caused by remounting the module following SAM and also due to the inconsistent heat sink thermal resistance as a result of variable water temperature and the flow rate.

However, the junction-to-case thermal resistance R_{thjc} is not affected by these factors. It can be seen from the graph that junction-to-case resistance stays unchanged after 4728 cycles, indicating no significant reduction of the solder attach area. This agrees with the SAM tomography images of the substrate mount-down solder shown in Fig. 13.

3) Comparisons With a Commercial SiC MOSFET Module: For comparison, a commercial three-phase SiC MOSFET module with similar power ratings was tested with the same thermal interface between module baseplate and the cold plate. The module includes six SiC MOSFETs and six SiC Schottky diodes soldered on aluminum nitride (AlN) DBC substrates, which are mounted on a Cu baseplate. The antiparallel diodes were subjected to power cycling. A constant heating current of 115 A was applied and shared among three legs so the monitored forward voltage and junction temperature are a global measurement across the whole module. This led to an initial temperature swing of 13–146 °C ($\Delta T = 133\,^{\circ}\text{C}$). The module was subjected to 4152 power cycles.

Fig. 14 shows the maximum junction temperature and forward voltage (V_f) of the freewheeling diodes during the power cycling test. The forward voltage increased 9% at the end of the test. Before 4000 cycles, it increases gradually indicating growing degradation in the thermal stack. The steep increase at the end of the test is considered to be caused by the wire bond lift-offs.

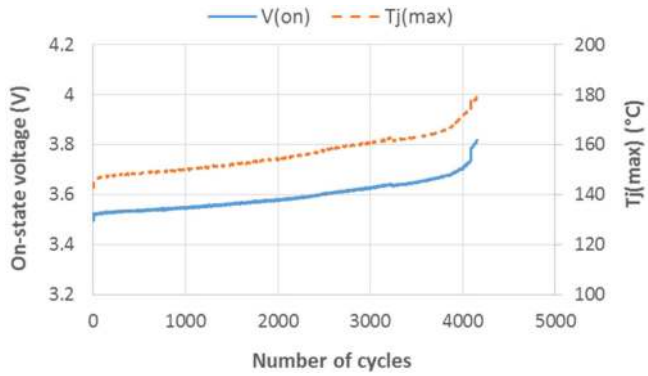


Fig. 14. Development of diode forward voltage during power cycling.

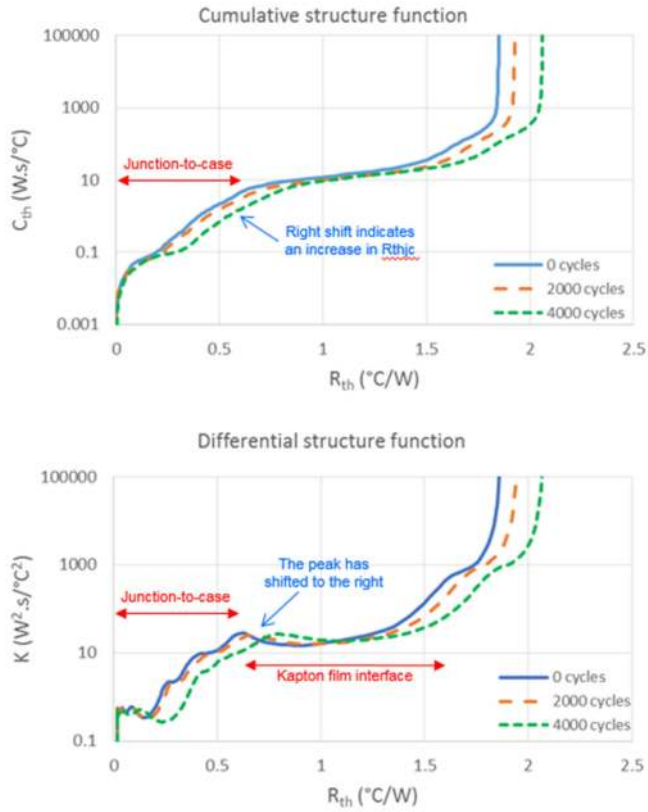


Fig. 15. Structure functions of the commercial SiC MOSFET module during power cycling.

The cumulative and differential structure function is extracted for the whole module and displayed in Fig. 15. It can be seen that the cumulative structure function has shifted to the right as the cycling number increases, which accounts for a change in the internal structure of the module resulting in an increase of junction-to-case thermal resistance [22]. In the differential structure function, each peak is related to a different material in the thermal stack and K is a value proportional to the cross-sectional area squared. Right shift of peaks indicates the increase of the thermal resistance of the assembly layers.

SAM tomography confirms that the degradation took place at the substrate mount-down solder layer, which is shown as the white area in the photo of 4152 cycles (see Fig. 16).

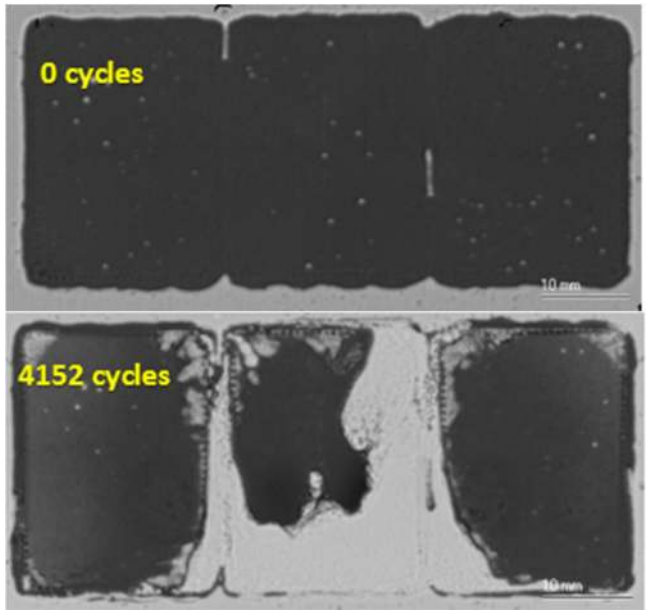


Fig. 16. SAM tomography images of the substrate mount-down solder in the commercial SiC MOSFET module.

4) Discussion: Assembly materials, layer thickness, and cycling time are all possible factors contributing to different failure modes presented in these two modules. Both the commercial SiC MOSFET module under test and PM_2_C_{int} are constructed with a Cu baseplate and AlN–copper substrate. PM_2_C_{int} has a thinner baseplate (2.8 mm) than the commercial module (3 mm), which possibly induces less strain in the substrate mount-down solder layer. Also, the substrate mount-down solder material in PM_2_C_{int} is SnSb5, which has a higher melting point and hence higher creep resistance than the eutectic SnAg used in the commercial module [23]. In addition, the power cycling time for PM_2_C_{int} is 30 s (8-second heating and 22-second cooling), which is much shorter than the cycling time for the commercial SiC MOSFET of 2 min (60-second heating and 60-second cooling). Longer cycling duration induces larger temperature swing and thus higher thermo-mechanical stress at the baseplate/substrate interface.

IV. Conclusion

In this work, a high-power SiC MOSFET module with embedded decoupling capacitors has been studied from the switching and packaging reliability perspective. Switching transient characterization of the module with integrated capacitors showed faster switching transition and less overshoot voltage compared with the same semiconductors in an identical package but without embedded capacitors, indicating suppression of the parasitic inductance within the device switching loop and thus providing favorable conditions for high-frequency operation. During active power cycling tests at comparable temperature swings, the SiC module prototype demonstrated a similar lifetime to the commercial SiC module. However, the two modules are composed of different materials and display different dominant degradation modes. During passive

temperature cycling under identical conditions, the substrate mount-down solder in the SiC module prototype showed similar degradation rate as the commercial Si-based IGBT. In addition, the capacitance of the integrated capacitor remained unchanged after cyclic passive temperature stress. Together, the tests demonstrate that the SiC MOSFET module with embedded decoupling capacitors has improved switching behavior and can be expected to display similar levels of thermo-mechanical reliability to commercial power modules.

ACKNOWLEDGMENT

This work was supported by the Engineering and Physical Sciences Research Council [grant number EP/K035304/1], (UK EPSRC) through the Centre for Power Electronics; and by the Advanced Propulsion Centre UK.

REFERENCES

[1] R. A. Wood and T. E. Salem, "Evaluation of a 1200V, 800A all-SiC dual module," *IEEE Trans. Power Electron.*, vol. 26, no. 9, pp. 2504–2511, Sep. 2011.

[2] A. Trentin, L. d. Lillo, L. Empringham, P. Wheeler, and J. Clare, "Experimental comparison of a direct matrix converter using Si IGBT and SiC MOSFETs," *IEEE J. Emerging Select. Topics Power Electron.*, vol. 3, no. 2, pp. 542–554, Jun. 2015.

[3] M. Meisser, M. Schmenger, and T. Blank, "Parasitics in power electronic modules: How parasitic inductance influences switching and how it can be minimized," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renew. Energy Energy*, Nuremberg, Germany, May 2015, pp. 1–8.

[4] O. Alatise, N.-A. Parker-Allotey, D. Hamilton, and P. Mawby, "The impact of parasitic inductance on the performance of silicon-carbide Schottky barrier diodes," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3826–3833, Aug. 2012

[5] R. Bayerer and D. Domes, "Power circuit design for clean switching," in *Proc. 6th Int. Conf. Integr. Power Electron. Syst.*, Mar. 2010, pp. 1–6.

[6] S. Li, L. M. Tolbert, F. Wang, and F. Z. Peng, "Stray inductance reduction of commutation loop in the P-cell and N-cell-based IGBT phase leg module," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3616–3624, Jul. 2014.

[7] E. Hoene, A. Ostmann, B. T. Lai, C. Marczok, A. Musing, and J. W. Kolar, "Ultra-low-inductance power module for fast switching semiconductors," in *Proc. IEEE 27th Int. Symp. Power Semicond. Devices ICs*, Nuremberg, Germany, 2013, pp. 198–205.

[8] P. Mourick, J. Steger, and W. Tursky, "750 A, 75 V MOSFET power module with sub-nH inductance," in *Proc. 14th Int. Symp. Power Semicond. Devices ICs*, 2002, pp. 109–112.

[9] B. Mouawad, J. Li, A. Castellazzi, P. Friedrichs, and C. M. Johnson, "Low parasitic inductance multi-chip SiC devices packaging technology," in *Proc. 18th Eur. Conf. Power Electron. Appl.*, Karlsruhe, Germany, Sep. 2016, pp. 1–7.

[10] M. Schmenger *et al.*, "Highly integrated power modules based on copper thick-film-on-DCB for high frequency operation of SiC semiconductors - Design and manufacture," in *Proc. 18th Eur. Conf. Power Electron. Appl.*, 2015, pp. 1–8.

[11] T. Ibuchi, E. Masuda, and T. Funaki, "A study on packaging design of SiC power module using near-field magnetic scanning techniques," in *Proc. IEEE Int. Workshop Integr. Power Packag.*, 2017, pp. 1–4.

[12] Z. Chen, "Electrical integration of SiC power devices for high-power-density applications," *Ph.D. dissertation*, Virginia Polytech. Inst. State Univ., Blacksburg, VA, USA, 2013.

[13] Z. Chen, Y. Yao, D. Boroyevich, K. D. T. Ngo, P. Mattavelli, and K. Rajashekara, "A 1200 V, 60 A SiC MOSFET multichip phase-leg module for high temperature high frequency applications," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2307–2320, May 2014.

[14] Y. Ren *et al.*, "Voltage suppression in wire-bond-based multichip phase-leg SiC MOSFET module using adjacent decoupling concept," *IEEE Trans. Ind. Electron.*, vol. 64, no. 19, pp. 8235–8246, Oct. 2017.

[15] C. Chen, Y. Chen, Y. Li, Z. Huang, T. Liu, and Y. Kang, "An SiC-based half-bridge module with an improved hybrid packaging method for high power density applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 8980–8991, Nov. 2017.

[16] CeraLinkTM capacitor for fast-switching semiconductors datasheet: TDK_01112017_Z63000Z2910Z001Z(2126)-1079719.pdf.

[17] J. Wang, H. S.-H. Chung, and R. T.-H. Li, "Characterization and experimental assessment of the effects of parasitic elements on the MOSFET switching performance," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 573–590, Jan. 2013.

[18] Z. Chen, D. Boroyevich, P. Mattavelli, and K. Ngo, "A frequency-domain study on the effect of dc-link decoupling capacitors," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2013, pp. 1886–1893.

[19] MentorGraphics. Power Tester 1500 A. [Online]. Available: http://www.mentor.com/products/mechanical/micred/power-tester-1500a/

[20] U. M. Choi, S. Jørgensen, and F. Blaabjerg, "Advanced accelerated power cycling test for reliability investigation of power device modules," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8371–8386, Dec. 2016.

[21] J. Lutz, H. Schlangenotto, U. Scheuermann, and R. D. Doncker, *Semiconductor Power Devices, Physics, Characteristics, Reliability*. Berlin, Germany: Springer-Verlag, 2011.

[22] M. A. Eleffendi, L. Yang, P. Agyakwa, and C. M. Johnson, "Quantification of cracked area in thermal path of high-power multi-chip modules using transient thermal impedance measurement," *Microelectron. Reliab.*, vol. 59, pp. 73–83, 2016.

[23] H. Mavoori and S. Jin, "Significantly enhanced creep resistance in low-melting-point solders through nanoscale oxide dispersions," *Appl. Phys. Lett.*, vol. 73, no. 16, pp. 2290–2292, 1998.

Authors' photographs and biographies not available at the time of publication.