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Electrical properties of high density arrays of silicon nanowire field effect transistors

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Proximity effect corrected e-beam lithography of hydrogen silsesquioxane on silicon on insulator was used to fabricate multi-channel silicon nanowire field-effect transistors (SiNW FETs). Arrays of 15-channels with a line width of 18 nm and pitch as small as 50 nm, the smallest reported for electrically functional devices, were fabricated. These high density arrays were back-gated by the substrate and allowed for investigation of the effects of scaling on the electrical performance of this multi-channel SiNW FET. It was revealed that the drain current and the transconductance (g_m) are both reduced with decreasing pitch size. The drain induced barrier lowering and the threshold voltage (V_{th}) are also decreased, whereas the subthreshold swing (S) is increased. The results are in agreement with our simulations of the electric potential profile of the devices. The study contains valuable information on SiNW FET integration and scaling for future devices. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4824367]

I. INTRODUCTION

The development of fin field-effect transistors (FinFETs) is pursued, as the minimum feature size of complementary metal oxide semiconductor (CMOS) devices continues to shrink down to the nanometer-scale. Top-down and bottom-up approaches using silicon on insulator (SOI) and CVD grown nanowires, respectively, have been suggested. In both cases, the production of densely packed arrays with small pitch has proven difficult. Furthermore, narrow-fin FETs have large series resistances, which result in a significant degradation of performance in the direct current operation region. Multi-fin field-effect transistors are one of the solutions proposed to improve the current drive in future devices. Therefore, studies on high density multi-fin FETs with small channel dimensions and narrow pitches are crucial for device scaling. Although several alternative nanolithographic processing schemes have been suggested, electron-beam lithography (EBL) remains one of the most reliable techniques for the generation of nanometer-scale features, in spite of its obviously low throughput. In particular, hydrogen silsesquioxane (HSQ) based resists have improved the feature sizes attainable due to their high resolution, small line edge roughness, high etch resistance, and good stability.[1,2] However, small pitch remains elusive due to proximity effects. Most reports on the electrical properties of nanoscale devices have only been demonstrated for single channel FETs[3] or with a low packing density of line patterns of the scale of a few hundred nanometers.[4,5] These studies do not provide any information on the packing density of devices.

In this paper, we report the fabrication and characterization of high density arrays of silicon nanowire field-effect transistors (SiNW FETs). The array consists of 15-channels with 18 nm line widths and pitch between 50 and 100 nm. The SiNW FET arrays were characterized structurally and their electrical performance was investigated at room temperature. This very high density of channels, one of the highest reported to date, was enabled by an optimized EBL process using HSQ resist and development in salty developer. We also present experimental results detailing the effect of pitch on the performance of SiNW FETs.

II. EXPERIMENTAL DETAILS

Silicon-on-Insulator (SOI) wafers with a 50 nm thick top layer on top of 145 nm thick buried oxide (BOX) layer were used as substrates. Both the top layer and the substrate are p-type boron doped Si, resistivity of $8.0 \sim 11.5\ \Omega$ cm. First, pre-patterns of alignment markers and probe contact pads were prepared using photolithography on SOI substrates followed by evaporation of titanium/gold (Ti/Au). Then, source and drain (S/D) metal electrodes were formed on the SOI substrates by EBL (Figure 1(a)). The width of S/D electrodes was 200 nm and the inter spacing between S/D electrodes was 500 nm. After the contact regions were defined, the native silicon oxide layer was removed with 7:1 buffered oxide etch (BOE) solution and then metal contacts were immediately evaporated with a thickness of Ti/Au = 5/15 nm.

HSQ (XR-1541 2% solids, Dow Corning) was spin-coated onto the pre-patterned substrates with a thickness of 50 nm. As the soft-bake temperature is increased, both the exposure dose and contrast decrease.[6] Thus, the resist-coated wafer was not baked in order to avoid thermally induced contrast reduction. E-beam exposure was performed with a

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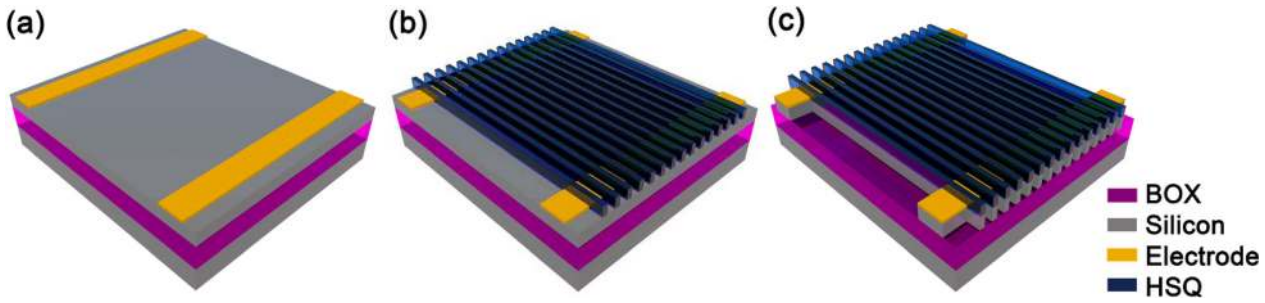

FIG. 1. Schematics of the fabrication process of an array SiNW FET. (a) Definition of S/D electrodes with positive resist by EBL and deposition of Ti/Au electrodes. (b) The HSQ patterns are formed between the S/D electrodes by EBL (c) The SiNW channels and S/D electrodes regions are etched by ICP-RIE.

Zeiss Supra 40 tool at an acceleration voltage of 20 keV with a 10 μm aperture. The beam current was ~40 pA, and the exposure patterns consisted of single-pixel-lines with various pitches.

In order to optimize the development process, two different developers were used: (A) tetramethylammonium hydroxide (TMAH). (B) An aqueous mixture of 1 wt. % sodium hydroxide (NaOH) and 4 wt. % sodium chloride (NaCl) (commonly called "salty" developer). After each development, the samples were rinsed in de-ionized (DI) water for 5 min, and then dried by gently blowing in nitrogen gas.[6,7] A post development bake was performed on a hot plate at 115 °C for 2 min. As a result, HSQ grating patterns were successfully formed on SOI substrates as shown in Figure 1(b). Both electrodes and channels were etched using an inductively coupled plasma reactive ion etch (ICP-RIE) (Oxford) of 1200 W ICP power and 30 W RIE power in 80 SCCM CHF_3, 15 SCCM SF_6 at 15 mTorr for 15 s with the substrate holder at 10 °C with 10 Torr He backside pressure (Figure 1(c)).

Scanning electron microscopy (SEM) images were acquired using a Zeiss Ultra Plus FE-SEM. Electrical characterization was carried out with a Keithley 2602 dual-channel source meter unit and a Keithley 2400 general-purpose source meter unit attached to a Suess needle prober operated at room temperature.

III. RESULTS AND DISCUSSION

A. Optimized fabrication process for high density silicon nanowire (SiNW) arrays using HSQ resist

To date, a range of different HSQ resist patterning techniques have been reported for the production of high density patterns on SOI. Normally, a thin HSQ resist layer is used to achieve a high resolution pattern because scattering effects during exposure can be reduced. Based on this thin resist method, resist structures with sub-10 nm features have been reported.[7–9] However, for transport measurements, electrical contacts must be formed on both sides of the channel. In process flows where the channel is formed first, the HSQ layer in the contact regions must be removed. This results in an undercut of the SiNW, which mechanically destabilizes the structures when using wet etching. With this conventional route, we were unable to obtain contacted devices as stress was introduced during metal deposition, leading to the nanowires collapsing. We therefore chose to define the bottom electrodes prior to the HSQ spin coating process.[5] In order to avoid poor step coverage, the use of undiluted HSQ was required,[10] which limited our minimum line width to 18 nm.

Figure 2 shows a SEM image of fabricated HSQ grating patterns. The sample was developed in 25% TMAH developer for 2 min at a temperature of 50 °C. In Figure 2(a), we

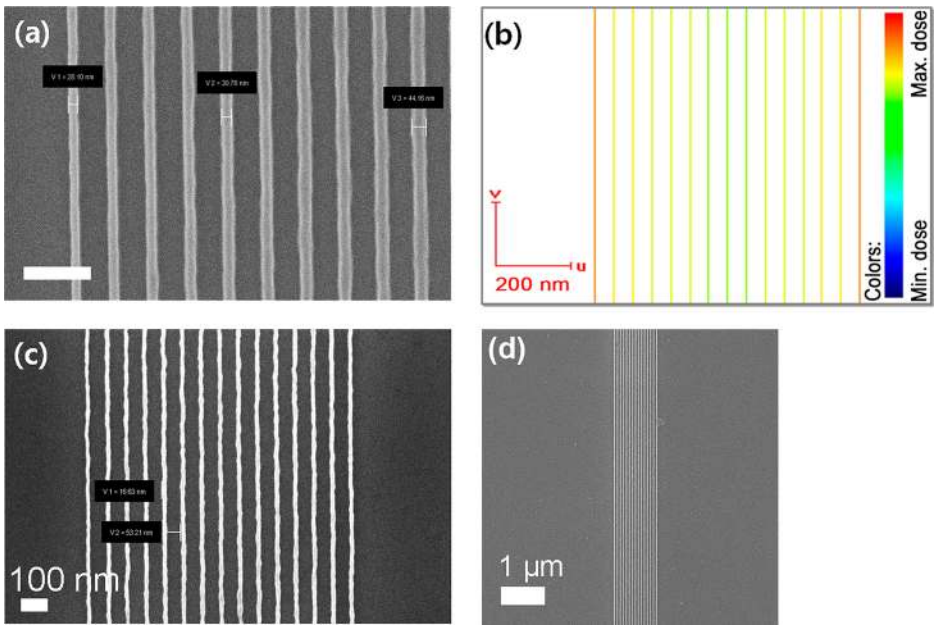

FIG. 2. SEM images of the HSQ grating patterns obtained with a 25% TMAH developer at a temperature of 50 °C. (a) Line array patterns widened in the center due to the proximity effect. The center line size is ~44 nm, and the edge line size is ~28 nm. (b) The pattern which applied a different dose for each line after PEC based on the Monte-Carlo simulation. (c) A line array pattern after PEC was used for dose compensation. The widths of the silicon nanowires are almost identical. (d) The SEM image of SiNWs along a longitudinal direction in low magnification.

show a line pattern with all of the lines exposed to the same electron dose. The central line was broadened by approximately 60% compared to the lines at the edge as shown in Figure 2(a). This is a well-known phenomenon known as the proximity effect. When electrons penetrate through a resist layer, they are scattered by resist molecules or the substrate atoms via forward-scattering or back-scattering events. The majority of scattered electrons originate from forward-scattering via small angles, while the back-scattered electrons have a large angle projection. In addition, through back scattering events in the substrate, electrons return back to the resist at a significant distance from the incident beam, thereby causing additional undesirable resist exposure. This backscattering is what causes the proximity effect. Due to their large angle projection the backscattered electrons have less influence on isolated patterns, but considerably more influence on densely patterned areas, making it difficult to achieve high density packing. It was difficult to create a pattern with less than 100 nm pitch. For this reason, proximity effect correction (PEC) was used to obtain dense patterns in higher resolution.

PEC adjusts the dosage of the electron beam in accordance with the desired pattern feature. The dosage for each line depending on their position was adjusted using PEC based on Monte Carlo simulations. Figure 2(b) shows a pattern with different doses after PEC. In Figure 2(c), the results for a pattern with 70 nm pitch are shown; it is obvious that all of the lines have the same width. 50 nm pitch could be achieved using this method. Figure 2(d) shows a SEM image of 70 nm pitch size after PEC, in low magnification. The patterns are successfully defined along a longitudinal direction.

A post-development bake, so-called postbake or hardbake, is performed after development in order to increase the thermal, chemical and physical stability of the developed resist structures, enabling subsequent processing such as electroplating, and wet and dry chemical etching. SEM images in Figure 3 clearly show the differences of the 18 nm linewidth grating patterns, with 50 nm pitch, before and after the hardbake. Without the hardbake, significant footings are seen between the lines. However, after the hardbake, the number of footings between the lines is reduced by a factor of 3. Furthermore, the linewidth is reduced from 18 nm to 14 nm, which can be attributed to the enhanced cross-linking of HSQ.

A crucial point for reaching high density patterns is the contrast value of the developer used. In order to improve the resolution of the patterns, we used a so called "salty developer" (Refs. 6 and 11) on thick resist layers for the first time, which proved to be more efficient than hot development,[12–14] two-step development[15] or the use of a potassium hydroxide containing developers.[16] The salty developer enhanced the contrast value by 3 times compared to a 25% TMAH developer without any significant loss of the resist sensitivity.[17]

SEM images in Figure 4 show arrays composed of 15-SiNW channels with a narrow width of 18 nm. The pitches are varied between 100 nm, 70 nm, and 50 nm (Figures 4(a)–4(c)) after development in a salty developer with PEC and a hardbake. Figure 4(d) shows a cross-sectional view of the channels with 70 nm pitch. The cross-section profile exhibited a round top after etching because HSQ remained on top of the Si. However, it is evident that the SiNWs have a square shape, demonstrating anisotropic etching and confirming the excellent uniformity of our structuring process. After formation of SiNWs, we measured line width roughness. Figure 4(e) shows line scan profiles of the SiNW patterns. It clearly shows the SiNWs have nearly uniform width and wire spacing between the wires. As shown in Figure 4(f), the plot shows the width mean of each line of SiNWs. The error bars represent the standard deviation of measurements, reflecting a distribution of the line width with $0.71 \sim 1.9$ nm roughness range.

B. Electrical characteristics of a single-channel SiNW

As our contacting procedure ensured electrically functional devices in all cases, without any additional doping step or thermal annealing for the S/D regions, often the cause of non-uniform channel doping, this is to our knowledge the smallest pitch of electrically viable multi-channel SiNW structures reported. This allowed for the effects of packing these structures to high density to be investigated.

We first investigated the electrical properties of a single SiNW FET with 18 nm channel width as shown in Figure 5(a). The transport characteristics shown in Figure 5(b) are typical for a nano-channel FET with a Schottky barrier (*SB*) between lightly p-doped silicon and a Ti electrode. The on-off ratio of the transfer characteristics (I_{on}/I_{off}) reached over 10^4 ($V_{ds} = 100$ mV), which is sufficient for application in practical devices.

Ideally, Φ_{Bn} (electron Schottky barrier height) can be expressed as Φ_M-χ, where Φ_M is the metal work function and χ is the electron affinity of silicon ($\chi \approx 4.05$ eV). By using the work function values of Ti as 4.33 eV, Φ_{Bn} can be estimated to be 0.28 eV. The *SB* with SiNW FETs significantly improves the off state leakage, and it can act excellent in enhancement-mode.[18] The inset of Figure 5(b) shows the conduction band in the channel for different gate voltages. The transfer curve exhibits two slopes below the threshold. This can be understood by assuming that the dominant

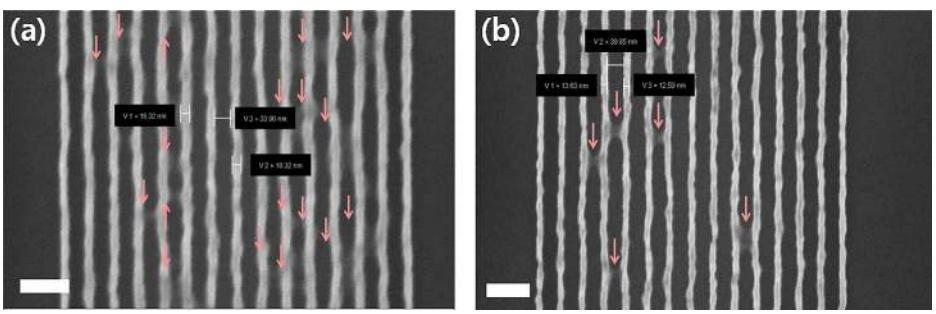

FIG. 3. SEM images of 50 nm pitch structures showing the effects of the hardbake (a) before and (b) after. After the hardbake, the number of footings (indicated by arrows) between the lines was reduced from 18 to 6 with a reduction of the line width from 18 nm to 14 nm. The hardbake was performed on a hot plate at 115 °C for 2 min. Scale bars 100 nm.

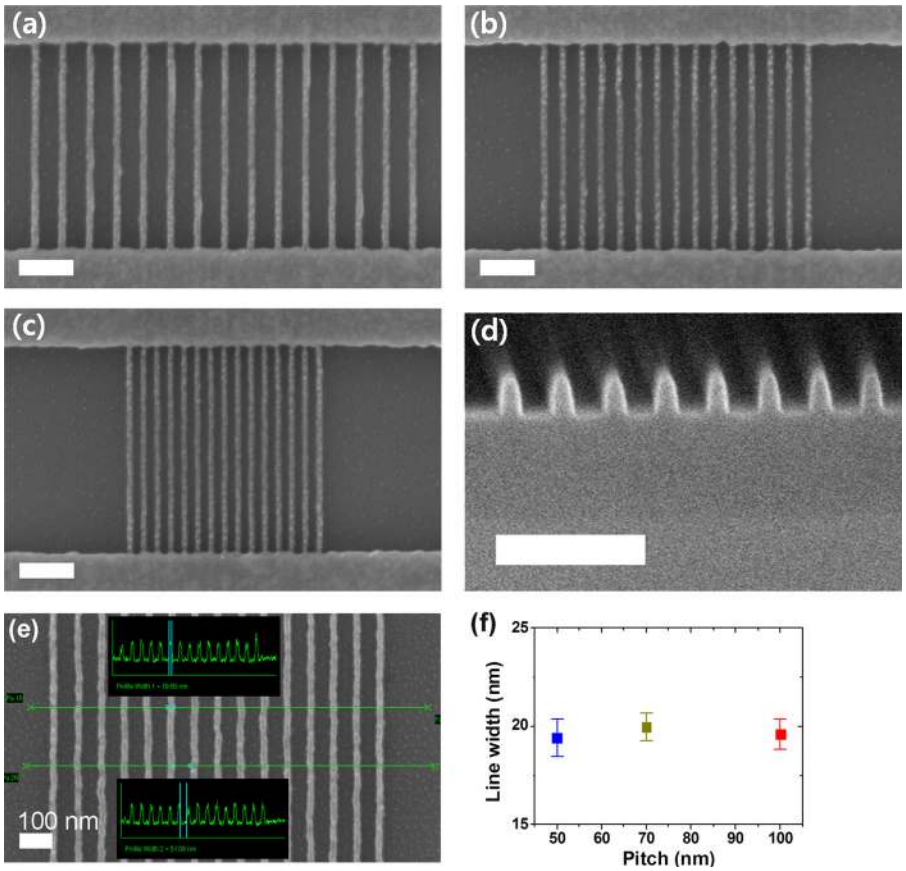

FIG. 4. SEM images showing multi-channel SiNW FETs with different pitches. (a) 100 nm, (b) 70 nm, and (c) 50 nm pitch. Scale bars 200 nm. All SiNW channels have an average width of 18 nm and length of 750 nm. (d) Cross-sectional SEM image of HSQ grating line patterns of (b). (e) Line scan profile of the 70 nm pitch size of SiNW FETs. (f) Plot of line width roughness of each line as a function of pitches. The error bar stands for standard deviation of measurements.

mechanism of carrier injection is different in each region. It has previously been shown that carrier injection in *SB* FETs can occur either by thermal emission over the potential barrier or by thermally assisted tunneling through the Schottky barrier.[19,20] The gray part, fitted with the blue line, is the region associated with thermal emission over the potential barrier. In this region, carriers are injected from the source over the potential barrier, leading to a steep slope.

The maximum potential barrier is higher than the Schottky barrier height in the source, and thus the device behaves like a conventional metal oxide semiconductor field-effect transistor (MOSFET). The part displayed in black, fitted with the red line, represents the region of both thermal emission and tunneling across the barrier. When the conduction band is pushed below the Schottky barrier height in the source, the current consists of the thermal emission and tunneling component, leading to a shallower slope. Upon increasing the gate voltage, the thermal emission component is only slightly changed due to image force induced barrier lowering. Thus, the principal reason for the increase in current is tunneling through the Schottky barrier at the source. In summary, the sub threshold slope exhibits two different slopes which are 3.36 V/dec in the thermal emission dominated region and 7.19 V/dec in the tunneling dominated region.

C. Comparison of the electrical characteristics of SiNW array devices as a function of the pitch

We also investigated the effect of pitch on the electrical properties through comparison of multi-channel SiNW FETs with three different pitches (50 nm, 70 nm, and 100 nm). Figure 6(a) shows the transfer characteristics of these devices on a logarithmic scale (solid lines). The devices were operated at a high gate voltage because the gate oxide had a thickness approximately 100 times thicker than conventional FETs. As can be seen in transfer characteristic plots in Figures 5(b) and 6(a), an intriguing peak is observed near zero gate voltage. It can be tentatively assigned to doping with Na^+ possibly from the salty developer, which is Na based chemicals. Dry etching can induce traps at the SiNW surface, and possible Na^+ ion diffusion in the BOX which is used in gate oxide in our study. This Na^+ ion drift very rapidly through the oxide. Therefore, the peak is attributed to Na^+ ions with varying mobility.[21] Principally, this effect can be significantly reduced using a sacrificial Si_3N_4 layer.[22]

The values for the subthreshold swing are extracted by fitting the peak values of $\Delta Log\ (I_{ds})/\Delta V_{gs}$ (dashed line in Figure 6(a)). Figure 6(b) shows the transconductance of the nanowires as a function of gate voltage with varying pitch. A constant drain-source bias voltage (V_{ds}) of 100 mV was induced on the SiNW arrays. The transconductance (g_m) is nearly zero below the threshold voltage (V_{th}) because of the small drain current. It goes through a maximum at the point of inflection, and then decreases because of degradation of the effective channel mobility and source/drain series resistance. The effective channel mobility usually consists of three dominant scattering mechanisms, Coulomb, phonon, and surface-roughness scattering. Of these, surface-roughness scattering is dominant at high electric fields without dependence on temperature. For this reason, the effective mobility

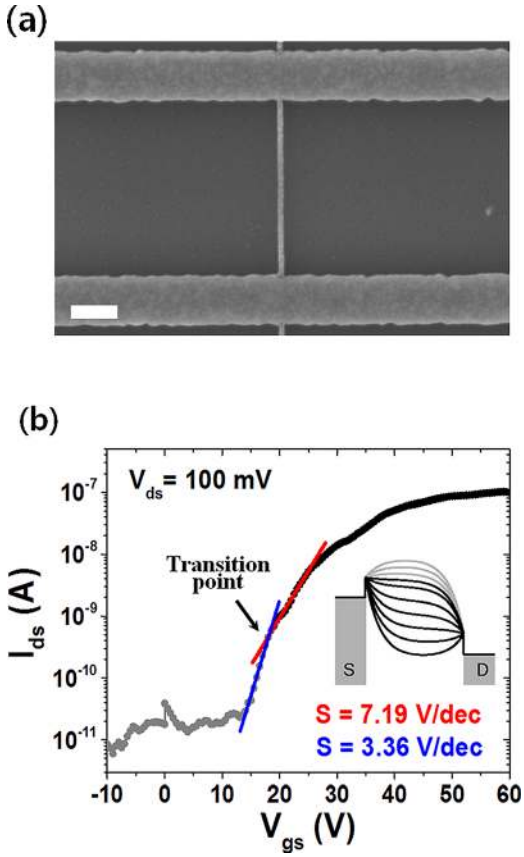

FIG. 5. Single-channel SiNW FET characteristics. (a) SEM image with 18 nm width and 750 nm length. (Scale bar 200 nm.) (b) Transfer characteristics of the device at $V_{ds} = 100$ mV on a logarithmic scale. Below the transition point (blue line), the carrier injection is dominated by thermal emission, while above the transition point (red line) it is dominated by both thermal emission and tunneling. The inset shows the conduction band in the channel for different gate voltages of the SB FETs.

reduction with effective electric field has been attributed to enhanced surface roughness scattering with increased gate voltage.[21,23] However, in the case of the device with 50 nm pitch, the field applied was not sufficient for this to occur, despite the application of a high gate voltage, due to screening of the electric field.

In general, partially depleted transistors suffer from gate induced floating body effects. These effects are known to induce a second peak in the transconductance (g_m) versus gate voltage (V_{gs}) curve in the linear regime; however, this disappears when the devices become fully depleted.[24] In our experiments, the second peak is not observed; thus, the characteristics of our device imply that the devices were fully depleted. The g_m from the channel of the nanowire arrays is bigger than that of a single nanowire device due to the larger effective wire width (W_{eff}). The maximum value of g_m decreases from 11.2 to 3.4 nS when the pitch is reduced from 100 to 50 nm, denoting a small effective width for small pitch.

Simulations of the electric potential profile of SiNW FET array were carried out by solving Poisson's equation with FlexPDE version 6. The carrier density of the channel cross-section is represented on a logarithmic scale for 3 parallel wires of 500 nm length with 50 nm (left) and 100 nm (right) pitch, as shown in Figure 7(a). A similar carrier density at the top of each wire with 100 nm pitch is depicted. However, in the case of the wire with 50 nm pitch, the central wire has a lower carrier density at the top of the wire, which is apart from the surface, compared to the other outer wires. This can be linked to the narrow pitch, which induces fringing fields among the Si NWs and begins to screen the electric field from the bottom gate. The suppression of electric field is pronounced in the central nanowires; thus, narrow nanowires display an inhomogeneous carrier density. Figure 7(b) shows the simulated contour plot of electric potential profile in the on state of the SiNW FET arrays with 50 nm (upper) and 100 nm pitch (lower), the narrow pitch screens the electric field from the back gate at the center of the SiNW arrays. This screening effect reduces the effective electrostatic field which is applied to the device arrays. As a result, the electric potential between wires is reduced as the pitch is decreased. The electric potential distributions with 50 nm and 100 nm pitch illustrate very clearly this phenomenon in Figure 7(c). At 50 nm pitch (black line), the electric potential among wires has a value 27% lower than for 100 nm pitch (red line), which is rather unaffected by the fringing field. Thus, screening of the electric potential, which disturbs carrier inversion and reduces total carrier density, is only influential with small pitch.

Figure 8(a) shows the transconductance (g_m) of the nanowires as a function of pitch at $V_{ds} = 100$ mV. In the linear regime of the transfer characteristic, g_m is written as

$$g_m = \frac{\partial I_{ds}}{\partial V_{ds}}\bigg|_{(V_{ds}=const)} = \frac{\mu C_{ox} W_{eff} V_{ds}}{L}, \qquad (1)$$

where μ, C_{ox}, W_{eff}, and L represent field-effect mobility, gate oxide capacitance per unit area, total effective silicon width of the transistor, and gate length, respectively. The total effective silicon width, for multi-channel FETs, is expressed as the sum of each channel

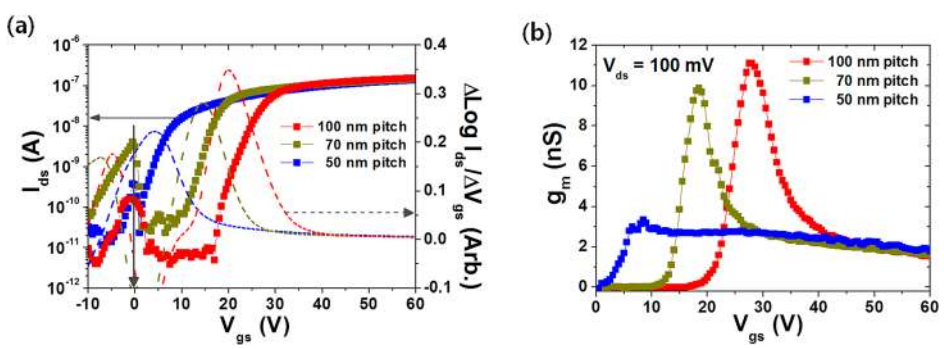

FIG. 6. (a) Transfer characteristics (solid lines). The shift in V_{th} upon decreasing the pitch is clearly visible. The peaks at $V_{gs} = 0$ V indicate that there are no effects from unintentional doping. Subthreshold swing (S) values in Figure 7 are extracted from the peak values of $\Delta Log\ (I_{ds})/\Delta V_{gs}$. (b) Transconductance ($g_m$) versus gate voltage ($V_{gs}$) for the SiNW arrays with different pitch at a constant drain-source bias voltage $V_{ds} = 100$ mV.

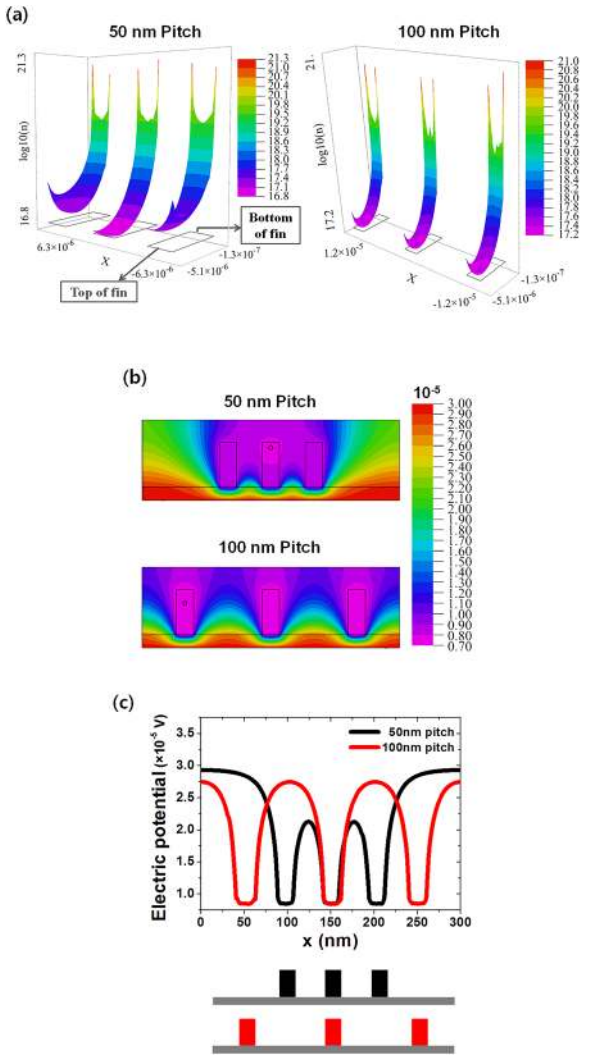

FIG. 7. Simulation of the SiNW FET arrays. (a) The carrier density profile in the on state with 50 nm (left) and 100 nm (right) pitch. (b) Contour plot of electric potential profile for a perpendicular cross section of a SiNW FET with 50 nm and 100 nm pitch. (c) The overlap of electric potential plot for directly comparison of SiNW arrays with 50 nm and 100 nm pitch.

$$W_{eff} = (n-1)(pitch) + W_{wire}. \tag{2}$$

Here, n and W_{wire} are, respectively, the number of nanowires in parallel between source and drain and the nanowire width. From the above two equations, g_m is proportional to W_{eff} which, in turn, is proportional to pitch. Experimentally, we show that g_m is reduced from 11.2 to 3.4 nS when the pitch is reduced from 100 to 50 nm, which can be attributed to the small effective width given by the small pitch. The g_m is linearly proportional to W_{eff} (Eq. (1)) and the relation between W_{eff} and S_{pitch} is well described with Eq. (2). In other words, W_{eff} is proportional to S_{pitch} which is affected by the screening electric field. As the screening electric field increases as S_{pitch} decreases, they have inversely proportional relation.

Furthermore, Figure 8(a) shows the drain induced barrier lowering (DIBL) effect, which is a phenomenon typically observed in short channel devices. It can be measured by the change of the threshold voltage of the transfer curves in the subthreshold region divided by the drain voltage difference of the two curves. In the absence of any DIBL, the two curves would coincide in the subthreshold region. In conventional MOSFETs, the DIBL effect can cause a reduction of the built-in potential between S/D electrodes when the drain-source voltage is increased. However, in *SB* FETs, the drain voltage increases when the width of the Schottky barrier is reduced, leading to an increase of the tunneling current.[25,26] The DIBL is proportional to $e^{-L/\lambda}$,[27,28] where the characteristic length λ can be expressed as

$$\lambda = \sqrt{\frac{\varepsilon_{si} W_{eff} t_{ox}}{n \varepsilon_{ox}}}, \tag{3}$$

where ε_{si} is the electrical permittivity of the silicon, ε_{ox} is the electrical permittivity of the gate oxide and t_{ox} is the gate oxide thickness. This relation indicates that the DIBL can be reduced by decreasing W_{eff}. Consistent with theoretical predictions, our results have shown (in Figure 8(a)) that the DIBL decreases with decreasing pitch, which is important for future scaling laws with nano-channel FETs.

Figure 8(b) shows V_{th} and the subthreshold swing (S) of multi-channel FETs as a function of pitch at $V_{ds} = 100$ mV. The shift in V_{th} can be explained by considering additional capacitance contributions at the edges between channels. As a device with trench isolation, the field lines from the gate electrode are focused by the channel edge. Thus, at the edge of the channel, an inversion is formed at lower voltages than at the center. Therefore, V_{th} becomes lower in devices with smaller width, and as a result, V_{th} decreases with decreasing pitch. When the drain current is plotted on a logarithmic scale, it becomes obvious that it varies with gate voltage below V_{th}. This subthreshold conduction behavior can be described by S, which measures the dependence of the drain current on the gate voltage. S is an important device characteristic expressing the change in the input V_{gs} required to

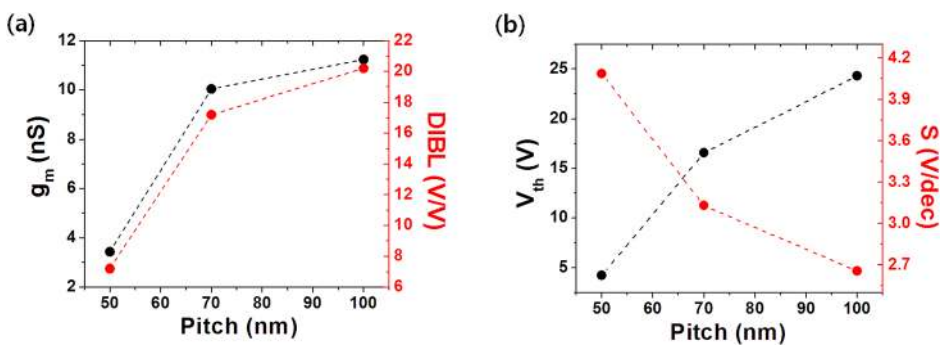

FIG. 8. Comparison of extracted parameters of multi-channel SiNW FETs with different pitches. (a) Transconductance (g_m) and DIBL effect (b) Threshold voltage (V_{th}) and Subthreshold swing (S) of the nanowires as a function of pitch at $V_{ds} = 100$ mV.

reduce the subthreshold current by one decade; it is therefore a measure of the switching behavior.

S is given by

$$S = \frac{dV_{gs}}{d(\log(I_{ds}))} = \frac{kT}{q}\log(10)\left[1 + \frac{C_{ss} + C_{dep}}{C_{ox}}\right], \quad (4)$$

where C_{ss} is the surface state capacitance, C_{dep} is the depletion capacitance and C_{ox} is the gate oxide capacitance. The results show that S is increased from 2.7 to 4.2 V/dec by decreasing pitch as shown in Figure 8(b), which can be explained by the following.

The current decreases to zero when the gate voltage is below V_{th}.[29] For fully depleted devices, the C_{dep} is suppressed because the depletion charge is limited by the thickness of the Si film and therefore does not vary with the gate voltage.[30] Therefore, the surface state capacitance C_{ss} dominates the subthreshold swing of fully depleted devices. The C_{ss} is primarily composed of surface state capacitive components, the fringing capacitance (C_{fr}), which is induced by the coupling between each side of the silicon wires and the gate, the so-called fringing field. In the case of an array structure, the fringing capacitance density ($C_{fr}/area$) increases with decreasing pitch.[31] Thus, C_{ss} increases with decreasing pitch. As a result, S increases when the pitch decreases as it is proportional to C_{ss}.

IV. SUMMARY AND CONCLUSIONS

We have demonstrated the smallest pitch reported to date of densely patterned HSQ gratings by direct EBL writing and transferred the pattern to silicon nanochannels on a SOI substrate by an ICP-RIE process. Due to the absence of additional processing for the S/D region, the Schottky barrier was formed at the contact region and lead to high on-off ratios due to a suppressed off current.

Our results represent the first experimental investigation of the effect of varying pitch on the electrical behavior of high density SiNW FETs. From this, we elucidated the effect of different pitch on the electrical behavior. As a result, the drain current was reduced with decreasing pitch due to a reduction of the effective electrostatic field. Further, we have shown that by decreasing the pitch of multi-channel SiNWs, both the DIBL and g_m are decreased because they are proportional to W_{eff} which decreases when the pitch is decreased. Therefore, V_{th} and S can be related to the fringing capacitance between channels. This gives rise to a reduction of V_{th} and an increase of S. We believe this study yields valuable information and will act as an important guide for future high integration density level with SiFETs whilst also providing experimental evidence for theoretical predictions.

ACKNOWLEDGMENTS

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