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Electrical Properties of Phase Change and Channel Current Control in Ultrathin Phase-Change Channel Transistor Memory by Annealing

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We studied phase-change channel transistor memory devices with an ultrathin $Ge_2Sb_2Te_5$ chalcogenide film channel and tried to demonstrate two combined functions (memory: resistance change and selection: channel current control) by annealing in this paper. Drain–source resistance can be markedly decreased by 2–3 orders of magnitude after annealing due to the phase change from the amorphous to crystalline phases. A channel current control effect in which the drain current decreases with the gate voltage was clearly observed in 10- and 20-nm-thick $Ge_2Sb_2Te_5$ devices. The absolute channel current modulation by the gate voltage in the crystalline state is much stronger than that in the amorphous state. Furthermore, the channel current control ability in devices with thin $Ge_2Sb_2Te_5$ is stronger than that in devices with thick $Ge_2Sb_2Te_5$. The channel current control effect might result from the potential change of the ultrathin $Ge_2Sb_2Te_5$ channel by the gate voltage.
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KEYWORDS: transistor memory, phase change, chalcogenide, channel current control, annealing

1. Introduction

Electronic phase-change random-access memory (PRAM) has attracted much interest due to its promising merits.[1,2] The application of this device is based on the ability of chalcogenides to be reversibly transformed between the highly resistive amorphous and lowly resistive crystalline phases by Joule heating.

The memory cell of PRAM consists of a transistor and a reversible chalcogenide resistor as shown in Fig. 1(a). Furthermore, by simply putting the reversible resistor into the transistor, we proposed a novel phase-change channel transistor memory (PCTM) for ultrahigh-density memory.[3,4] Its cross-sectional diagram is shown in Fig. 1(b). Figures 1(c) and 1(d) are schematic circuit diagrams of PRAM and PCTM cells, respectively.

The gate and drain electrodes of a PCTM cell can work as the word line and bit line, respectively. Thus, two functions can be combined in a transistor:

1) Nonvolatile memory based on phase-change effect as shown in Fig. 2(a)

By applying a high and short electrical pulse between the drain and source electrodes of the PCTM cell to heat the phase-change chalcogenide channel of PCTM to a temperature higher than the melting point (T_m) and cool it very quickly, it enters a highly resistive amorphous state.

On the other hand, the channel of PCTM would be crystallized, and thus, a lowly resistive crystalline state could be obtained if we apply a low and long electrical pulse to heat the channel to a temperature between the melting point and the crystallization temperature (T_c).

2) Selection of memory cell (channel current control) based on nanocrystal effect, field effect or even other effects as shown in Fig. 2(b)

According to the report by Yano *et al.*, the gate voltage had a clear effect on the channel current in their fabricated nanocrystal Si transistor.[5] Here, we consider our structure to be similar to their structure, and thus, the gate voltage might also have a significant impact on the channel current when the channel consists of chalcogenide nanocrystals. In contrast, when the channel of PCTM is in an amorphous state, the gate voltage should have a weak impact on the channel current because the electrical conductivity of the amorphous phase is much lower than that of the crystalline state.

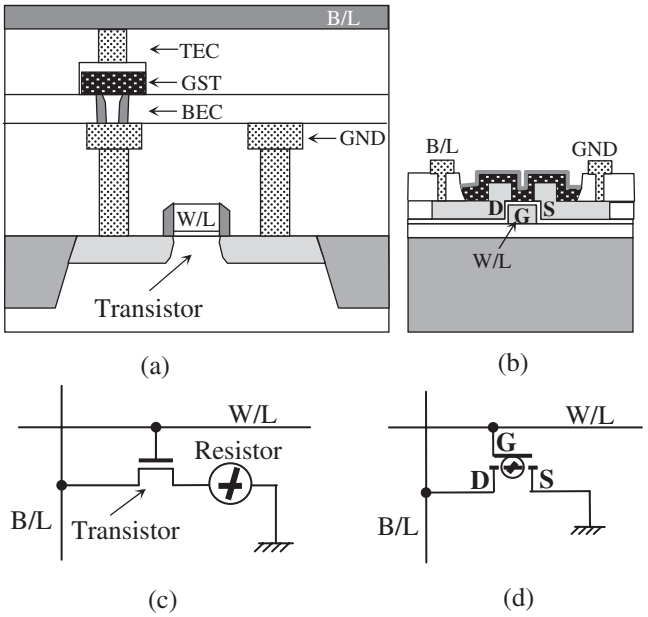

Fig. 1. (a) Schematic cross-sectional diagram of 1 transistor/1 resistor (1T/1R) structure of PRAM cell. (b) Schematic cross-sectional diagram of 1T structure of PCTM cell. (c) and (d) Circuit schematic diagrams of PRAM and PCTM shown in (a) and (b), respectively.

Frye and Adler reported the field effect in chalcogenide glasses.[6] However, to our knowledge, the field effect in crystalline chalcogenide has not yet been investigated. After crystallization of the PCTM channel, the field effect might become strong.

On the basis of these reported results, a schematic diagram of the channel current control effect shown in Fig. 2(b) indicates selection (by applying V_{SE} to the gate electrode) and deselection (by applying V_{DSE} to the gate electrode) of a certain memory cell.

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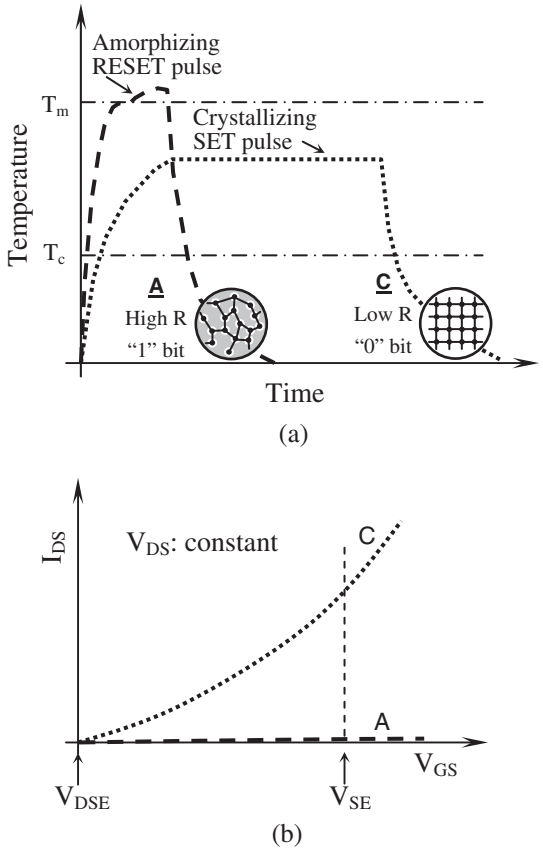

Fig. 2. (a) Schematic diagram of phase change in PCTM indicating amorphizing RESET and crystallizing SET processes. (b) Schematic diagram of channel current control in PCTM, which will possibly be realized by nanocrystal effect, field effect or other effects.

Crystal size could be reduced greatly with the film thickness of chalcogenide films.[4] Furthermore, it is much easier to control the temperature in the channel of PCTM by annealing than by electrical pulse application. $Ge_2Sb_2Te_5$ (GST) is one of most important chalcogenides for PRAM. Hence, it is important to study PCTM devices with an ultrathin GST film and demonstrate the two combined functions mentioned above by annealing, first.

2. Experimental

The schematic cross-sectional diagram of the fabricated PCTM device is shown in Fig. 1(b). Figures 3(a) and 3(b) show the optical images of a device sample and its enlarged channel area. Figure 3(c) shows the three-dimensional atomic force microscopy (AFM) image of a device sample. A layer of 30-nm-thick SiO_2 and 30-nm-thick SiN was used as the gate insulator of the PCTM device. The gate insulator is thick enough to suppress the leakage current at gate voltages up to 30 V. The source, drain and gate electrodes are P-doped Si (n^+ type). Chalcogenide GST films with thicknesses of 10 and 20 nm were deposited using a sputtering system (i Miller, Shibaura Mechatronics). The deposition rate of the GST material was approximately 0.57 nm/s. A 300-nm-thick capping layer of ZnS–SiO_2 was finally deposited to protect the GST channel from oxidation as well as mechanical damage. Current–voltage (*I–V*) characteristics of device samples were measured using a semiconductor parameter analyzer (4155B, Agilent Technologies) in air at room temperature. In the *I–V* measurements, tungsten (W) probes were used to contact the electrode pads of the devices.

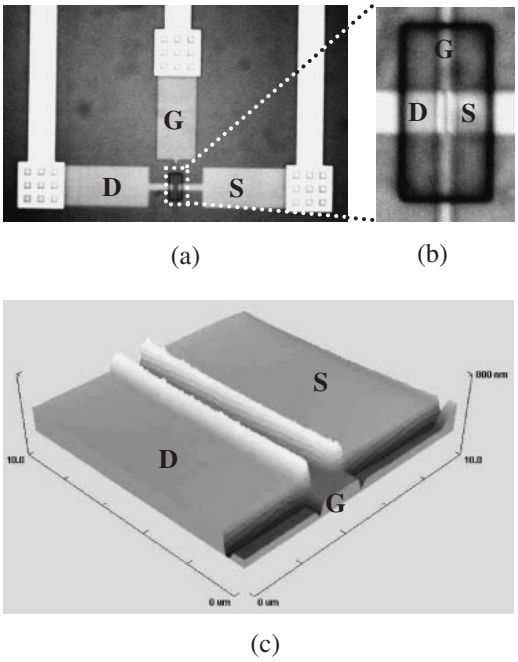

Fig. 3. (a) Optical image of PCTM device sample. (b) Enlarged optical image of channel area. (c) Three-dimensional AFM image of channel area of PCTM device.

3. Results

3.1 Electrical properties of phase change by annealing

PCTM device samples were annealed at increasing temperatures from 127 to 235 °C for 2 min on a hot plate. Figure 4 shows two typical *I–V* characteristics of the device samples before annealing (in an amorphous state) and after annealing (in a poly-crystalline state) in a drain voltage range from −2.5 to 2.5 V. The devices shown in Fig. 4 have a channel length of 1.0 μm and a channel width of 7.0 μm.

The source–drain resistances (R_{DS}) of the device samples have been roughly calculated at a voltage of 2.5 V. A typical resistance vs annealing temperature curve is plotted in Fig. 5. Resistance decreases slightly at 127 and 144 °C, whereas it suddenly drops from 4×10^8 to $2 \times 10^6\ \Omega$ by about two orders of magnitude at approximately 160 °C. The sudden decrease in resistance was caused by phase transformation from amorphous (high resistance) to crystalline (low resistance), which can be used for nonvolatile memory. The crystallization temperature T_x, when annealing for 2 min, is approximately 160 °C.

3.2 Electrical properties of channel current control by annealing

Crystallization is a process of nucleation and crystal growth. By annealing at a temperature slightly lower than T_x with time, a more detailed transition can be obtained. Thus, channel current control is available with GST crystal growth in the channel.

Figure 6 shows drain current (I_{DS}) vs drain voltage (V_{DS}) at gate voltages (V_{GS}) of −10, 0, and 10 V before annealing and annealing at 135 °C for 5 and 15 min. *I–V* characteristics

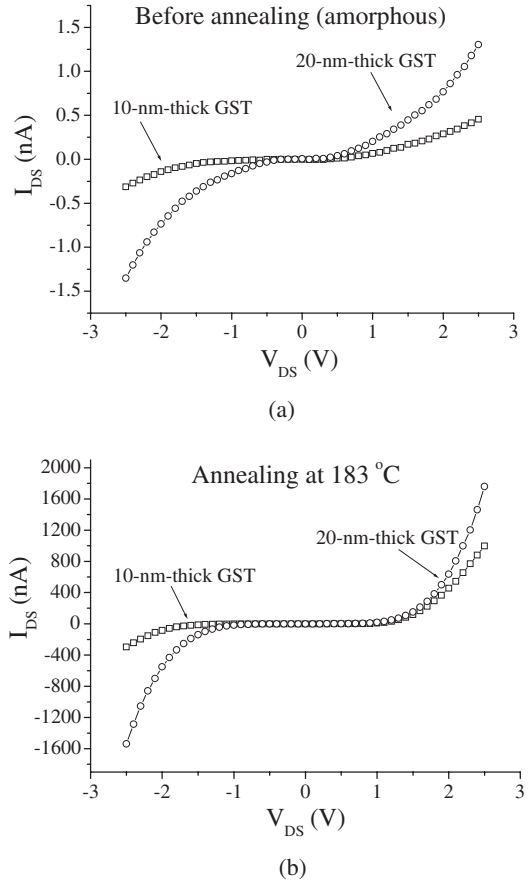

Fig. 4. Typical I_{DS}–V_{DS} characteristics of ultrathin GST PCTM device samples (a) before annealing and (b) after annealing at 183 °C.

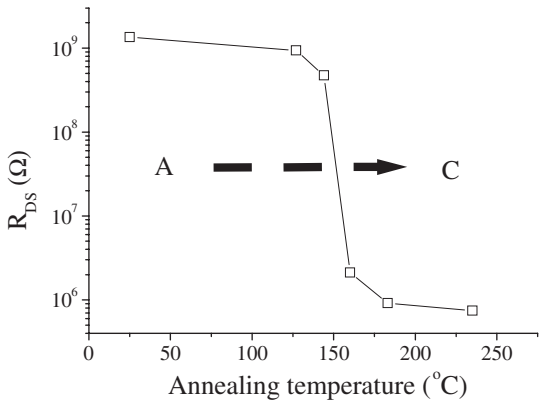

Fig. 5. Typical resistance vs annealing temperature illustrating phase change from amorphous to crystalline phases.

at the three different gate voltages show clear differences. At a certain drain voltage, the drain current drops markedly with an increase in the gate voltage.

To understand the channel current control ability more clearly, transfer characteristics of the PCTM devices were also measured before and after annealing at 135 °C for 5 and 15 min. Figure 7 shows the channel current control effect of a 10-nm-thick GST device at a drain voltage of 3 V when the GST channel was amorphous and partially crystalline. At a given gate voltage, drain current increases with annealing duration, which should be attributed to the crystallization of the GST chalcogenide channel. The channel current control

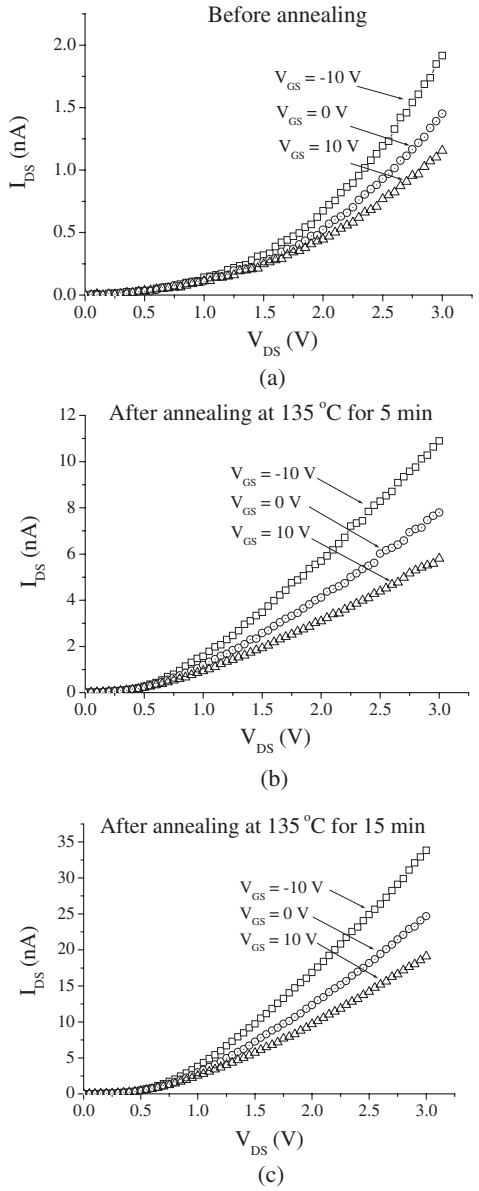

Fig. 6. Drain current vs drain voltage modulated by gate voltage of 10-nm-thick GST device (a) before annealing and (b) and (c) after annealing at 135 °C for 5 and 15 min, respectively.

effect becomes much stronger after annealing at 135 °C for 15 min than before annealing.

On the other hand, we can also anneal the devices at increasing temperatures, but only for a limited time. One typical result of the current control effect of 20-nm-thick GST devices at a drain voltage of 3 V before and after annealing at various temperatures for 2 min is shown in Fig. 8. After annealing at 183 and 235 °C, the channel current can be markedly controlled by gate voltage compared with that before annealing.

4. Discussion

A channel current control effect by gate voltage, although not strong, was clearly observed. The leakage current from the gate electrode should not be the reason for this. The gate insulator is composed of 30-nm-thick SiO_2 and 30-nm-thick SiN and thus is sufficiently thick to suppress the leakage current. The electrical current measured between the source

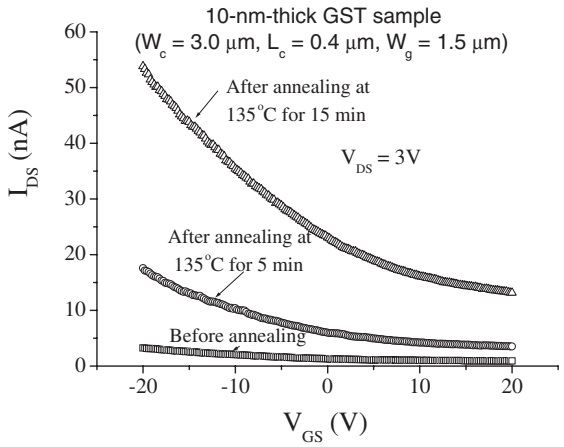

Fig. 7. Current control effect of 10-nm-thick GST device before annealing (amorphous) and after annealing at 5 and 15 min (crystalline).

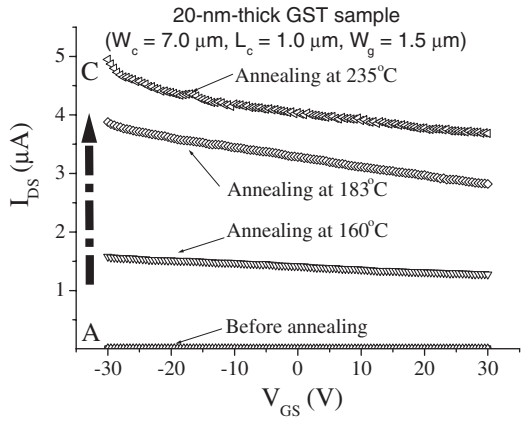

Fig. 8. Current control effect of 20-nm-thick GST device before and after annealing at 160, 183, and 235 °C for 2 min.

or drain and the gate electrodes is in the range of 1 nA when the voltage is even up to 30 V. The range is much lower than the change in drain current by the gate voltage.

The GST material was characterized to be a p-type semiconductor by the hot probe method as shown in Table I. Thus, in our device, GST materials adopt holes as a major carrier, forming an n-channel metal–oxide–semiconductor field-effect transistor (MOSFET) structure if we consider the PCTM device structure here on the basis of the semiconductor conductivity type of GST films. According to semiconductor theory, the former p-type GST channel would be depleted, accumulated, inversed to n-type with an increase in the gate voltage from 0 V, resulting in an increase in drain current with the gate voltage. However, this is not the case here. Measured drain current decreased with the gate voltage as shown in Figs. 7 and 8.

It is difficult to know the exact values of the parasitic resistances and capacitances in the PCTM devices and to estimate the effect of these parasitic components on transistor characteristics at present. The electrical characteristics of the junction between n^+ Si source/drain and p-GST and the effect of parasitic components on the PCTM transistor characteristics are under investigation.

The reason for current control might be due to the potential change by the gate voltage. The movement of the hole carrier through the GST channel might be suppressed with an increase in the gate voltage, owing to the increased potential for the hole carrier.

Table I. Semiconductor conductivity type of GST films after annealing.

Annealing temperature (°C)			
180	258	338	415
Semiconductor conductivity type: P			

Table II. Channel current control of 10-nm-thick GST device shown in Fig. 7.

Annealing conditions	ΔI_{DS} (nA)	$I_{DS\text{-}0}$ (nA)	A_{cc}
Before annealing	2.3	1.3	1.77
135 °C, 5 min	14.1	6.0	2.34
135 °C, 15 min	40.7	23.1	1.76

Table III. Channel current control of 20-nm-thick GST device shown in Fig. 8.

Annealing temperature (°C)	ΔI_{DS} (nA)	$I_{DS\text{-}0}$ (nA)	A_{cc}
Before annealing	1.3	2.4	0.57
160	184.9	1294.1	0.14
183	580.5	2848.2	0.20
235	466.3	3459.8	0.13

Let us define the channel current control ability of the gate voltage A_{cc} as the ratio of $\Delta I_{DS}/I_{DS\text{-}0}$, where ΔI_{DS} is the absolute change in drain current at gate voltages from -20 to 20 V and $I_{DS\text{-}0}$ is the drain current at a gate voltage of 0 V. For the 10- and 20-nm-thick devices before and after annealing, A_{cc} values are summarized in Tables II and III. It is clear that the absolute channel current change by gate voltage in the amorphous state is much lower than that in the crystalline state and that the channel current control ability of 10-nm-thick GST devices is much stronger than that of 20-nm-thick GST devices.

5. Conclusions

On the basis of the measured electrical properties of phase change and channel current control of 10- and 20-nm-thick GST PCTM devices, conclusions can be reached as follows.

(1) Source–drain resistance could change approximately 2–3 orders of magnitude due to annealing based on the phase change effect, which can be used for nonvolatile memory.
(2) After the crystallization of the chalcogenide GST channel, a much larger absolute channel current change by the gate voltage could be obtained, which can be used for cell selection in a memory array.
(3) The possibility of the combination of the above two functions (nonvolatile memory and cell selection) is demonstrated by annealing.
(4) The current control effect in 10-nm-thick GST devices is much stronger than that of 20-nm-thick GST devices.

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