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Electrical property comparison and charge transmission in p-type double gate and single gate junctionless accumulation transistor fabricated by AFM nanolithography

Arash Dehzangi[1*], A Makarimi Abdullah[2], Farhad Larki[1], Sabar D Hutagalung[2], Elias B Saion[1], Mohd N Hamidon[3], Jumiah Hassan[1] and Yadollah Gharayebi[4]

Abstract

The junctionless nanowire transistor is a promising alternative for a new generation of nanotransistors. In this letter the atomic force microscopy nanolithography with two wet etching processes was implemented to fabricate simple structures as double gate and single gate junctionless silicon nanowire transistor on low doped p-type silicon-on-insulator wafer. The etching process was developed and optimized in the present work compared to our previous works. The output, transfer characteristics and drain conductance of both structures were compared. The trend for both devices found to be the same but differences in subthreshold swing, 'on/off' ratio, and threshold voltage were observed. The devices are 'on' state when performing as the pinch off devices. The positive gate voltage shows pinch off effect, while the negative gate voltage was unable to make a significant effect on drain current. The charge transmission in devices is also investigated in simple model according to a junctionless transistor principal.

Keywords: Atomic force microscopy, Junctionless transistors, Local anodic oxidation, Silicon-on-insulator, Double gate, Single gate junctionless silicon nanowire transistor

Background

The aggressive trend of scaling transistors requires a new and more effective device to catch up with this rapid trend for modern transistors. Several innovations in fabrication process such as high κ dielectrics [1], metal gate electrodes [2], stressors [3], and new transistor architectures based on silicon-on-insulator (SOI) such as Fin field-effect transistors (FETs) [4], multigate FETs [5], omega-gate FETs [6], gate-all-around FETs [7], or developed non-epitaxial raised metal Schottky source drain [8] have been introduced. In the recent years, junctionless transistors (JLTs) appeared to be the promising alternative for new generation of transistors [9]. All existing transistors contain semiconductor junctions. Contemporary transistors with ultrasmall size need

ultrasharp doping concentration gradients in junctions. The doping must switch from ultra high concentration n-type to p-type along the very small area in size of some nanometers, which imposes severe limitations on the processing thermal budget and requires the development of costly millisecond annealing techniques. In JLT the doping concentration in the channel source and drain is uniform with high concentration profile for the channel in order to have a reasonable amount of current flow when the device is turned on [10]. The lack of doping concentration gradients provides the smaller size and cancels the need for costly ultrafast annealing techniques. In the last two years, the research in JLTs was focused in design and property [11-13], simulation [14-16], high temperature performance [17], and new fabrication method with higher mobility and better performance [18-20].

The principle of atomic force microscopy (AFM) nanolithography, using local anodic oxidation (LAO) on

* Correspondence: arashd53@hotmail.com
[1]Department of Physics, Faculty of Science, Universiti Putra Malaysia, Serdang, Selangor 43400, Malaysia
Full list of author information is available at the end of the article

SOI, has been described for the first time by Snow and Campbell et al. [21,22], and they astutely expanded AFM nanolithography for fabrication of nanostructures. Ionica et al. [23] have remarkably reported the electrical characteristics of the devices made by AFM nanolithography. In the recent years, some new works have been performed to improve the method of AFM nanolithography [24,25]. However, the lack of sufficient explanation or interpretation for the behavior of these structures is still an interesting issue and worth for further investigation. In fact, fabrication of nanotransistors by AFM nanolithography with similar structure has been developed with prominent result in the last decade, but recent rising of the JLTs theory and fabrication can bring up the AFM nanolithography as the extra alternative. We already reported the fabrication of the p-type single gate (SG) JLT device with a simple structure, low doping concentration, and no gate oxide layer [26-29]. The most important advantage of AFM nanolithography is that it impedes damage of the crystalline structure of silicon due to highly energetic electrons which are normally introduced to the structure by techniques such as electron beam lithography.

In this paper we report the fabrication of a double gate structure with improved method by implementing the advantages of AFM nanolithography in contact mode with a simple structure. We used the SOI technology to ensure a very sharp interface top silicon layer-silicon dioxide and used buried oxide layer as an etch stop layer during fabrication. Low doping concentration p-type SOI was used in order to have less scattering effect and low 'off' current. Also, the electrical property of both double gate (DG) and single gate JLT will be compared; the charge transmission, according to the JLTs' principal with the glance of accumulation mode transistors function, will be investigated.

Methods

Device fabrication

The AFM nanolithography process was performed by using scanning probe microscope machine (SPI3800N/4000, SII Nanotechnology Inc., Chiba-shi, Chiba, Japan) in contact mode. Low doped (10^{15} cm^{-3}) p-type (100) SOI wafer was prepared using Unibond™ (Unibond International Ltd., Uxbridge, Middlesex, UK) processed with a 145-nm buried oxide (BOX) thickness, 90-nm top Si layer thickness, and a resistivity ρ of 13.5 to 22.5 Ω cm used as the substrate [30]. Prior to use, the SOI wafer was cut into small sizes (1×1 cm), cleaned by modified standard Radio Corporation of America cleaning process and then dipped in hydrofluoric acid (HF) (1% water solution) for 30 s in order to replace the Si-O bonds by low energy Si-H bonds. After sample preparation, AFM nanolithography with LAO method was

applied to provide etching of the stop layer on top of SOI substrate. Finally, KOH anisotropic etching and HF oxide removal etching completed the fabrication of device (Figure 1).

Local anodic oxidation

An AFM tip (Cr/Pt conductive coating) was used to draw oxide patterns on top of the SOI substrate. The hydrogen atoms can be locally removed on the surface of the substrate with AFM when a negative tip voltage provides a local oxidation by means of field-enhanced oxidation process. The voltage pulse was applied to form a liquid bridge between the tip and the sample; meanwhile, another voltage was applied to the silicon substrate to induce nano-oxidation, and the absorbed water layer on the surface provided the required electrolyte under this ambient condition. During the oxidation, the force reference was −0.1 N, also the writing speed, scan speed, and applied tip voltage were held at 0.5 μm/s, 1.0 μm/s, and 9 V, respectively (all parameters were optimized). All mentioned parameters with the relative humidity percentage of 65% to 68% provided the thickness of 3 nm for oxide layer, which is an acceptable range, and the patterned structure is well-shaped. The air ambient humidity is essential to achieve the oxidation [31,32]. In Figure 2, the LAO process is schematically shown.

Figure 3a,b,c,d shows the DG and SG structures after the LAO with the best gate symmetry and the smallest reproducible dimensions we had achieved. In the SG structure the nanowire moved towards the side gate to avoid of leakage current appeared in the previous work [27].

Wet etching process

KOH wet etching is a very significant part in the fabrication of SG and DGJLT. In fact, having contamination, ill-etched, or over etching structures were hardly avoidable in wet
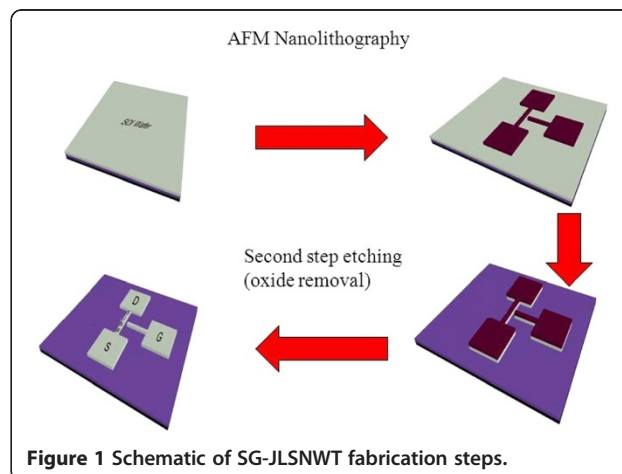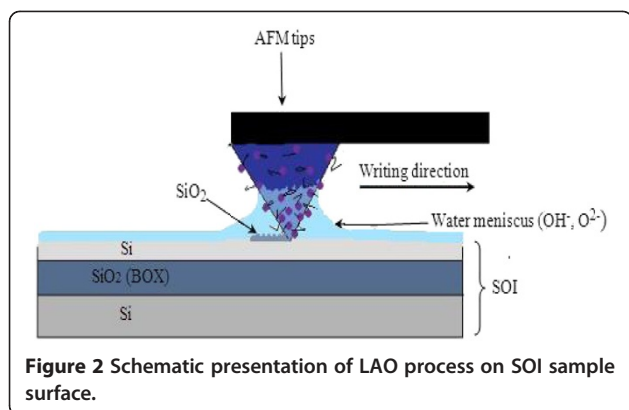

Figure 1 Schematic of SG-JLSNWT fabrication steps.

Figure 2 Schematic presentation of LAO process on SOI sample surface.

etching which, accordingly, the accuracy and precaution are important. To remove the undesired Si area, KOH was used as an etchant. The KOH concentration also affects the quality of the etched surface. Referring to the previous reports in KOH wet etching [33-37], we used a 30 wt.% KOH solution, saturated with isopropyl alcohol (IPA) at 63°C to remove all the non-protected silicon areas. IPA was used in this work as initiator to improve the cleaning process providing smooth surface. IPA reduces the etch rate, hence improving the surface roughness and making the etching process more controllable. The best optimized condition was the solution of 30 wt.% KOH with 10 vol.% IPA for wet etching at 63°C, immersing time for 20 s, and stirring at 600 rpm. The stirring of the solution is to ensure the uniformity of the etching process.

The final structure was obtained by removing the oxide layer using HF acid (Figure 3b,d). In fact, several models have been proposed for the silicon anisotropic etching mechanism in aqueous KOH, which we have chosen as the method by considering of the crystallographic planes for a cubic crystal. In a cubic crystal, the (110) plane is normal to the diagonal of a surface plane, and the (111) plane is normal to a volume diagonal. For the atoms located on the (100) plane, they have two dangling bonds and two bonds remaining in the crystal. Like in our case, when a (100) plane is exposed by the etching solution, OH^- can attach to the dangling bonds and loosen the other bonds, so they can break easily. The KOH etching of (100)-oriented silicon provides V-shaped grooves [33].

In Figure 4, the high magnification transmission electron microscopy (TEM) micrograph of the etch depth for nanowire profile is shown for another sample. The adjacent gate is not shown in the picture. The SOI with 90 nm thickness of the Si layer makes the whole structure, after etching with the thickness of 90 nm. Both SG and DG structures have 100 nm for the channel width, 200 nm for the channel length, and 4 μm for the distance between the source and the drain. The gap between the gate and the channel for both structures were 100 nm (Figure 3). The electrical connections were provided by two pads considered as source and drain with the gate work function of 5.12 eV. The Si thickness of the whole structure including the channel, gate pad(s), source and drain contacts were 90 nm with the same p-type doping concentration (10^{15}).
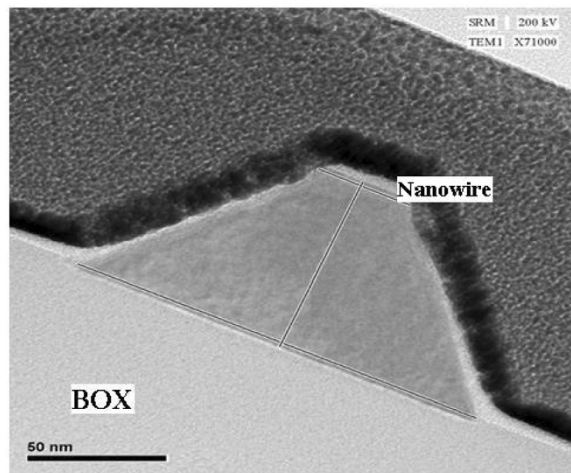

Figure 3 AFM and SEM images of DG (a,b) and SG (c,d) JLTs after LAO and etching process.
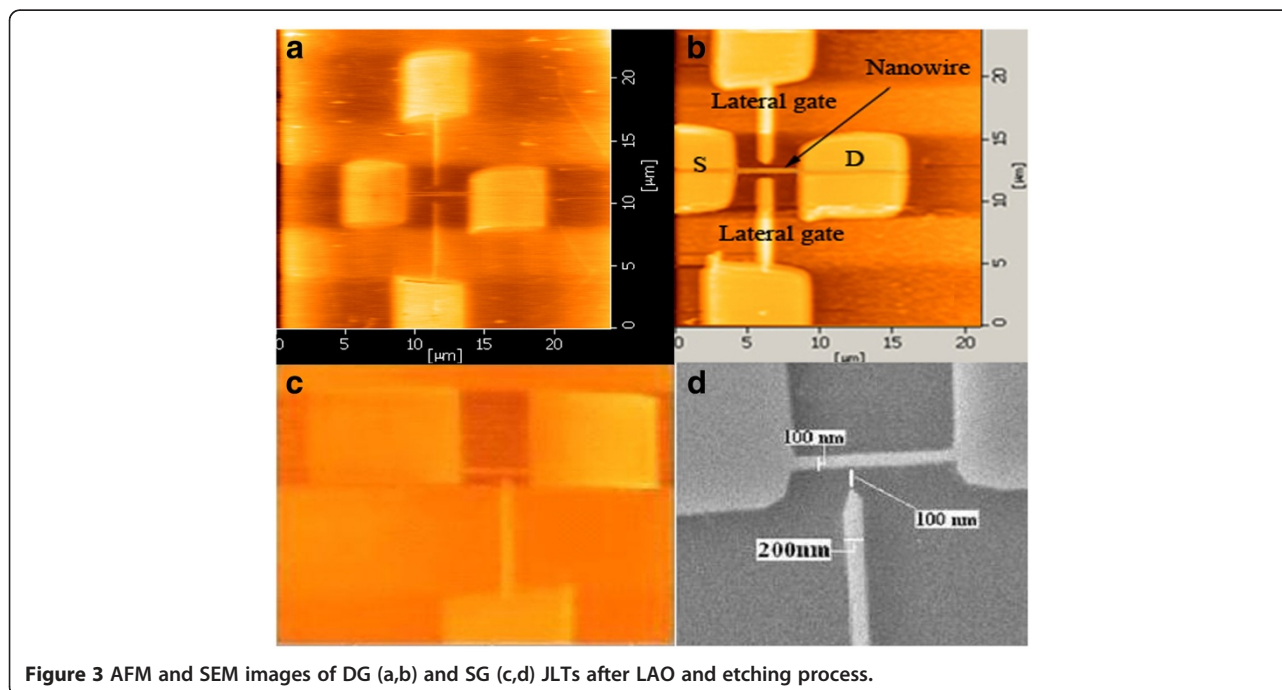
Figure 4 High magnifications TEM micrograph of etch depth profile to show the dimension of the nanowire.

Figure 5 Transfer characterization graph for DG and SG JLT.

Results and discussion

Results

The electrical characterization of the transistor was characterized by semiconductor parameter analyzer (Lakeshore, Desert Cryogenics Agilent HP 4156 C, Agilent Technologies, Santa Clara, CA, USA). Figure 5 shows the transfer characteristic for DG and SGJLT. The pinch off effect can be seen due to positive lateral gate applying on the channel. The subthreshold swing (SS) and on/off ratio for double gate junctionless transistor (DGJLT) were 10^6 and 100 mV/decade, respectively, and for SGJLT were 10^5 and 167 mV/decade respectively. By increasing the positive gate voltage, the current dropped. This indicates that the device required positive gate voltage to be turned off. The pinch off effect for both devices is recognizable which *off* state occurred in +1.5 and +2.5 V in DG and SG structures, respectively. The result for output characteristic shows that the drain current (I_D) does not significantly increase with the negative increase of gate voltage (not shown), unlike the conventional p-type channel metal-oxide-semiconductor field-effect transistor (MOSFETs). Also, high and positive threshold voltage (+1.2 V for SG and +0.8 V for DG) suggests that the device is in an *on* state. It indicates that the transistor was in the *on* state with zero gate voltage.

The I_D-V_{DS} characteristics for SG and DG structures are shown in Figure 6 for positive gate voltage. Low current is due to the low doping concentration profile (10^{15} cm^{-3}) for the channel, which is lower than reported current value of the high doping concentration profile (5×10^{19} cm^{-3}) JLTs. The MOSFETs or JLTs with high doping concentration mostly suffered with the high scattering effect or threshold voltage variation. Low channel doping can improve field-effect mobility for improved transconductance and drive current and decrease the
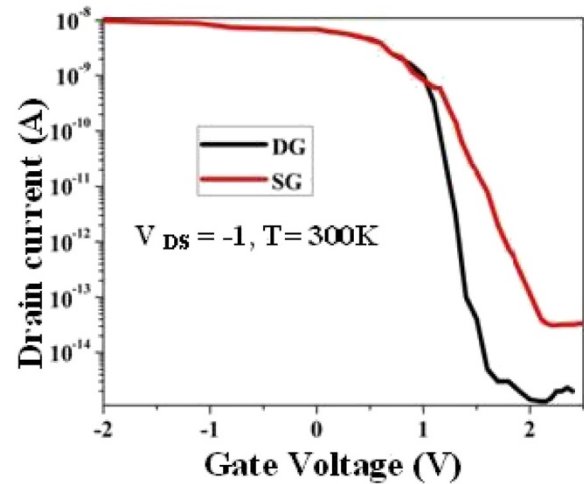
scattering effect and thresholdvoltage variations [38]. It can also provide low current in an *off* state; however, low off current is achievable by increasing the gate work function values. The electrical characteristics of the devices
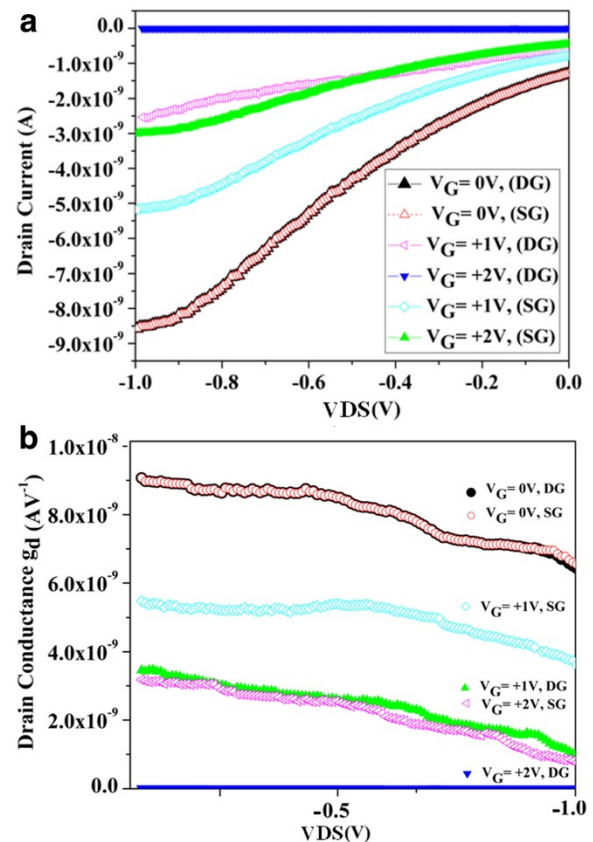

Figure 6 Output characteristic (a) and drain conductance (b) for DG and SGJLT.

have the same trend compared to the reported cases fabricated by AFM nanolithography with nearly similar structure [21,39,40]. In fact, in none of the reported cases, the devices were used as the pinch off device. Normally, high doping SOI was implemented and was never checked to use in a reverse bias to investigate the pinch off effect. Also in our work, we do not have remarkable increase in the current due to the negative gate voltage, while some previous works have shown a higher rate for increasing the current under the gate voltage (mostly positive voltage for the n-type case), and also a higher current value (due to the higher doping concentration).

In Figure 6a, we can recognize the effect of the gate on channel in a DG structure which is more effective than SG due to the asymmetry of SG. In the DG structure the pinch off effect was achieved in $V_G = +2$, while this value cannot provide the same current value in SG. This required higher voltage to approach pinch off effect in SG structure which was in $V_G = +3$ V (Figure 5). Figure 6b shows the drain conductance for SG and DG structures under the different gate voltage. By increasing the gate voltage, the drain conductance for both structures will be decreased. For comparing DG structure to SG device, we have a more effective gate voltage in the channel approaching the pinch off effect (*off* state) with lowest drain conductance, which is consistent to the output characteristics and our expectation about the DG structure. The trend for drain conductance is the same with MOSFETs [41] and JLTs [42], yet the slope is smaller here which can be explained by low doping concentration and current value.

Subthreshold swing

Although the SS value is relatively higher than the best value in single crystal silicon devices [15] and recent JLTs [20,43,44], it is still comparable with the lowest reported value of vertical silicon nanowire array devices [45]. In general, the degradation of SS is due to the increase in the interface state density, decrease of oxide capacitance, and increase in the doping concentration of metal oxide silicon transistor's channel [46]. However, in our work the interface state density probably cannot play an important role since we have only one interface with the channel (channel/BOX interface), and the current value is low. The most important reason for higher SS value in our case could be explained by the lack of oxide layer between the gate and the channel. It lacks the fixed potential drop in cross section of the nanowire (perpendicular to the current flow), which is necessary for inducing sufficient potential to change current linearly with the gate voltage [44]. In SGJLT device, the asymmetry of the gate location provides higher SS value compare to DGJLT device with the symmetric gate locations.

Model description

In recent reports on experimental JLTs [18,47], we did not encounter any case of *on* state condition under the zero gate voltage due to having an opposite doping concentration for the gate and the channel, unless for the simulation cases and for very small gate lengths [48]. The charge transmission in DG and SGJLT operates quite differently from the conventional MOSFETs and also slightly different from the JLT description in recent literature. The devices are working in *on* state for nonzero V_{DS} and $V_G = 0$ V. The reason can arise from the fact that the field effects from the different work function of the gate and channel cannot cause the device to be turned off at $V_G = 0$ V due to the same doping concentration of the channel and gate contact, and no oxide layer for the gate.

Basically, regardless of the gate work function difference between the gate electrode and channel, JLTs are 'gated resistor' which is in the *on* state at $V_G = 0$ V [16]. According to the JLT's principal, when the device is turned on, it approaches the flat band condition. It basically behaves as a resistor, and the electric field perpendicular to the current flow is equal to zero in the 'bulk' channel. In fact, as the advantage of our fabrication method, the AFM lithography keeps the surface and the body of the upper Si layer of the SOI intact and untouched. So we expect to find more bulk property, for example, higher mobility and less surface scattering effect for the channel under the gate.

Immediately after applying V_{SD}, the device goes to an *on* state. The *on* current is controlled by the semiconductor doping concentration and not by the gate capacitance. The operation of devices is outlined in Figure 7, and the three regions I, II, and III are denoted. The structures are a gated resistor turned off by depleting the channel (region II), when essential positive gate voltage is applied. It will be turned off based on the pinch off effect principle, when V_G provides a sufficiently large barrier in the gating region; the highest depletion occurs near to the drain side of the channel due to the stronger electric field in the drain side (Figure 7b,d). Figure 7a,c schematically show the devices in the *on* state. In this condition, the subthreshold current flows by increasing the V_{DS} until the saturation current will be reached at region II, even for $V_G = 0$ V. Since the system is in *on* state from $V_G = 0$, one can say that the threshold voltage is shifted into the positive voltage, and the neutral wire is instantaneously shaped when the bias is applied to the source/drain contacts (Figure 7a, c). That is the reason one can claim that the devices are already in flatband condition like the pinch off transistors [49,50]. In the *on* state condition, the holes concentration in the channel increases, and the neutral or undepleted channel forms between the source and the drain until the peak of the holes concentration in the channel reaches the doping concentration N_A.
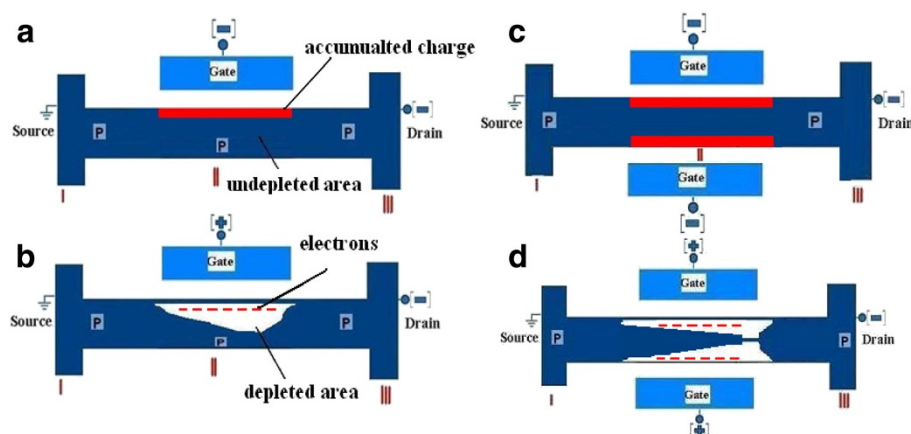
Figure 7 Schematic operations (a,b) of the SG and DG (c,d) for positive and negative gate voltage.

In Figure 8, the schematic profile view of holes location transmission path and comparison of accumulation mode device with SG and DG device are shown. For the DGJLT the neutral wire locates in the center of the channel and close to the bottom, as shown in Figure 8, c and f. It is worth to mention that in SGJLT, the neutral or depleted wire will be formed not exactly in the center. Due to the specific shape of the device and having only one interface with BOX at the bottom, the neutral wire must be formed near to the bottom of the channel and away from the side gate sidewall (Figure 8, b and e). By further increasing the V_{DS} in the *on* state, the depletion will be starting near to the drain due to high electric field in this area in region III, and this is the reason for having saturation for the current [51]. The high electric field in the drain gives rise to the full depletion in nanowire near to the drain area acting as a buffer against the

high electric field in the drain, which accordingly, will lead the current to be saturated.

However, by negatively raising the gate voltage, it is probable to have a little increasing of the current due to some accumulated charges, which were injected from the source (region I) to the channel (red color areas in Figure 7). The drain current mainly flows through a bulk channel. An additional small conduction likely originated from a lightly accumulated channel in sidewalls facing the gates, when the gate voltage is large enough. The influence of the gate on the channel is not very effective to induce an accumulation mode due to the device configuration, low doping concentration, and the lack of oxide layer between the gate and the channel. Accordingly, increasing the gate voltage cannot help to make an effective accumulation layer and we do not expect to have the accumulation mode for high gate voltage. Normally in high doping JLTs in *on* state, after increasing the gate voltage, the device is able to be converted into the accumulation mode with significant increasing of the current (mostly is not desired to reach) [9,47]. Actually, another reason that we interpret the devices as JLT and not in accumulation mode is the ineffective negative increasing gate voltage on the channel.

In the accumulation mode, in *on* state condition, the subthreshold current flows through the bulk of the device near the center of the nanowire just like the JLTs (Figure 7a). But the magnitude of this current is less than ten percent of the whole current achievable. By increasing the gate voltage, the majority of the holes are confined in inversion layers at the sidewalls, with marked peaks at the corners (Figure 7d). In the reported and high doping JLTs, we can increase the gate voltage in order to have accumulation charge and raise the current after reaching the flatband. But still, the largest part of the current is due to bulk conduction. The formation of a surface accumulation channel is also observed at high V_G. In comparison to the trigate FETs, Fin FETs, gate-all-around (GAA) FETs or
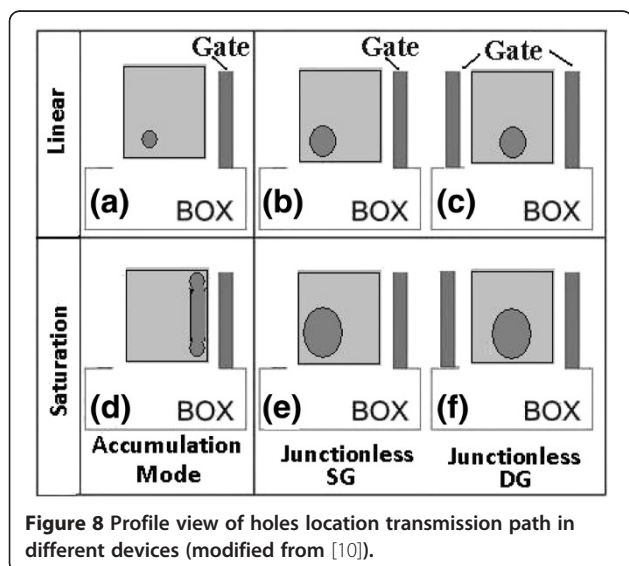

Figure 8 Profile view of holes location transmission path in different devices (modified from [10]).

reported JLTs in which there were more interfaces with the gate oxide layer or BOX and more current values after increasing the negative gate voltage for p-type channels. Here, we only have one interface between the channel and the BOX in order to provide charge accumulation. Accordingly, the increasing negative gate voltage is not able to produce more current compare to the trigate FETs, Fin FETs, GAA FETs, or reported JLTs. For our SG and DGJLTs as gated resistors, when the device is turned on, these essentially behave as a resistor, and the drain current is controlled by regions I and II and doping concentration. For linear region I_D could be given approximately by [47]:

$$I_D \approx q\mu N_A \frac{TW}{L} V_{DS}. \tag{1}$$

Where N_A is the semiconductor doping concentration, μ is the effective mobility, q is the electron charge; T, W, and L are the thickness, width, and the length of the channel respectively. Equation 1 was first time suggested by Colinge [9] for JLTs and also by Fonash et al. [52] who also suggested the similar equation before Colinge's group about the accumulation mode of unipolar Si nanowire transistors. This equation points out that I_D is controlled by the doping concentration N_A, and not by the gate capacitance per area C. We believe that the I_D equation in our case would be very similar to Equation 1. For high doping concentration cases, which were mostly considered in literatures for JLTs, Equation 1 is suggesting for linear region. In our case, considering the *on* state device, low concentration profile for the p-type material, and also the effect of the fins at the side of the channel to the source and the drain contacts, we suggest the same equation, unless, for the V_{DS} we have effective voltage for the channel V_{Ch}, which is obeying the $|V_{Ch}| < |V_{DS}|$. Then, we have

$$I_D \approx q\mu N_A \frac{TW}{L} V_{Ch}. \tag{2}$$

In the *on* state condition, for a given V_{DS}, the electric field from the source to the negatively biased drain must be significantly small (nearly zero) in the neutral wire at the center of the channel. In the linear region we expect that the negative charge in region I (Figure 7), which is adjacent to the area of I/II interface, should be gathered. This charge in the p-type material can only come from depletion in the channel in linear region.

In our case to enter the saturation region from linear region and since the device is trying to reach the saturation condition, we propose that we would have the condition at which the effective channel voltage become fixed at V_{Ch}^{Sat}. Then, further increases in V_{DS}, take place across the channel region and causes the negative charge (electrons) accumulation at the two sides of the channel near the source and the drain interfaces with channel

and also in $|V_{Ch}^{Sat}| < |V_{DS}|$. Considering the Colinge et.al suggestion [47] for saturation region, we have

$$I_{DSat} \approx q\mu N_A \frac{TW}{2L} \left(V_{Ch}^{Sat}\right)^2. \tag{3}$$

This equation can be compared with the general expression of drain current for conventional MOSFETs in the saturation region or even in the accumulation mode [53]. In addition, because of the presence of ohmic contacts for the majority carriers and their location, which is away from the channel edges, we will not have any ambipolar behavior. Unfortunately, the transistors showed leakage through the gate electrode when gate voltages exceeded –3 V. However, the device worked was acceptable for gate voltages smaller than –3 V and gave us some information to confirm our simple model.

Conclusions

The DG and SGJLT were fabricated by AFM-LAO nanolithography on low doped p-type SOI, followed by two improved wet etching process. We do not have a conventional situation for above the threshold voltage and channel saturation, since the devices are gated resistor and *on* state pinch off transistor. Then negative V_G cannot provide the accumulation in channel, but the pinch off occurs alike in a regular junctionless field-effect transistor. The output and transfer characteristic comparison of DG and SG structures were shown and the simple model according to the JLT principal.

Authors' contributions
AD designed and carried out the experimental work, conducted basic characterizations of the sample, analyzed all the data, the model description, and wrote the manuscript. AMA performed the TEM observations and participated in characterization. FL conceived of the study and participated in the experimental work, design, and coordination. SDH participated in the sequence alignment and provided the AFM and SPA instruments. EBS and MNH supervised the research work. JH critically revised the manuscript and YG participated in sequence alignment. All authors read and approved the final manuscript.

Author details
[1]Department of Physics, Faculty of Science, Universiti Putra Malaysia, Serdang, Selangor 43400, Malaysia. [2]School of Materials and Mineral Resources Engineering, Universiti Sains Malaysia, Nibong Tebal, Penang 14300, Malaysia. [3]Functional Devices Laboratory, Institute of Advanced Technology, Universiti Putra Malaysia, Serdang, Selangor 43400, Malaysia. [4]Department of Chemistry, Islamic Azad University, Behbahan Branch University Street, Behbahan 6361713198, Iran.

References

1. Lee C, No SY, Eom DI, Hwang CS, Kim HJ: **The electrical and physical analysis of Pt gate/Al 2 O 3/p-Si (100) with dual high-k gate oxide thickness for deep submicron complementary metal-oxide-semiconductor device with low power and high reliability.** *J Electron Mater* 2005, **34**:1104–1109.
2. Chau R, Datta S, Doczy M, Doyle B, Kavalieros J, Metz M: **High-/metal-gate stack and its MOSFET characteristics.** *Electron Device Letters, IEEE* 2004, **25**:408–410.
3. Song Y, Zhou H, Xu Q, Luo J, Yin H, Yan J, Zhong H: **Mobility enhancement technology for scaling of CMOS devices: overview and status.** *J Electron Mater* 2011, **40**(7):1–29.
4. Lansbergen G, Rahman R, Wellard C, Woo I, Caro J, Collaert N, Biesemans S, Klimeck G, Hollenberg L, Rogge S: **Gate-induced quantum-confinement transition of a single dopant atom in a silicon FinFET.** *Nat Phys* 2008, **4**:656–661.
5. Colinge J: **Multi-gate SOI MOSFETs.** *Microelectron Eng* 2007, **84**:2071–2076.
6. Li Y, Chou HM, Lee JW: **Investigation of electrical characteristics on surrounding-gate and omega-shaped-gate nanowire FinFETs.** *Nanotechnology, IEEE Transactions on* 2005, **4**:510–516.
7. Yang B, Buddharaju K, Teo S, Singh N, Lo G, Kwong D: **Vertical silicon-nanowire formation and gate-all-around MOSFET.** *Electron Device Letters, IEEE* 2008, **29**:791–794.
8. Shima A, Sugii N, Mise N, Hisamoto D, Takeda K, Torii K: **Metal Schottky source/drain technology for ultrathin silicon-on-thin-box metal oxide semiconductor field effect transistors.** *Japanese Journal of Applied Physics* 2011, **50**:04DC06.
9. Colinge JP, Lee CW, Afzalian A, Akhavan ND, Yan R, Ferain I, Razavi P, O'Neill B, Blake A, White M: **Nanowire transistors without junctions.** *Nat Nanotechnol* 2010, **5**:225–229.
10. Nazarov A, Colinge J, Balestra F, Raskin JP, Gamiz F, Lysenko V: *Semiconductor-On-Insulator Materials for Nanoelectronics Applications*. Berlin: Springer Verlag; 2011.
11. Gundapaneni S, Ganguly S, Kottantharayil A: **Bulk planar junctionless transistor (BPJLT): an attractive device alternative for scaling.** *Electron Device Letters, IEEE* 2011, **32**:261–263.
12. Kranti A, Yan R, Lee CW, Ferain I, Yu R, Akhavan ND, Razavi P, Colinge J: *Junctionless nanowire transistor (JNT): properties and design guidelines*, In *Solid-State Device Research Conference (ESSDERC), 2010 Proceedings of the European: September 14–16 2010*. Sevilla: IEEE Xplore Digital Library; 2010:357–360.
13. Zhao DD, Nishimura T, Lee CH, Nagashio K, Kita K, Toriumi A: **Junctionless Ge p-channel metal–oxide–semiconductor field-effect transistors fabricated on ultrathin Ge-on-insulator substrate.** *Applied Physics Express* 2011, **4**:031302.
14. Gnani E, Gnudi A, Reggiani S, Baccarani G: **Theory of the junctionless nanowire FET.** *IEEE Transactions on Electron Devices* 2011, **58**:2903.
15. Lee CW, Afzalian A, Akhavan ND, Yan R, Ferain I, Colinge JP: **Junctionless multigate field-effect transistor.** *Appl Phys Lett* 2009, **94**:053511-053511-053512.
16. Ansari L, Feldman B, Fagas G, Colinge JP, Greer JC: *Atomic scale simulation of a junctionless silicon nanowire transistor*, In *12th International Conference on Ultimate Integration on Silicon (ULIS): March 14–16 2011*. Cork: IEEE Xplore Digital Library; 2011:1–3.
17. Lee CW, Borne A, Ferain I, Afzalian A, Yan R, Dehdashti Akhavan N, Razavi P, Colinge JP: **High-temperature performance of silicon junctionless MOSFETs.** *Electron Devices, IEEE Transactions on* 2010, **57**:620–625.
18. Raskin JP, Colinge JP, Ferain I, Kranti A, Lee CW, Akhavan ND, Yan R, Razavi P, Yu R: **Mobility improvement in nanowire junctionless transistors by uniaxial strain.** *Appl Phys Lett* 2010, **97**:042114.
19. Hsieh E, Chung SS: *A new type of inverter with juctionless (J-Less) transistors*, In *Silicon Nanoelectronics Workshop (SNW): June 13–14 2010*. Honolulu: IEEE Xplore Digital Library; 2010:1–2.
20. Choi SJ, Moon DI, Kim S, Duarte JP, Choi YK: **Sensitivity of threshold voltage to nanowire width variation in junctionless transistors.** *Electron Device Letters, IEEE* 2011, **32**(2):1–3.
21. Campbell P, Snow E, McMarr P: **Fabrication of nanometer scale side gated silicon field effect transistors with an atomic force microscope.** *Appl Phys Lett* 1995, **66**:1388.
22. Snow E, Campbell P, McMarr P: **Fabrication of silicon nanostructures with a scanning tunneling microscope.** *Appl Phys Lett* 1993, **63**:749–751.
23. Ionica I, Montes L, Ferraton S, Zimmermann J, Saminadayar L, Bouchiat V: **Field effect and Coulomb blockade in silicon on insulator nanostructures fabricated by atomic force microscope.** *Solid State Electron* 2005, **49**:1497–1503.
24. Pennelli G: **Top down fabrication of long silicon nanowire devices by means of lateral oxidation.** *Microelectron Eng* 2009, **86**:2139–2143.
25. Martinez J, Martínez RV, Garcia R: **Silicon nanowire transistors with a channel width of 4 nm fabricated by atomic force microscope nanolithography.** *Nano Lett* 2008, **8**:3636–3639.
26. Dehzangi A, Larki F, Saion E, Hutagalung SD, Hamidon M, Hassan J: *Field effect in silicon nanostructure fabricated by atomic force microscopy nano lithography*, In *IEEE Regional Symposium on Micro and Nanoelectronics (RSM): September 28–30 2011*. Kota Kinabalu: IEEE Xplore Digital Library; 2011:104–107.
27. Hutagalung SD, Lew KC: **Electrical characteristics of silicon nanowire transistor fabricated by AFM lithography.** *IEEE Xplore Digital Library* 2010, :358–362.
28. Dehzangi A, Larki F, Saion EB, Hatagalung SD, Abdullah AM, Hamidon MN, Hassan J: **Study the characteristic of P-type junction-less side gate silicon nanowire transistor fabricated by AFM lithography.** *American Journal of Applied Science* 2011, **8**:872–877.
29. Larki F, Hutagalung SD, Dehzangi A, Saion EB, Abedini A, Makarimi AA, Hamidon MN, Hassan J: **Electronic transport properties of junctionless lateral gate silicon nanowire transistor fabricated by atomic force microscope nanolithography.** *Microelectronics and Solid State Electronics* 2012, **1**:15–20.
30. SOITEC PTF: *38190 Bernin, France*, In *Book 38190 Bernin, France* (Editor ed. ^eds.). City http://soitec.com/en/index.php.
31. Sugimura H, Nakagiri N: **Chemical approach to nanofabrication: modifications of silicon surfaces patterned by scanning probe anodization.** *Jpn J Appl Phys Vol* 1995, **34**:3406–3411.
32. Avouris P, Martel R, Hertel T, Sandstrom R: **AFM-tip-induced and current-induced local oxidation of silicon and metals.** *Appl Phys Mater Sci Process* 1998, **66**:659–667.
33. Yun M: **Investigation of KOH anisotropic etching for the fabrication of sharp tips in silicon-on-insulator (SOI) material.** *Journal-Korean Physical Society* 2000, **37**:605–610.
34. Abdullah AM, Hutagalung SD, Lockman Z: *Etching effect on the formation of silicon nanowire transistor patterned by AFM lithography*, In *Proceedings of the International Conference on Nanotechnology: Fundamentals and Applications; August 4–6 2010*. Ontario: Repository@USM; 2010:398. http://eprints.usm.my/19500/
35. Pennelli G, Piotto M, Barillaro G: **Silicon single-electron transistor fabricated by anisotropic etch and oxidation.** *Microelectron Eng* 2006, **83**:1710–1713.
36. Youn S, Kang C: **Effect of nanoscratch conditions on both deformation behavior and wet-etching characteristics of silicon (1 0 0) surface.** *Wear* 2006, **261**:328–337.
37. Philipsen HGG, Kelly JJ: **Influence of chemical additives on the surface reactivity of Si in KOH solution.** *Electrochim Acta* 2009, **54**:3526–3531.
38. Choi YK, Ha D, King TJ, Bokor J: **Investigation of gate-induced drain leakage (GIDL) current in thin body devices: single-gate ultra-thin body, symmetrical double-gate, and asymmetrical double-gate MOSFETs.** *Japanese Journal of Applied Physics PART 1 Regular Papers Short Notes and Review Papers* 2003, **42**:2073–2076.
39. Bouchiat V, Faucher M, Fournier T, Pannetier B, Thirion C, Wernsdorfer W, Clement N, Tonneau D, Dallaporta H, Safarov S: **Resistless patterning of quantum nanostructures by local anodization with an atomic force microscope.** *Microelectron Eng* 2002, **61**:517–522.
40. Ionica I, Montès L, Ferraton S, Zimmermann J, Saminadayar L, Bouchiat V: **Field effect and Coulomb blockade in silicon on insulator nanostructures fabricated by atomic force microscope.** *Solid State Electron* 2005, **49**:1497–1503.
41. Hauser JR: **A new and improved physics-based model for MOS transistors.** *Electron Devices, IEEE Transactions on* 2005, **52**:2640–2647.
42. Duarte JP, Choi SJ, Choi YK: **A full-range drain current model for double-gate junctionless transistors.** *Electron Devices, IEEE Transactions on* 2011, **58**(12):1–7.
43. Chen CY, Lin JT, Chiang MH, Kim K: *High-performance ultra-low power junctionless nanowire FET on SOI substrate in subthreshold logic application*, In *IEEE International SOI Conference (SOI) 2010: October 11–14 2010*. San Diego: IEEE Xplore Digital Library; 2010:1–2.

44. Pai CY, Lin JT, Wang SW, Lin CH, Kuo YS, Eng YC, Lin PH, Fan YH, Tai CH, Chen HH: **Numerical study of performance comparison between junction and junctionless thin-film transistors.** In *IEEE*. 2010:1410–1412.

45. Ramos J, Augendre E, Kottantharayil A, Mercha A, Simoen E, Rosmeulen M, Severi S, Kerner C, Chiarella T, Nackaerts A: **Experimental evidence of short-channel electron mobility degradation caused by interface charges located at the gate-edge of triple-gate FinFETs.** *IEEE Xplore Digital Library* 2006, :72–74.

46. Cho WJ: **Characterizations of Interface-state Density between Top Silicon and Buried Oxide on Nano-SOI Substrate by using Pseudo-MOSFETs.** *Journal of Semiconductor Technology and Science* 2005, **5**:83.

47. Colinge J, Lee C, Dehdashti Akhavan N, Yan R, Ferain I, Razavi P, Kranti A, Yu R: *Junctionless transistors: physics and properties*, In *Semiconductor-On-Insulator Materials for Nanoelectronics Applications*. Heidelberg: Springer; 2011:187–200.

48. Ansari L, Feldman B, Fagas G, Colinge JP, Greer JC: **Simulation of junctionless Si nanowire transistors with 3 nm gate length.** *Appl Phys Lett* 2010, **97**:062105.

49. Sorée B, Magnus W, Vandenberghe W: **Low-field mobility in ultrathin silicon nanowire junctionless transistors.** *Appl Phys Lett* 2011, **99**:233509-233509-233503.

50. Sorée B, Magnus W: *Silicon nanowire pinch-off FET: basic operation and analytical model*, In *10th International Conference on Ultimate Integration of Silicon. ULIS 2009:March 18–20 2009*. Aachen: IEEE Xplore Digital Library; 2009:245–248.

51. Colinge JP, Ferain I, Kranti A, Lee CW, Akhavan ND, Razavi P, Yan R, Yu R: **Junctionless nanowire transistor: complementary metal-oxide-semiconductor without junctions.** *Sci Adv Mater* 2011, **3**:477–482.

52. Fonash SJ, Iqbal MM, Udrea F, Migliorato P: **Numerical modeling study of the unipolar accumulation transistor.** *Appl Phys Lett* 2007, **91**:193508.

53. Iqbal MMH, Hong Y, Garg P, Udrea F, Migliorato P, Fonash SJ: **The nanoscale silicon accumulation-mode MOSFET—a comprehensive numerical study.** *Electron Devices, IEEE Transactions on* 2008, **55**:2946–2959.