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## Electro-thermal modeling of high power IGBT module short-circuits with experimental validation

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# Electro-Thermal Modeling of High Power IGBT Module Short-Circuits with Experimental Validation

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## SUMMARY & CONCLUSIONS

A novel Insulated Gate Bipolar Transistor (IGBT) electro-thermal modeling approach involving PSpice and ANSYS/Icepak with both high accuracy and simulation speed has been presented to study short-circuit of a 1.7 kV/1 kA commercial IGBT module. The approach successfully predicts the current and temperature distribution inside the chip of power IGBT modules. The simulation result is further validated using a 6 kA/1.1 kV non-destructive tester. The experimental validation demonstrates the modeling approach's capability for reliable design of high power IGBT power modules given electrical/thermal behavior under severe conditions.

## 1 INTRODUCTION

Power electronic systems play a particularly important role in motor drives, utility interfaces with renewable energy sources, power transmission, electric or hybrid electric vehicles and many other applications. In 2012, nearly 70% of all electricity was processed through power electronics, the rate of which is likely to reach 80 % in 2015 [1]. In modern power electronic systems, there are increasing demands to improve whole system endurance and safety level while reducing manufacturing and maintenance costs [2]. According to manufacturers' questionnaires, semiconductor devices are considered the most critical and fragile component in industrial power electronic systems [3], the failure of which result in up to 34% of power electronic system failures [4]. Because IGBTs are one of the most critical components as well as the most widely used semiconductor devices in industrial power electronic systems in the range above 1kV and 1kW [4], the reliability of IGBTs has drawn more and more attention. In particular, the ability to withstand abnormal conditions (e.g. short-circuits), is strictly required to achieve sufficient robustness in critical applications, especially where the maintenance costs are very high [5].

It is worth pointing out the junction temperature (Tj) is probably the most critical parameter responsible for IGBT converters failures. For instance, the phenomena of current constriction and thermal runaway, which cause IGBT modules failures during heavy loads and short-circuits, are commonly connected with regenerative effects involving high Tj [6]. Additionally, the final destruction coming from various failure-triggering events, (e.g. dynamic breakdown, latch-up and gate driver failure) is similarly due to high Tj [7]. Therefore, a precise electro-thermal model is required to accurately estimate the Tj in order to determine IGBT modules robustness margins and prevent potential failures with high confidence levels.

Plenty of research has been conducted into IGBT electrical-thermal co-simulation. Traditional ways of extending widely-used electrical simulation tools (e.g. Spice, Saber) to electrical-thermal simulations by introducing lumped thermal impedance, cannot provide accurate Tj as well as temperature distribution and hot spots because there are only a few thousands intrinsic nodes in such tools, which are not enough to guarantee the accuracy [8]. Finite-Element Method (FEM) software lacks optimization with respect to a multi-physics approach, resulting in a dramatic degeneration in simulation speed and accuracy. For instance, thermal simulator Icepak connected with circuit-level simulator Simplorer in ANSYS leads to heavy and slow process (seconds per simulation point). Moreover, this intrinsically-single-cell approximation method unavoidably loses plenty of information, e.g. uneven fast Tj variation and hot spots dynamics in IGBT chips, which strongly limit the prediction of imbalances among the cells of the real device. Another solution - physical cell-level (i.e. in the scale of few square microns) FEM simulation, like TCAD, can hardly predict temperature distribution among several cells [9], which is critical for studying short-circuit behavior.

Recently, a novel electro-thermal modeling method has been proposed, which combines a physics-based, device-level, distributed electrical PSpice model with a thermal FEM simulation, gaining flexibility on the electrical side without losing accuracy on the thermal side. Moreover, independent time steps are adopted for the electrical and thermal parts, thus achieving high calculation efficiency [10], [11]. This paper applies this method to model a 1.7 kV/1 kA IGBT power

module, and further study its electrical/ thermal behavior during short-circuits. The electro-thermal model is further validated by a 6 kA/1.1 kV Non-Destructive-Tester (NDT) for IGBT short-circuit tests. The paper is organized as follows: Section II introduces the basic principle of the novel electro-thermal modeling method. Then it presents the case study of a 1.7 kV/1 kA IGBT power module, to further describe the procedures, including profile definition, supervision scripts and model preparation. Section III shows the simulation results. It demonstrates the capability of the proposed method to investigate the electrical/ thermal behaviors during the power modules short-circuit, especially the electro-thermal interacting effects. Section IV briefly introduces the NDT setup, including short-circuit time setting schemes. Section V compares the modeling results with experimental results, demonstrating the new approach's accuracy and capabilities. Section V concludes the paper with discussions.

## 2 ELECTRO-THERMAL MODELING OF HIGH POWER IGBT MODULE

The basic principle of the proposed electro-thermal modeling method is described in this section. In order to illustrate this novel PSpice-Icepak co-simulation method, a case study of a 1.7 kV/1 kA commercial IGBT module is given in this section. The IGBT power module information is introduced. Then, the co-simulation configuration is explained in details, including: simulation profile definition, electrical model and thermal model configurations, as well as MATLAB supervision configuration.

### 2.1 Basic Principle

The proposed electro-thermal modeling method includes three major parts: a physics-based, device-level IGBT electrical model in PSpice, IGBT thermal analysis model in ANSYS/Icepak, and a monitoring program in MATLAB.
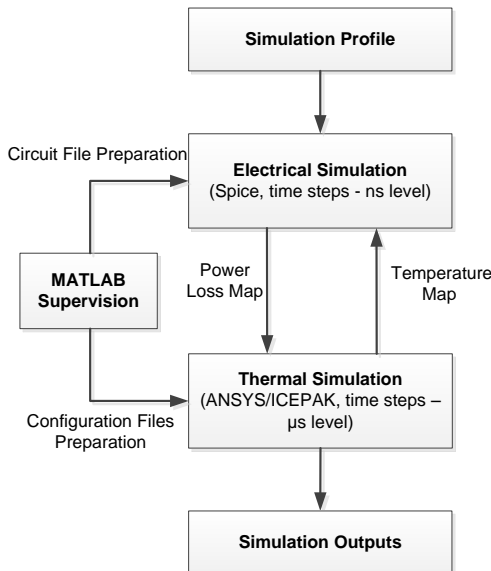


Fig. 1. Structure of the proposed electrical-thermal modeling method.
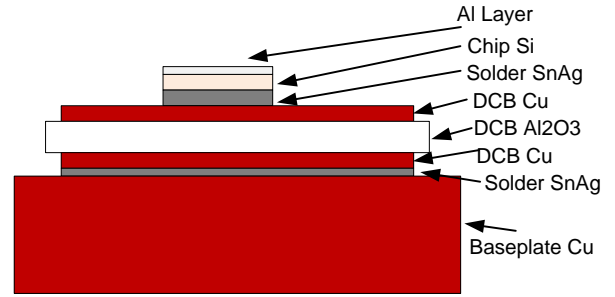


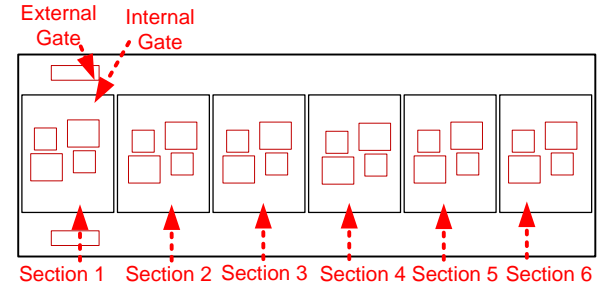Fig. 2. Schematic typical cross-section of the multilayers in IGBT power modules.



Fig. 3. Geometry of the internal structure of studied 1.7 kV/1 kA IGBT power modules.

Based on the PSpice electrical simulation, power loss distribution inside the chip is obtained and sent to the thermal simulation, and then ANSYS/Icepak thermal simulation feeds back temperature distribution to the PSpice electrical simulation, finally the chip temperature distribution can be achieved. The co-simulation process is shown in Fig. 1, of which the details will be illustrated in following sections through a case study of a 1.7 kV/1 kA IGBT power module.

### 2.2 Information about the Studied IGBT Module

This 1.7 kV/1 kA IGBT power module is widely used in high power applications, for instance wind turbine systems. The main specifications of the IGBT module are shown in Table I. The chips are soldered on a standard Direct Copper Bonded (DCB) layer, which is further soldered to a Cu baseplate, and the cross section structure is plotted in Fig. 2. It is worth noting there are six identical sections connected in parallel to increase the current capability, as shown in Fig. 3, so that the rated short-circuit current is 4 kA. Each section includes two IGBT chips and two freewheeling diode chips, which are configured as a half-bridge.

| Characteristic | Value |
|---|---|
| Collector-emitter voltage $V_{CES}$ | 1.7 kV |
| Continuous DC collector current $I_{Cnom}$ | 1 kA |
| Rated short-circuit current $I_{SC}$ | 4 kA |
| Gate-emitter maximum voltage $V_{GES}$ | +/- 20V |
| Number of parallel sections | 6 |

Table 1 –The studied IGBT power module main specifications.

### 2.3 Simulation Profile Definition

As is well known, the most critical abnormal working

condition for IGBTs is short-circuit, where both high voltage and high current are applied to the device at the same time. Therefore, a standard 10 μs short-circuit duration is chosen in the case study, with a thermal simulation step of 1 μs. It is worth noting that the diodes do not operate in this case study.

A MATLAB script is implemented to prepare configuration files and then coordinate information sharing between the other software at each thermal simulation step. Operations are divided into preparation state and simulation state.

During the preparation state, the MATLAB script automatically divides the device under simulation (i.e. the IGBT) into a specific number of virtual cells, which should be rectangle-shaped. Each cell includes one power source and one temperature monitoring point, which are placed in the IGBT body. One PSpice sub-circuit is automatically generated for each cell starting from a circuit template file, that includes the parameter identified for the considered device, and all of them are connected in parallel. The user should also define the external PSpice circuit profile as normal operation, overload or short-circuit.

During the simulation state, the power loss of each cell is calculated by the PSpice circuit with time resolution of nanoseconds for a given constant temperature map. The PSpice simulation lasts a thermal time step (typically in the range of microseconds) and it is stopped. At this point, dissipated power losses are given to the thermal simulation –



*(a)*



*(b)*

*Fig. 4. IGBT thermal model constructed in Icepak: (a). geometry of one section of IGBT power module, (b) details of the cross section on the vertical plane.*

the corresponding files in Icepak are updated accordingly, and the thermal simulation in Icepak is then done. Afterwards, the temperature data are transferred back to the PSpice model and so forth.

In the electrical model, the studied IGBT chip is divided into 4 by 4 cells. According to the information from manufacturer, the IGBT module's stray inductance is 10 nH, its gate capacitance is 81 nF, while the IGBT chip is 12.6 mm by 12.6 mm square size. Based on the datasheet information, corresponding IGBT lumped charge model can be obtained according to the method in [12].

Based on the information provided by the IGBT manufacturer, one IGBT section model is constructed in Icepak for thermal simulation. The geometry information of one section in Icepak is shown in Fig. 4 (a), and the cross section of the Icepak model is shown in Fig. 4 (b). It contains Al top layer, IGBT trench gate layer, IGBT body layer, solder, DCB and baseplate. Power source is located in the IGBT body layer. 543,000 nodes are defined in Icepak model. The thermal conductivity and heat capacity information of the materials used in the simulations at 25 ℃ are listed in Table 2.

| Material | Thermal Conductivity (W/m-K) | Heat Capacity (J/Kg-K) |
|---|---|---|
| Aluminum | 237 | 897 |
| Silicon | 148 | 705 |
| Solder | 57 | 220 |
| Copper | 401 | 385 |

*Table 2 – IGBT power module material thermal properties at 25 ℃ [13].*

## 3  ELECTRO-THERMAL SIMULATION RESULTS

As mentioned in last section, a standard 10 μs short-circuit duration has been chosen in the case study. There are two different short-circuit types: Type 1 short-circuit happens during IGBT turn-on, while Type 2 short-circuit happens when IGBT is at on-state, as illustrated in Fig. 5. At present, only type 1 short-circuits are studied in this paper.

### 3.1  *Electrical Simulation Results*

When a short-circuit happens during IGBT turn-on (at 5 μs), collector current Ic rises rapidly until reaching the saturated value of 780 A. It is noted that the IGBT chip's rated current is 150 A. Due to the high current slope di/dt and the stray inductance, there is a voltage drop during the short-circuit turn-on, at the collector voltage waveform. The PSpice simulation results are plotted in Fig. 6.

According to semiconductor physics, IGBT short-circuit current decreases with the junction temperature rising [14]. This phenomenon is also evidenced in the simulation, as shown in Fig. 6. Because the IGBT cells temperature is updated every thermal step – 1 μs, the short-circuit current also decreases by 1 μs step. As introduced in Section II, part 3, the thermal step duration can be modified in the MATLAB script according to requirements.

The voltage overshoot during the short-circuit turn-off is also because of the high current slope di/dt and the stray
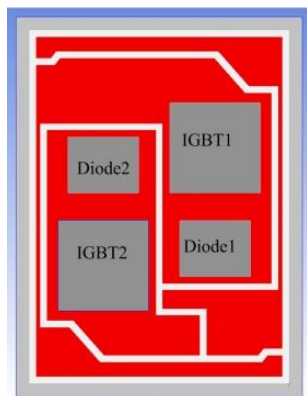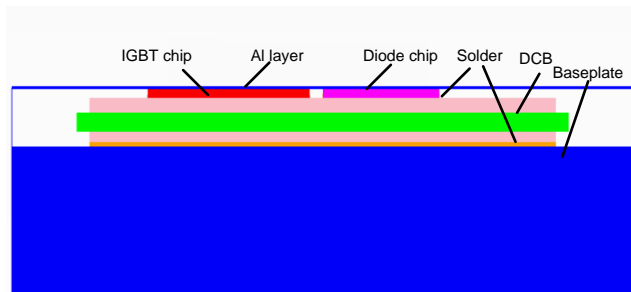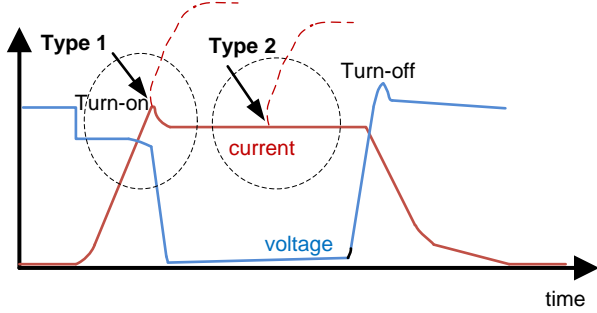
Fig. 5. Two types of short-circuits: Type 1 occurs during turn-on, Type 2 occurs during conduction state.
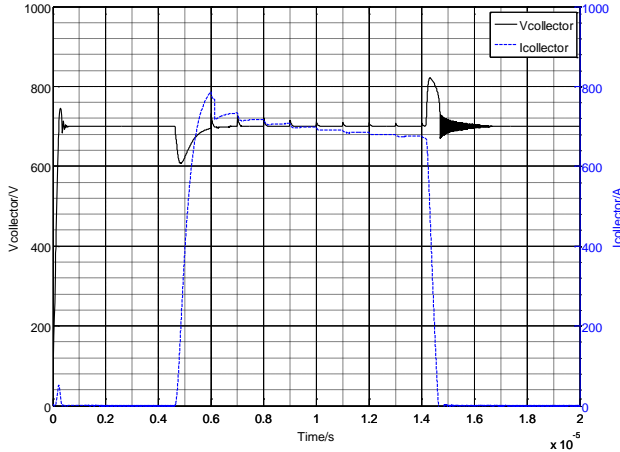


Fig. 6. PSpice simulated short-circuit current/voltage waveforms of the IGBT chip.

inductance.

### 3.2 Thermal Simulation Results

Four chip temperature maps obtained during short-circuit are depicted in Fig. 7. They are before short-circuit (at 2 µs), during short-circuit (at 10 µs), after short-circuit (at 16 µs and 18 µs) respectively. In the study case, temperature rises almost uniformly on the whole chip, but still some differences can be observed. This is because of the not perfectly equal current distribution among cells. The cells under bond-wires are conducting more currents than the others.

Before short-circuit, the chip is at room temperature (25 ℃) (as shown in the first picture at 2 µs). During short-circuit (at 10 µs): cells under bond wires (cells 1-4 and cells 9-12) are about 5 ℃ hotter than other ones because of the imbalanced current. After the turn-off of short-circuit, the temperature keeps rising due to the heat flow from the Si layer. IGBT chip's temperature rises as high as 150 °C at 18 µs due to the high energy shock in these conditions.

### 4 EXPERIMAL VALIDATION BY MEANS OF NON-DESTRUCTIVE TESTING SETUP

#### 4.1 Testing Setup Structure and Principle

The most critical abnormal working condition for IGBTs is a short-circuit, where both high voltage and high current can
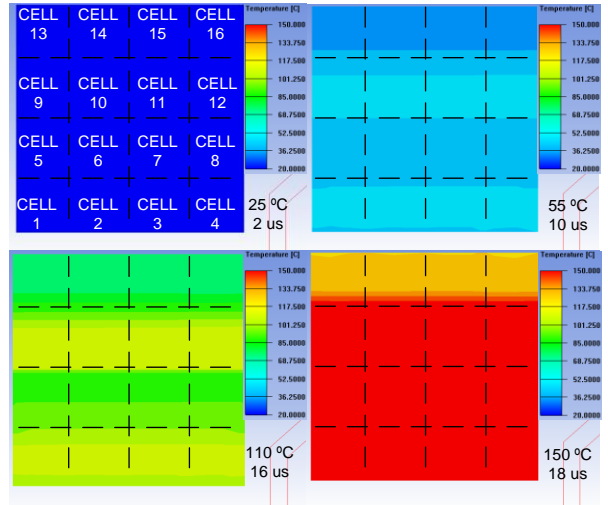


Fig. 7. IGBT power module chip temperature map in Icepak during short-circuit at 2/10/16/18 µs (times and highest temperature at bottom right of each image) (Temperature color bar – max 150 ℃, min 20 ℃).

damage the device within several tens of µs. In order to test short-circuits without damage, a non-destructive testing method has been proposed, the circuit of which is shown in Fig. 8. The NDT includes the Device Under Test (DUT), the series protection, parallel protection, load inductance $L_{load}$, DC link capacitance $C_{DC}$, a high voltage power supply $V_{DC}$, Schottky diodes, negative-voltage capacitance $C_{NEG}$ with corresponding negative voltage supply $V_{NEG}$.

The NDT structure includes the following parts. A high-voltage power supply charges up a high-voltage capacitor bank $C_{DC}$. The stored energy is used to supply power for short-circuits. The on-state series protection switch will be switched off immediately after the test and save the DUT. A Computer-Aided-Design (CAD) busbar has been developed to minimize the overall circuit inductance by optimization of the mutual coupling of the busbar components [15]. A 100 MHz FPGA provides the driving signals for the DUT and the switches for the protection, and also provides the precise time control for electrical measurement. The remote control and data acquisition is achieved by a Personal Computer (PC) which supervises the operation by connecting a LeCroy HDO6054-MS oscilloscope via an Ethernet link and a FPGA board through an RS-232 bus. Two commercial IGBT drivers drive
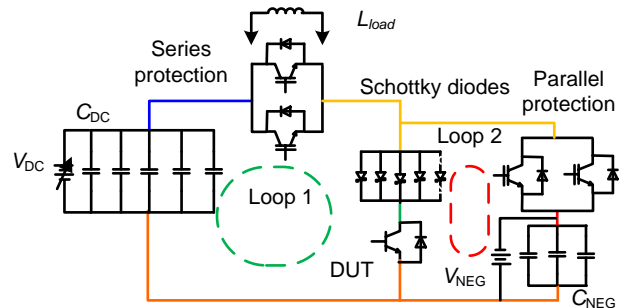


Fig. 8. Detailed schematic of the power circuit of the Non-Destructive Tester.

the protection switches and the DUT respectively. In order to perform short-circuits, the corresponding protection circuit on the DUT drivers has been deactivated. During tests, collector current, collector voltage and gate voltage waveforms are acquired together with the current flowing through a specific section of the DUT.

The operating principle is as follows: as shown in Fig. 6, the power circuit is divided into two loops –Loop 1, (the main loop) including the series protection, and Loop 2, including a parallel protection; the DUT is located in the common branch. The tester is operated in a standard single-shot way, so that the energy stored in the capacitors $C_{DC}$ is used for the tests. $C_{DC}$ and $C_{NEG}$ are composed of five and three capacitors in parallel, respectively, in order to reduce the intrinsic stray inductances. The same principle has been adopted for the two switches of the series protection, the two switches of the parallel protection and the five Schottky diodes.

Loop 2 is designed to improve the performance of the NDT. The "non-destructive testing" means that the series protection is activated right after the commutation to prevent the DUT from explosions in case of failure. This capability is strictly dependent on the series protection's capability to cut the current flowing through the DUT to zero immediately after the test. However, the turn-off transition of the series protection is non-ideal because IGBT switches have current tails, which would continue flowing through the DUT. To avoid this effect and divert the current tail, the parallel protection is fired up together with the activation of the series one. As demonstrated in [16], to improve the parallel intervention as well, a negative voltage biases a capacitor bank $C_{NEG}$ in order to enhance the voltage fall promptness during IGBT turn-on. Furthermore, to avoid a negative current flowing through the DUT, the Schottky diode bank is placed in series.

### 4.2 Short-circuit Operation Time Setting

The NDT can provide both short-circuit types by different configuration and control time schemes. At present, only type 1 short-circuits are studied. The circuit configuration and the control timing scheme for type 1 short-circuits are illustrated as follows:

Type 1 short-circuits happen at the device turn-on transient. The load inductance $L_{load}$ is removed in the main
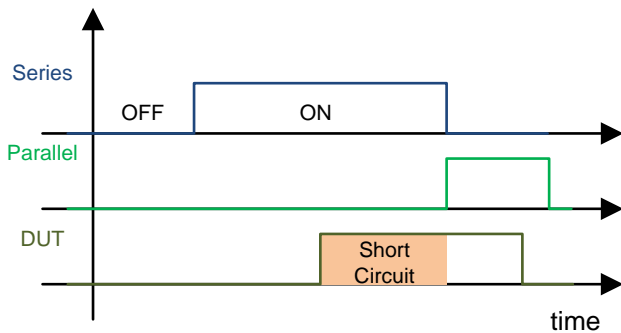


Fig. 9. Control timing settings of all the power devices for Type 1 short-circuit.

circuit. Before tests, the series protection is in on-state and the parallel protection is in off-state. Loop 1 has the stray inductance only and the Schottky diodes behave almost ideally, so the DUT is connected directly to the $C_{DC}$ capacitors. During the tests, the DUT falls to short-circuit when it is triggered. After the precise controlled time by 100 MHz FPGA, the DUT short-circuit is switched off by series protection IGBTs. At the same time, the parallel protection is turned on to avoid the undesirable tail current through DUT. The corresponding control time sequences of the series and parallel protections and DUT are as shown in Fig. 9. The negative voltage $V_{NEG}$ can speed up the parallel protection, and the Schottky diodes can avoid a current flow from the DUT to the negative voltage.

### 4.3 Experimental Validation

In order to validate the electro-thermal model of the power module, the short-circuit tests have been carried out at the same condition of the simulation. A 10 µs short-circuit test at 700 V for the studied power module has been performed in the laboratory at room temperature (25 ℃). The short-circuit current of one IGBT chip reaches 780 A, and decrease as the
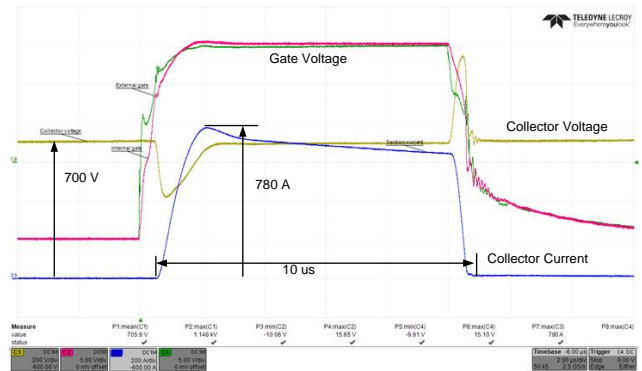


*(a)*
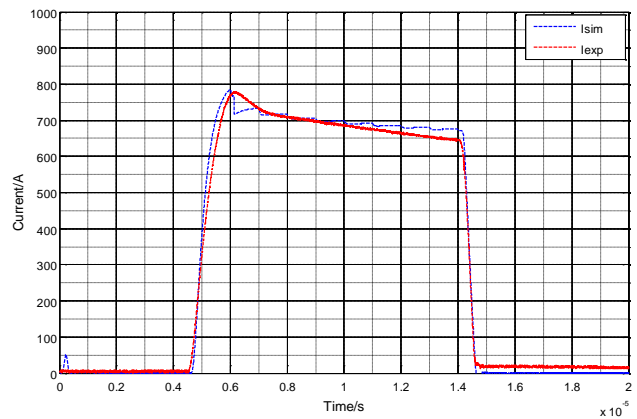


*(b)*

*Fig. 10. (a). Experimental collector voltage and current waveforms during a 700 V/10 us short-circuit for the IGBT module at room temperature 25 ℃, (b). comparison between the simulated short-circuit current and the experimental one under the same condition.*

time increasing. Experimental collector voltage/ current waveforms are shown in Fig. 10(a). Due to the test circuit stray inductance, it is observed the collector voltage undershoot and overshoot at the starting and end of the short-circuit operation, respectively.

The comparison between the simulated and experimental short-circuit currents is shown in Fig. 10(b). It shows that the co-simulation can predict short-circuit current precisely; especially how short-circuit current decreases due to self-heating effects.

*CONCLUSIONS*

An advanced IGBT electro-thermal modeling approach has been presented to study short-circuits of a 1.7 kV/1 kA commercial IGBT module. The approach successfully predicts the current and temperature distribution inside the chip of power IGBT modules, which is further validated by a 6 kA/1.1 kV non-destructive tester. The experimental validation demonstrated the modeling approach's capability for assisting in reliability design of high power IGBT power modules with respect to electrical/thermal behavior under severe conditions.

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Rui Wu received the B.Sc. degrees in electrical engineering from Huazhong University of Science and Technology, Wuhan, China, in 2009 and M.Sc. in Power Electronics from China Electric Power Research Institute, Beijing, China in 2012 respectively. He was also employed at China Electric Power Research Institute in 2012. He is currently working toward the Ph.D. degree in Aalborg University, Denmark. His research interests are multi-physics modeling of power devices and power device's behavior during abnormal conditions, especially short-circuits.

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Francesco Iannuzzo earned his Ph.D. degree in Electronics and Information Engineering from the University of Naples, Italy, in 2001, with a study on the reliability of power MOSFETs during diode operations. He is primarily specialized in the field of power device modelling.

He is full professor of Reliable Power Electronics at the Aalborg University, Denmark, where he is also part of CORPE (Center of Reliable Power Electronics http://www.corpe.et.aau.dk). He is author or co-author of more than 90 publications on journals and international conferences. His research interests are in the field of reliability of power devices, including against cosmic rays, power device failure modelling and development of non-destructive testing facilities for assessment of MW-scale power modules under extreme conditions.

Prof. Iannuzzo is a senior member of the IEEE (Reliability Society and Industrial Electronic Society) and of AEIT (Italian Electric, Electronic and Telecommunication Association).

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He has been with Aalborg University, Aalborg, Denmark, since 2012, where he is currently an Assistant Professor with the Department of Energy Technology. He is a Visiting Scientist with the ETH Zurich, Zurich, Switzerland, from August to September, 2014 and with the Massachusetts Institute of Technology (MIT), Cambridge, MA, USA, from September to November, 2013. He was with the ABB Corporate Research Center, Baden, Switzerland, in 2009. He has contributed over 20 journal papers and filed four patents. His current research interests include the reliability of DC-link and AC filter capacitors, reliability of power electronic systems, high voltage DC-DC power converters, time-domain control of converters, and passive components reduction technologies.

Dr. Wang is a recipient of the five paper awards and project awards from industry, IEEE, and the Hong Kong Institution of Engineers. He serves the Guest Associate Editor of the IEEE Transactions on Power Electronics Special Issue on Robust Design and Reliability in Power Electronics, and a Session Chair of various conferences in power electronics.

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Frede Blaabjerg was with ABB-Scandia, Randers, Denmark, from 1987 to 1988. From 1988 to 1992, he was a Ph.D. Student with Aalborg University, Aalborg, Denmark. He became an Assistant Professor in 1992, an Associate Professor in 1996, and a Full Professor of power electronics and drives in 1998. His current research interests include power electronics and its applications such as in wind turbines, PV systems, reliability, harmonics and adjustable speed drives.

He has received 15 IEEE Prize Paper Awards, the IEEE PELS Distinguished Service Award in 2009, the EPE-PEMC Council Award in 2010, the IEEE William E. Newell Power Electronics Award 2014 and the Villum Kann Rasmussen Research Award 2014. He was an Editor-in-Chief of the IEEE TRANSACTIONS ON POWER ELECTRONICS from 2006 to 2012. He has been Distinguished Lecturer for the IEEE Power Electronics Society from 2005 to 2007 and for the IEEE Industry Applications Society from 2010 to 2011.