Electro-thermal Simulations of Strained-Si MOSFETs under ESD conditions

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Abstract

Electro-thermal characteristics of strained-Si MOSFETs operating in high-current, high temperature regimes were investigated using device/circuit mixed mode simulations. The material parameters of strained-Si were calibrated for device simulations. Especially the phonon mean-free-path of strained-Si with high electric fields was estimated based on a full-band Monte Carlo device simulation. Despite the low thermal conductivity of buried SiGe layers, strained-Si devices show superior ElectroStatic Discharge (ESD) protection capability compared to unstrained-Si (bulk-Si) devices due to the high bipolar current gain and increased impact ionization rate.

1 Introduction

Strained Si/relaxed $Si_{1-x}Ge_x$ MOSFET has been suggested as a promising device for beyond the 50 nm CMOS node. It can overcome drive current scaling limitations because of its enhanced low-field electron mobility in the thin epi-Si layer. However, the low thermal conductivity of relaxed SiGe layers (~15 times lower than that of bulk-Si [1,2]) causes severe self-heating, considerably changing some electrical properties of a strained-Si/relaxed SiGe system in high current operation. In addition, since thermal properties of transistors are critical for ESD and other reliability problems, studying electro-thermal characteristics of strained-Si is of technological importance.

In this work, electrical and thermal characteristics of strained-Si are compared with bulk-Si by using device simulations with the phonon mean-free-path determined from the full-band Monte Carlo analysis. ESD protection capability of strained-Si devices is compared with bulk-Si devices by injecting the Human Body Model (HBM) and Machine Model (MM) ESD stress [3].

2 Calibration of Simulation Parameters

The energy band structure of strained-Si devices is determined using material parameters based on Ref. [1,4]. Fig. 1 shows simulated energy band diagrams for strained- and bulk-Si devices [5]. The strained-Si NMOSFET has a strained-Si layer of 15 nm thickness and source/drain junction depth of 50 nm. The gate length and gate oxide thickness are 130 nm and 2.5 nm, respectively. The energy band gaps of strained Si and $Si_{0.75}Ge_{0.25}$ are 0.98 and 0.90 eV, respectively, and the band gap of Si is 1.08 eV at the room temperature. Temperature dependent carrier mobility models and temperature dependent band gap models [6] are employed to account for thermal effects.

The phonon mean free path of electrons (λ_n) is closely related to energy relaxation times in scattering processes [7]. Energy relaxation times for strained-Si were therefore calculated using full-band Monte Carlo (FBMC) device simulations [8]. Fig. 2 shows the calculated energy relaxation times for electrons in strained-Si and bulk-Si with respect to electric field. In [1], the energy relaxation time was increased by roughly a factor of two from the bulk-Si value. However, the FBMC simulation results in Fig. 2 show that the increase of energy relaxation time of the strained-Si, relative to bulk-Si, is reduced as the electric field increases. This implies that the mean-free-path (λ_n) in strained-Si for high current operation should be reduced from the value used in the lower electric field regime. In this work, λ_n of strained-Si on $Si_{0.75}Ge_{0.25}$ layer is assumed to increase by 50 % from that for bulk-Si; λ_n = 10 nm for bulk-Si and λ_n = 15 nm for strained-Si on $Si_{0.75}Ge_{0.25}$.

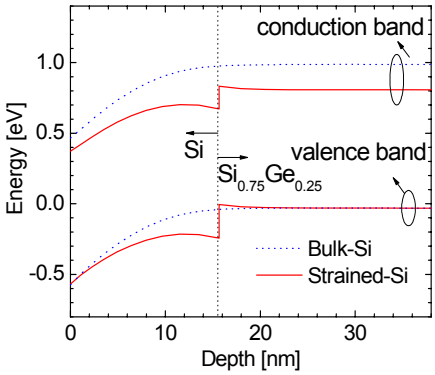


Figure 1: Simulated band-diagrams of strained- and bulk-Si devices along the depth direction at V_G = 0 V.

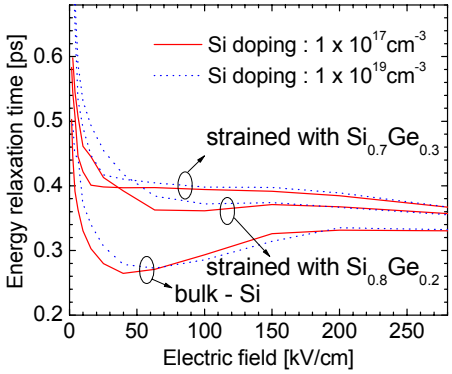


Figure 2: Electron energy relaxation times with respect to electric fields for strained- and bulk-Si.

3 ESD Simulation Results and Discussions

Electro-thermal device simulations were performed for strained- and unstrained-Si (bulk) NMOSFETs based on the previously determined material parameters. Various levels of HBM, MM ESD pulses were injected into the drain of 100 µm wide NMOSFET, while the gate, source, and substrate are grounded.

Fig. 3a shows simulated I_D and V_D curves as functions of time with 2.4 kV HBM stress. As can be seen here, the current rise time is ~10 ns and the current increases up to ~1.5 A. In Fig. 3b, I_D - V_D curves extracted from Fig. 3a are illustrated. The impact ionization rate and the current gain, β of the parasitic npn transistor in strained-Si are expected to be higher than those for bulk-Si devices. The snapback voltage (V_{TI}) of strained-Si devices is therefore lower than that for bulk-Si devices and the hold voltage (V_h) -the minimum voltage required for the bipolar operation- is also lower for strained-Si devices. From an ESD perspective, a protection device with high β and low V_h in SiGe technology are advantageous for discharging ESD stress current [9], since lower V_h generates less heat under high current conditions. When the current rises further above 0.5 A, lattice temperatures inside the stressed devices rise significantly, reducing carrier mobility and increasing on-resistance as shown. As both on-resistance and lattice temperatures increase further, the bandgap is reduced

significantly, which triggers the second breakdown (as indicated by V_{T2} and I_{T2} in Fig. 3b. The second breakdown triggering current (I_{T2}) of strained-Si devices is higher than that of bulk-Si devices by ~7 %.

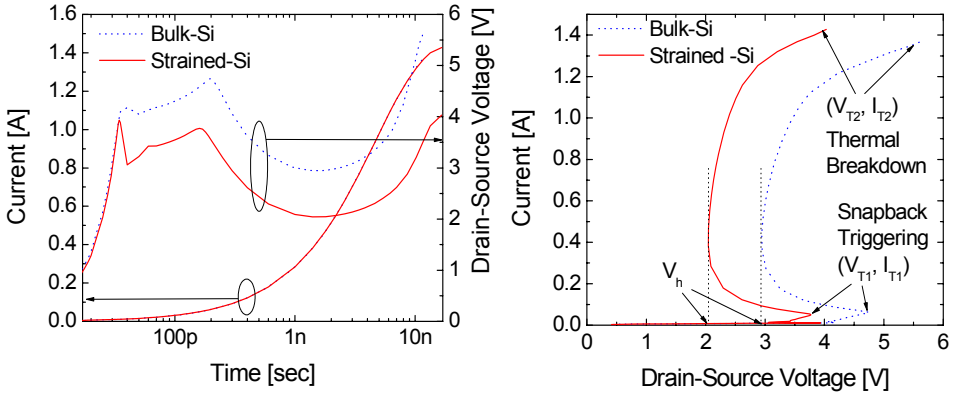


Figure 3: (a) Simulated I_D and V_D as functions of time for strained- and bulk-Si NMOSFETs with gate grounded. 2.4 kV HBM ESD stress is applied. (b) I_D *vs.* V_D curves for the strained- and bulk-Si NMOSFET with gate grounded.

ESD simulations with the HBM and MM stress show that strained-Si devices fail at 2.4 kV HBM and 150 V MM stress levels while bulk-Si fail at 2.0 kV HBM and 130 V MM. These simulation results imply that the power density and peak lattice temperature during parasitic bipolar operation are lower for the strained-Si device than those for the bulk-Si device, even though thermal dissipation of strained-Si devices is much less compared to bulk-Si. In other words the local overheating inside strained-Si NMOSFETs can be effectively suppressed owing to the higher current gain (β) of the parasitic npn transistors.

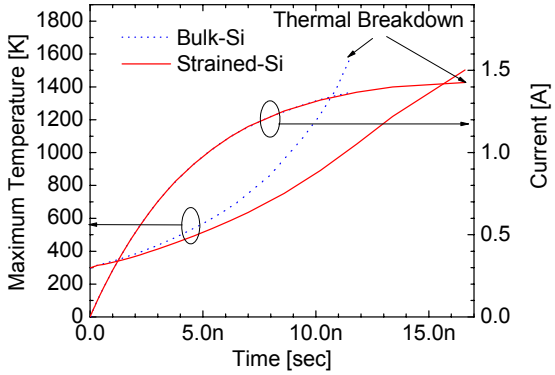
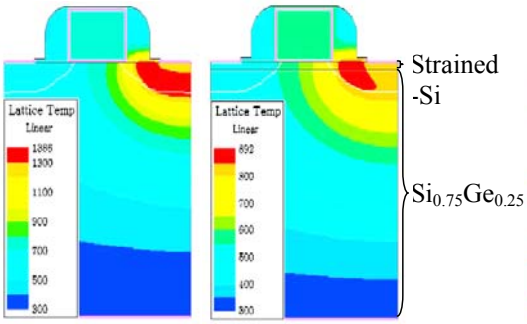


Figure 4: The peak temperatures inside both strained-Si and bulk Si devices, as functions of time after 2.4 kV HBM ESD stress being initiated (I_D is also plotted).

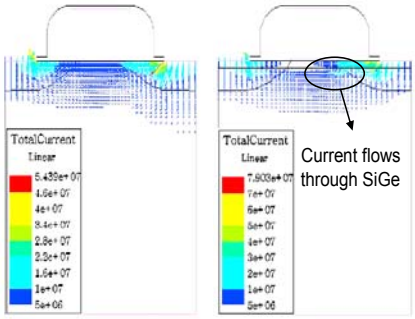
Fig. 4 shows the peak temperatures as functions of time after 2.4 kV HBM ESD stress being initiated. The temperature in bulk-Si increases faster, while having an almost same I_D over the whole duration of the ESD event. Fig. 5 shows temperature contours for bulk-Si and strained-Si devices at 10 ns when the current reaches ~1.3 A. As

expected in Fig. 4, local heating near the drain region of bulk-Si is severer. The peak lattice temperature of bulk-Si (~1350K) is therefore much higher than that of strained-Si (~890 K). It is worth pointing out that in strained-Si devices under ESD conditions, current flows mainly through the SiGe layer rather than through the surface layer as observed in Fig. 6. This phenomenon can suppress current localization at the Si surface, suggesting that once the parasitic bipolar turns on, uniform conduction can be achieved in strained-Si devices due to the high β of parasitic npn transistors [9, 10].



Bulk-Si Strained-Si

Figure 5: Temperature contours for bulk-Si and strained-Si devices at 10 ns after initiating an ESD pulse.



Bulk-Si Strained-Si

Figure 6: Current vector plots for bulk-Si and strained-Si devices at 10 ns after initiating an ESD pulse.

4 Conclusions

In this work, we have shown that strained-Si/SiGe NMOS devices show superior ESD protection capability compared to bulk-Si devices. Strained-Si devices have higher bipolar current gain and impact ionization rates compared to bulk-Si devices due to narrower energy band gap and longer phonon mean-free-path. Owing to the better performance of parasitic npn transistors, the local overheating can be effectively suppressed in strained-Si devices so that the second breakdown triggering current for strained-Si devices is higher than that of bulk-Si devices by ~7 %. Furthermore, strained-Si devices are also expected to have better current uniformity, since main current path during the parasitic bipolar action is through the buried SiGe layer. Contrary to the case of SOI devices which have similar self-heating and heat confinement problems, strained-Si NMOS devices can be used effectively for ESD protection devices

References

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