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Wang, Wenbo

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Electromagnetic Design of High Frequency PFC Boost Converters using Gallium Nitride Devices

Wenbo Wang

王文博

Electromagnetic Design of High Frequency PFC Boost Converters using Gallium Nitride Devices

Proefschrift

ter verkrijging van de graad van doctor

aan de Technische Universiteit Delft,

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voorzitter van het College voor Promoties,

in het openbaar te verdedigen op

donderdag 19 oktober 2017 om 10:00 uur

Door

Wenbo WANG

Master of Engineering, Northwestern Polytechnical University, China

geboren te Shandong, China

This dissertation has been approved by the

promotor: Prof. dr. J.A.Ferreira

Composition of the doctoral committee:

Rector Magnificus	Chairman
Prof. dr. J.A.Ferreira,	Delft University of Technology, promotor
Dr. J. Popovic,	Delft University of Technology, co-promotor

Independent members:

Prof. dr. G.Q.Zhang	Delft University of Technology
Prof. dr. J.J. Smit	Delft University of Technology
Prof.dr. L. Wang	Xi'an Jiaotong University
Prof.dr. N. Kaminski	University of Bremen

Other member:

Ir. F. Pansier	Delft University of Technology, advisor

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To my parents

献给我的父母

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People may be born equal overall, but not so in every single measure. There are people with better intuitive feelings over one particular subject than others, the ones naturally have stronger curiosity compared to the rest, those who are inherently more patient, etc. When I began my Ph.D, I felt like I have got nothing. Power electronics was more of one course to me rather than something I had great interests in. With the starting project of passive integration, I did not have much motivation and enthusiasm in asking why and finding out reasons behind. Moreover, I showed a lack of patience in adjusting myself to be initiative and to work in a systematic way. Needless to say, I had a really bad start and never pictured what it would be like when I finish. Now, I managed to translate the research work conducted in the past few years into this thesis. There have been many people who helped, encouraged, supported and accompanied me through these years and thus contributed to my work and this thesis either directly or indirectly. I would like to take this opportunity to express my gratitude and appreciation to them.

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Chapter 1. Introduction

1.1 Thesis Background

Power Electronics, in general, is an enabling technology that facilitates efficient conversion, control and conditioning of electric power from power sources to loads [1-1]-[1-4]. Nowadays, almost all kinds of electrical energy processing in industrial, commercial, residential, utility, transportation, aerospace and military applications benefit from employments of power electronics systems [1-1] [1-3]-[1-5]. The development of power electronics, therefore, is driven by both the push from innovations in the technology itself and the pull from requirements of the applications it is used in [1-6].

1.1.1 Demands on performance of power electronics systems- Application pull

Power electronics systems are spreading into every corner of transportation, industry, lighting, consumer, communication and energy generation, transmission and distribution applications [1-2]. Within each section of application category, power electronics systems are facing different energy sources, diversity in the loads, wide power level span, etc. And therefore, demands on performance measures of power electronics system can diverse a lot depending on environmental conditions and regulatory requirements of the specific application. Many different kinds of application requirements have been identified and categorized, such as high efficiency, high power density and low cost.

High efficiency is a crucial demand of power electronics systems driven mainly by regulations originated from purpose of energy-saving. Since most of electrical energy now flows through power electronics systems, slight efficiency increase in power electronics systems would lead to great energy savings worldwide [1-5]. In European Union (EU), for instance, electric energy consumption was reported occupying 20% of total final energy consumption in 2009 and will be growing much faster than any other energy sources in the following few decades. It was predicted that by implementing power electronics systems in three key application groups as listed in Figure 1.1, which contribute to 78% of electric energy consumption in total, about 25% of EU electricity consumption can be saved [1-7]. Efficiency improvements in these power electronics systems would result in further great energy consumption reduction across EU. Moreover, current trend of ever-increasing demand for energy, pressing dwindling of fossil fuels and urgent need to mitigate environmental pollution and climate change problems has resulted in tightened regulatory requirements and increased energy price. Increasing efficiency of power electronics systems will therefore directly bring financial benefits and indirectly help to save energy and ease environmental problems. In the past few decades, efficiency increase in power electronics systems is made possible mainly by progress in power semiconductor devices. Development of

traditionally used Si devices, as will be elaborated further in 1.1.2, is entering into maturing stage after the uninterrupted improvements of the technology for three decades. Further performance improvements of power semiconductors are still needed as Si devices usually account for an important share of power loss and have noticeable effects on overall efficiency in today's power converters, especially the hard-switching [1-8] [1-9]. The dilemma cannot be overcome without a radical change in power semiconductor technology.

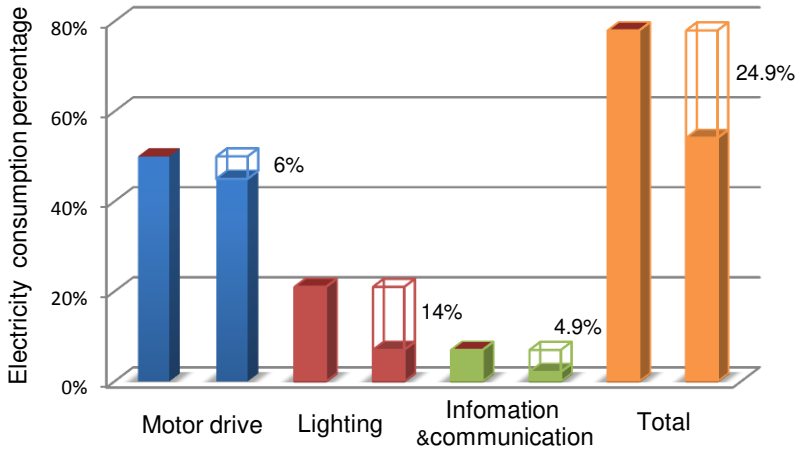


Figure 1.1. Electric energy saving potentials by application of power electronics in EU [1-7]

High power density is required in applications where space and/or weight is limited such as portable devices, automotive, lighting aerospace and telecom facilities. In applications with relatively less strict demand on volume reduction, power electronics systems and their associated thermal management can take large part of the whole system footprint and it is favourable to push power density of these systems to higher level as well. Increase of power density has traditionally been achieved by pushing up operation frequencies of power converters utilizing faster-switching Si power semiconductors to reduce size of bulky passives components while keeping switching loss of the semiconductors, and the volume of cooling system thereof, low. Take Si transistor based POL converters as an example, as illustrated in Figure 1.2, the increase of power density is made possible through both increase in operation frequency to reduce size of passive components and decline in power handling to keep size of the thermal management parts small. Adoption of this approach to achieve higher level power density is being challenged by the fact that, with operation frequency being pushed up, volume distribution within a power electronics system is changing i.e. the size-dominating part is shifting from passives to cooling constructions [1-10]. As size of the cooling construction is determined mostly by both the amount of loss in power semiconductors and high temperature operation capability of the device, better device is needed. Consequently, to further increase power density of a power electronics system, transistors more suitable for operating in elevated frequencies than state-of-art Si devices have to be applied. In fact, application of low voltage GaN devices in the conventionally Si device based

POL converters to further increase power density of the converters has already been performed, as can be seen in Figure 1.2. Due to the lack of suitable high voltage devices, further increase of power density in line-voltage power converters e.g. PFC boost converter, unfortunately, has not been accomplished.

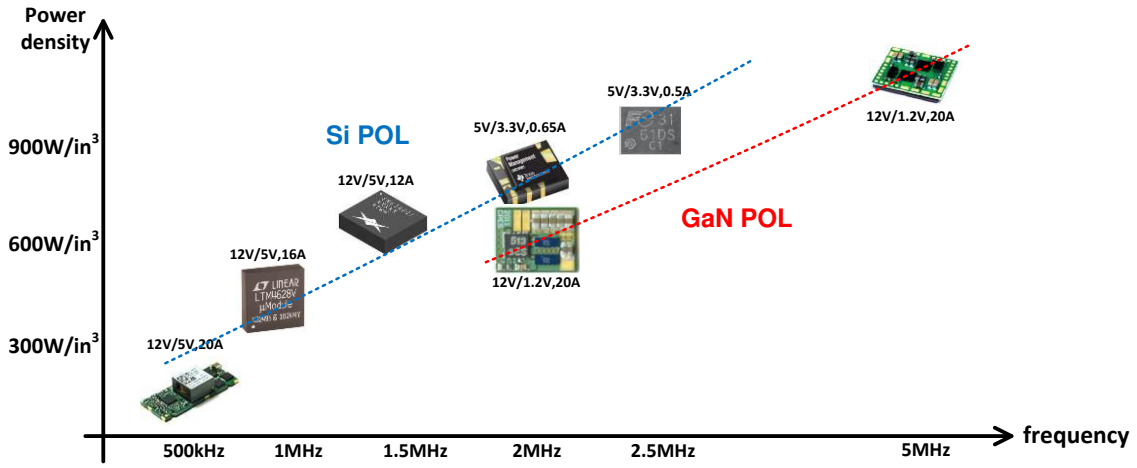


Figure 1.2 Power density increase by pushing up operation frequency in POL converters [1-11] - [1-13]

(Specification: input voltage/output voltage, output current)

Low Cost has always been and will continue to be one important measure that is common to all power electronics systems. A typical power electronics system usually is assembled with power devices mounted on heatsinks while the passives, control circuits, protection circuits etc. implemented on PCBs [1-14]. Cost in a power electronics system, accordingly, includes component cost (passive and active components), mechanical parts (PCBs, connectors, etc.) and thermal parts (heatsinks) cost, assembly cost (labor), etc. Currently, there's a trend of rising cost of copper and magnetic material and falling cost of Si based semiconductor products, which makes size and volume reduction of magnetic parts critical to further compress cost of components [1-15]. As PCB construction technology is maturing, room for cost reduction of PCB per unit area is limited. Since the size and volume of heatsink needed depends greatly on the amount of loss in a power device and the maximum temperature the device can work at, cost of the thermal parts can be lowered if thermal burden is relieved i.e. loss in power devices are reduced or the device can handle higher thermal stress. Assembly of power electronics products is labor-intensive as different kinds of assembling technology are demanded, ranging from electric parts to mechanical parts, from through hole technology to surface mount technology, and so on. Although there are efforts to reduce assembling cost, development of standardized components for instance, the most common practice taken by power electronics product manufacturers is to have the assembly processed in low labor cost countries like China [1-2]. In fact, the manufacturing now is moving to countries like India and Vietnam where labor is even cheaper to minimize assembling cost. Given current status and future trend on costs of different

sectors in a power electronics system, there's still room for cost reduction if size of both magnetic components and heatsinks can be reduced. To fulfill this further cost reduction need, power semiconductor devices that are capable of operating at high operation frequency with low loss need to be developed.

There are also other performance measures, such as high reliability, long lifetime, high modularity, high maintainability etc. [1-8]. However, in one way or another, they all couple with at least one of the three factors discussed above. For example, as losses will be dissipated in the form of heat in a power electronics system, increasing efficiency i.e. reducing loss would decrease temperature of components and mechanical parts like wire/connectors leading to prolonged lifetime and enhanced reliability of the system as a whole in the long run. On the other hand, with sufficient loss reduction, heatsinks maybe exempted from a power electronics system, resulting in more compact design and thus ease the task of modularity.

1.1.2 Developments of power semiconductor technologies- Technology push

It is well acknowledged that power semiconductor is the heart of a power electronics system, and performance improvements of the system depends, to great extent, on innovations of the switching device [1-1]. Improvements in circuits or topologies, control, passive components and packaging techniques, etc. also contribute to the development of power electronics. However, these technologies generally follow the development of power semiconductors to best accommodate the semiconductors in different applications [1-16].

There are different opinions on which event marks the beginning of power electronics, e.g. Bimal K. Bose considered the appearance of glass-bulb mercury-arc rectifier in 1901, while Thomas G. Wilson preferred the invention of magnetic amplifier in 1912 [1-1] [1-17] [1-19]. There is, however, no dispute over the fact that revolutionary development of power electronics technology did not start until controllable solid-state electronic devices appeared. Commercial availability of thyristor or SCR (silicon controlled rectifier) and bipolar junction transistors (BJT) in the 1950's stimulated rapid expansion of power electronics in conversion and control of electric power. With the help of continuous improvements on characteristics and reliability of the devices, in particular the disclose of Gate Turn Off thyristor (GTO), thyristors dominated in high power applications for almost two decades. In fact, thyristors are still active today in high power, low frequency applications. Meanwhile, BJTs were favored in low and medium power applications. Although there have been great efforts to increase the ratings of BJTs e.g. the introduction of Darlington structure, due to inherent demerit of current-control technology and limited switching speed, the BJTs were gradually replaced by MOS (Metal-Oxide-Semiconductor) gated, voltage-controlled transistors from late 1970's [1-17] [1-18]. The advent of insulated-gate power devices, in particular MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) in the 1970's and IGBT

(Insulated Gate Bipolar Transistor) in the 1980's, are significant milestones in the history of power semiconductors as these devices have been shaping the industry of power electronics ever since.

Although there were innovations and applications of many different types of power semiconductor technologies, such as MCT (MOS gate controlled Thyristor) and IGCT (Insulated Gate-commutated Thyristor), MOSFET and IGBT have been the most popular devices in the past three decades. Due to trade-offs among different characteristics of power transistors e.g. off-state voltage blocking capability, on-state current carrying ability, time needed for transitions between on and off state, etc. MOSFET is the dominating device in low power/voltage, high frequency applications like PFC (Power factor correction) and DPS (Distributed Power Systems); while IGBT reign in medium and high power/voltage, low frequency applications such as UPS (uninterruptable power supplies) and Photovoltaic (PV) inverters. After 30 years' successive technological innovations, characteristics of MOSFETs and IGBTs have improved dramatically and have entered into maturing stage. In fact, as manufacturing technologies has evolved to such advanced stage, physical limits of the traditionally used Silicon (Si) material, such as breakdown field and thermal conductivity, are being approached. Further performance improvements in one of the important characteristics may not practically possible without the degradation of the other(s). Take power MOSFETs that can be used in PFC boost converter (≥600V) as an example, the on-state resistance can be as low as 0.015 Ω in a 650V superjunction MOSFET with a package of so-called Max 247. This MOSFET, however, has a large input capacitance of 18.5 nF that leads to very slow switching speed [1-20]. On the other hand, several MOSEFT products with a maximum blocking voltage of up to 1.5kV are available from the market, among which the one with smallest on-state resistance is the product packaged in TO247 with a R_{dson} value of up to 1.8 Ω [1-21]. In addition, maximum junction temperature of today's Si MOSFETs is confined to 200 °C [1-22].

Attempts to develop Si transistors, especially the ESBT (Emitter-Switched Bipolar Transistor), that can stretch theoretical limits of the material had been performed. ESBT has a cascode configuration combining a high voltage, high current BJT and a low voltage, fast switching MOSFET, packaged either as a single monolithic chip or in a hybrid way [1-23]. The particular structure allows achievement of high voltage, small resistance and fast switching speed simultaneously. Today, maximum blocking voltage of commercial ESBT products is up to 1.7kV, packaged in TO247 with on-state resistance of 0.07 Ω [1-24]. The ESBTs, however, requires complex driving and control to achieve optimal functionality, resulting from the fact that the switching of both the BJT (the current of which affects not only the static but also dynamic behavior) and the MOSFET needs to be handled in an intelligent way [1-25]. In a PFC boost converter where the current through the transistor varies, for instance, a driving scheme of adjusting the voltage and current in the base of ESBT according to the instantaneous value of the

current is required [1-26]. Although there has been lots of efforts to provide suitable driving solutions, ESBT is not widely preferred in today's industrial applications [1-23] [1-26].

Wide bandgap (WBG) materials, such as Gallium Arsenide (GaAs), Silicon Carbide (SiC), Gallium Nitride (GaN), diamond, etc. offer significantly better electrical and thermal properties over Si. And thus, theoretically, performance of WBG power semiconductors would be superior to Si counterparts. Research on developing WBG devices has been going on for many years and focuses have gradually been given to SiC and GaN devices as they showed the best tradeoffs among material properties, commercial availability of starting material and relatively maturity of their technological processes [1-27]. Compared with Si technology, as illustrated in Figure 1.3, SiC and GaN semiconductors are capable of operating at higher temperature, higher voltage and higher frequency conditions [1-28] [1-30].

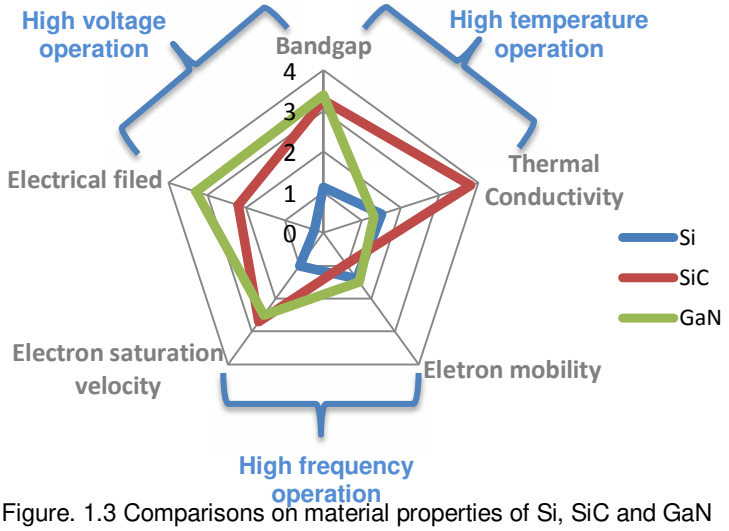


Figure. 1.3 Comparisons on material properties of Si, SiC and GaN

With recent availability of qualified products from multiple suppliers, discussions on SiC and GaN technology is shifting from theoretical analysis and speculations to practical solutions to best accommodate the devices in various applications. Currently, a variety of SiC products are available including MOSEFT, diode, JFET, IGBT, BJT, which are mostly tailored for high voltage (>900V), high power applications; GaN products, on the other hand, are also available in the form of different types of transistors and diodes. The major family of GaN transistors is high electron mobility transistors (HEMTs) and HEMT-derivatives, which are suitable for low voltage (<900V), high frequency applications [1-29]. Results from evaluations and applications of the emerging new devices showed that performances of traditional power electronics systems can be elevated in terms of efficiency, power density, etc. Moreover, WGB devices are also capable of initiating new applications that are beyond the reach of Si technology.

- **High efficiency** power converter prototypes were successfully implemented using GaN transistors [1-30] [1-31]. For instance, efficiency of a 300V/50V, 200W synchronous buck

converter operating at 500kHz can be pushed up to more than 92% in hard switching and over 99% in soft switching using a 600V, 0.25 Ω GaN transistors [1-32].

- **High power density** power electronics systems facilitated by GaN transistors have already been demonstrated [1-11] [1-34] [1-35]. Power density of a low voltage GaN HEMT based 12–1.2V POL (point of load) converter, for example, can be pushed up to 1100 W/in^3 when it operates at 5MHz with a maximum output current of 20A [1-11].
- **New applications** potentials of WBG transistors have been well promoted and, with availability of qualified products, realizations of the potentials can be expected [1-36]. It was predicted that with the availability of SiC or GaN devices, which have a high temperature operation ability up to 250 °C, a loosened requirement on heat exchanger of power electronics systems in space exploration is possible, which could lead to new design of the thrust engine suitable for deeper space missions [1-37] [1-38].

As performances of WBG devices do live up to expectations, with wider adoption of the devices i.e. increased production and decreased cost, they are believed to be able to replace Si devices and reshape the industry power electronics in near future [1-29].

1.1.3 Applications of GaN semiconductors in power electronics systems - Development trend of power electronics

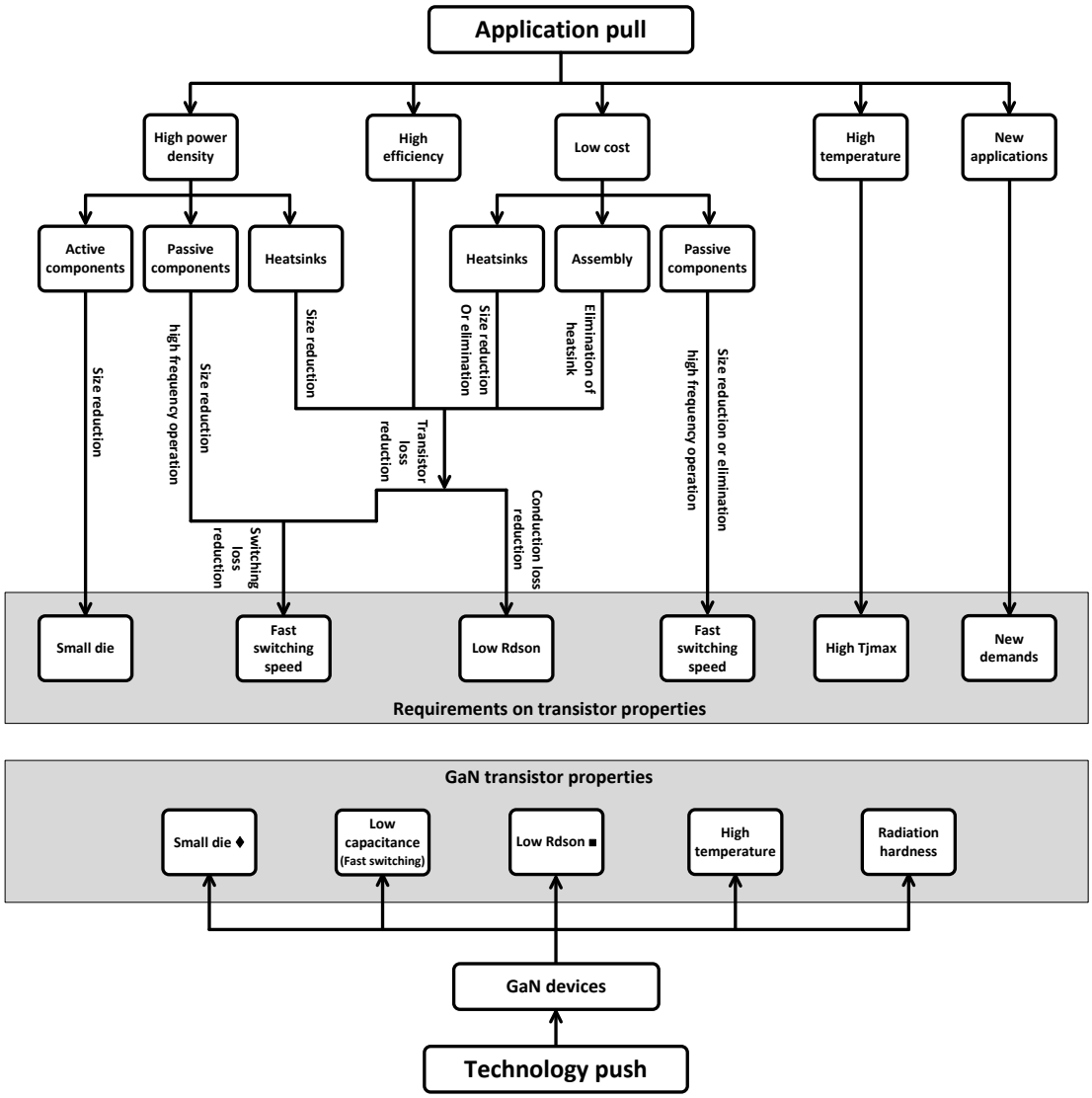
As the high efficiency, high power density and low cost requirements of power electronics systems can all be translated into the need of suitable power semiconductors for high frequency operation, with the advent of GaN devices that are superior to state-of-art Si devices in terms of switching speed, a trend of high frequency operation with GaN semiconductors to satisfy the demands is appearing. In fact, application of GaN devices in high frequency power electronics systems will bring benefits more than expected especially in hard switching systems, as illustrated in Figure 1.4.

GaN devices have much faster switching speed than Si counterparts, resulting in great switching loss reduction in many power electronics applications even at high frequencies. Material properties of GaN device also promise lower on-resistance of the device compared with Si counterparts with the same voltage blocking capability and die size, leading to reduced conduction loss in the device. Size as well as cost reduction of both passive components and heatsinks can be achieved simultaneously by pushing up operation frequency while having low loss in switching devices. Besides, when GaN operates at sufficient high frequencies that permit the usage of air core magnetics or/and when losses in GaN is low that elimination of heatsinks is possible, assembly cost can also be reduced. Furthermore, when the same voltage and on resistance characteristics are maintained, GaN devices would need much smaller die (and smaller package) than corresponding Si devices. And thus, the effect of GaN device on system

miniaturization starts already from size reduction of the component itself. Moreover, in GaN products, a thin GaN epi-layer usually grows on a Si substrate and the manufacturing process is compatible with conventional fabrication equipment for Si devices [1-39]. Given the fact that GaN device requires smaller die size than Si device with similar ratings, GaN products may even be cheaper than Si products in future.

GaN devices are, in theory, capable of surviving high temperature operations thanks to low intrinsic carrier concentrations of the material, which will not affect carrier conductivity and functioning of the devices thereof up to 600°C [1-40]. At this moment, maximum junction temperature of GaN products is confined to 175 °C, limited mainly by a lack of suitable packaging technologies [1-41] [1-42]. Research on developing better packaging techniques for both discrete GaN devices and GaN power modules has already started and noticeable progress has been made recently. The X-6 low-profile package from APEI, for example, is developed to accommodate discrete GaN HEMT up to 225°C [1-43]. With more advanced packaging technology, wider temperature span of GaN devices can be expected. As no high temperature GaN product is commercially available, with which the potentials of GaN devices could have been explored in this thesis, the high temperature capability of GaN devices is not considered in this work.

GaN devices also hold the potentials for enabling new applications. Although emerging GaN products already perform better than Si counterparts in measures of efficiency and power density, more advanced characteristics as promised by basic material properties can be expected from future GaN devices. For instance, most GaN transistors available now are heterojunction devices in lateral structure as they grow on non-GaN substrates like Si, SiC and Sapphire. And therefore, the transistors are regarded as low voltage devices. In fact, high voltage GaN transistors of both lateral structure and vertical structure are appearing: a 1700V cascode-configured GaN-on-Si HEMT was reported by Transphorm while a 1200V enhancement mode vertical JFET was already developed by Avogy [1-29] [1-44]. With performance of GaN devices be promoted further, various new applications which are beyond the capabilities of Si devices could be enabled. Among many others, wireless power transfer, RF envelope tracking, rad-hard satellite and avionics power supplies are some of the predicted applications that will be initiated by GaN devices. Wireless power transmission and RF envelope tracking systems utilizes a blend of high-frequency operation with high-power and high-voltage capabilities. Power systems for satellite and avionics applications, on the other hand, take advantage of GaN transistors' high frequency, high temperature capabilities as well as the ability to operate in high radiation conditions [1-45].



■ For the same blocking voltage and die size

◆ For the same blocking voltage and on-resistance

Figure 1.4. Trend of high frequency operation with GaN devices

1.2 Problem description

Losses in GaN devices and the effects of parasitics on losses

Emerging GaN semiconductors, judging from their wide bandgap material properties, are good candidates to replace Si devices and enable power converter to operate at increased switching frequencies. In theory, GaN devices have much improved FOM (Figure-of-Merit) than Si counterparts, and thus the new devices have the potential of boosting the performances of existing power electronics systems and sparking new applications [1-10] [1-45]. Characteristics of

actual GaN devices, however, are determined by more than just the properties of the material. Issues such as die design and fabrication approach, device packaging technology, the way they are used in circuits etc., also contribute to what GaN transistors can achieve, especially in high switching frequency applications [1-35] [1-46]. Available low voltage GaN transistors come with extremely small die size and package compared to Si MOSEFT with similar electric ratings [1-45]; while newly developed high voltage GaN transistors have comparable die size and package as Si counterparts with the same ratings [1-32] [1-48]. And thus, for the purpose of exploring potentials of GaN devices, it is essential to evaluate and analyze losses in the devices to reveal benefits and limitations of applying them in high frequency power converters.

It is a natural approach to execute loss assessments of GaN transistors in existing power converters where the transistors are used as direct replacement of Si MOSFETs. As GaN devices have high current slew rate (di/dt) during switching transients, high voltage drop across parasitic inductances will occur in a fixed converter setup. And therefore, in addition to the characterization of package parasitics, the electromagnetic environment surrounding the transistors i.e. circuit parasitic elements also have to be defined and specified. In particular, the electromagnetic volume of low voltage GaN transistor is negligible compared to the rest parts of the power converter circuit, the environment has profound influence on switching characteristics and losses of the transistor and must be well accounted for [1-10].

Optimal usage of GaN transistors and limitations in high frequency applications

Optimal usage of GaN devices, however, may not be achieved if they are used simply as a drop-in replacement of Si devices in existing power converters. The available converter architectures are mostly designed to suit Si devices, and whether full benefits of GaN transistors can be achieved in these concepts are questionable. To fully exploit the potentials of GaN devices for high frequency operations and, more importantly, to find applications in which benefits of GaN devices could be maximized, optimal topologies and operation modes that accommodate GaN transistors best needs to be identified. Moreover, challenges and design trade-offs other than suitable topologies and operation modes also presents in a GaN converter, such as thermal management, voltage stress, etc. Heat removal approach for GaN devices, especially for low voltage GaN HEMTs, could be challenging as the new devices have different packaging technologies, electrical and thermal properties, etc. compared to Si devices. Thermal management approach taken should be an optimal solution, as a trade-off exists between thermal management and high frequency performance in a GaN converter [1-10]. To successfully take advantage of GaN technology, the GaN based power electronics system as a whole needs to be optimized. Besides, limitations of the optimal conditions in which GaN transistors will be applied needs to be clarified to guide proper design and implementation of GaN based applications.

1.3 Thesis objectives

With the purpose of overcoming challenges introduced in Section 1.2, the main goal of this thesis is to *explore potentials of GaN devices for high frequency applications*. Objectives of the thesis, accordingly, can be summarized as:

I. Investigate limitations of GaN devices for high frequency applications

As performance of emerging GaN transistors is unknown, evaluation of their capabilities in certain applications, PFC converters in this work, needs to be carried out. The evaluation should reveal how GaN devices perform in existing systems where they are used directly as replacement of Si devices; whether they can outperform Si counterparts in existing systems; what kind of benefits the new technology brings compared to Si devices in these systems; what are the influences of circuit and package parasitic elements on performance of GaN devices (issues, such as circuit/package parasitic inductances, that hinder realization of fast switching and problems, like device parasitic capacitance, that affects suitable switching conditions); what are the limitations in applying GaN transistors in high frequency operations.

II. Explore topologies and operation modes that accommodate GaN devices and clarify limitations of the topologies and modes for high frequency operations

To fully explore the potentials of GaN devices, optimal topologies and operation modes where benefits of GaN technology can be fully exploited should be identified. The optimal topologies and operation modes, which could be widely-adopted conventional schemes, unpopular existing systems or even new technologies, should overcome or even take advantage of the spotted limitations. For instance, in active PFC solutions, traditionally a boost converter, mainly because of its simplicity, is popular rather than choices like buck-boost, Sepic, etc. Whether the boost will remain the preferred solution or one of the alternative circuits will be made more attractive with the advent of GaN devices needs to be verified. Furthermore, new PFC topologies might even be needed when all the existing options fails to well accommodate GaN devices. In addition, new challenges, design trade-offs and limitations that arise when applying GaN devices in the identified topologies and operation modes should be taken care of.

III. Demonstrate benefits of GaN technology in high frequency power conversion applications

Demonstration on benefits of GaN technology in real applications, PFC converter in this thesis, should be conducted. Optimal usage of GaN devices in an application that

embodies both optimal topology and operation mode so as to maximize the benefits of the devices should be carried out as a case study.

1.4 Thesis layout

Chapter 2 presents an overview on GaN devices and converters. Both the evolution of different types of GaN semiconductors and performance of converters employing the newly appeared devices will be reviewed. Special attention will be paid to two different kinds of GaN transistors, low voltage GaN HEMT (High Electron Mobility Transistor) and High voltage GaN GIT (Gate Injection Transistor), and their applications in converters. The goal of this chapter is to demonstrate the potential of GaN technology on development of power electronics from the perspective of technology push.

Chapter 3 covers developments of PFC converters and investigation of preferred topology for pushing up frequency of the PFC stage. The concept of PFC technique and approaches to realize the technique is introduced first. Possible topologies such as boost, buck, buck-boost, etc. to implement PFC are then compared and summarized with both their advantages and disadvantages. An investigation on whether pushing up operation frequency will make one or more topologies better options for PFC than traditionally used boost converter i.e. whether GaN devices could combat the disadvantages while retaining or even enhancing their advantages of these topologies is carried out afterwards. After the confirmation that boost converter will remain as a preferred choice for implementing high frequency PFC, it is chosen as the platform for evaluating and demonstrating potentials and benefits of GaN devices. The purpose of this chapter is to illustrate application pull of current and future power electronics systems using PFC converters as an example.

Chapter 4 performs loss modeling and analysis of GaN devices in a high frequency boost converter. With the assistance of a generalized equivalent circuit which is derived based on their physical structures and basic operation principles of low voltage GaN HEMT and high voltage GIT, analytical loss model of GaN devices that accounts for influences of circuit and package parasitics, is developed. The model is employed to analyze losses in both GaN HEMT and GaN GIT and to disclose the critical parasitic elements in a GaN boost converter in CCM (Continuous Conduction Mode). The goal of this chapter is to uncover the benefits and limitations of GaN devices in high frequency operation when the devices are simply used as a drop-in replacement of Si device in existing power electronics systems, using hard-switched boost converter as a platform.

Chapter 5 explores optimal operation modes and the limitations of the modes in a PFC converter that can suit GaN device best so that full advantage of GaN can be taken of. Losses in GaN transistors in CCM are analyzed firstly through the help of loss model developed in chapter 4 to

expose desirable switching and conduction conditions of the devices for high frequency operation. Exploration on approaches to accommodate GaN devices with the desired conditions are then carried out, starting with a study on possible operation modes of a PFC boost converter, which, in essence, provides different switching and conduction conditions. It is revealed that the conventionally used BCM-VS in PFC boost converter is an ideal application for GaN devices from loss point of view as the mode naturally enables most of application conditions that GaN devices desires. Further loss reduction approaches in BCM-VS, on both switching loss and conduction, is introduced. Experimental results proved and demonstrated the analysis. Besides, the limitations of applying GaN devices BCM-VS are clarified. This chapter aims to identify optimal utilization conditions where benefits of GaN technology can be fully exploited and combat new challenges that come along.

Chapter 6 presents design and optimization approach of a PFC boost converter using GaN GIT. Loss modeling and design of a PFC boost converter are performed. Optimization of the converter is conducted to minimize total loss and thus achieve high conversion efficiency. An experimental demonstrator is built, the results of which are summarized and analyzed. This chapter demonstrates benefits of GaN technology in real applications, using PFC boost converter as a case study.

Chapter 7 concludes this thesis and discusses recommendations derived from the results of this thesis for future research.

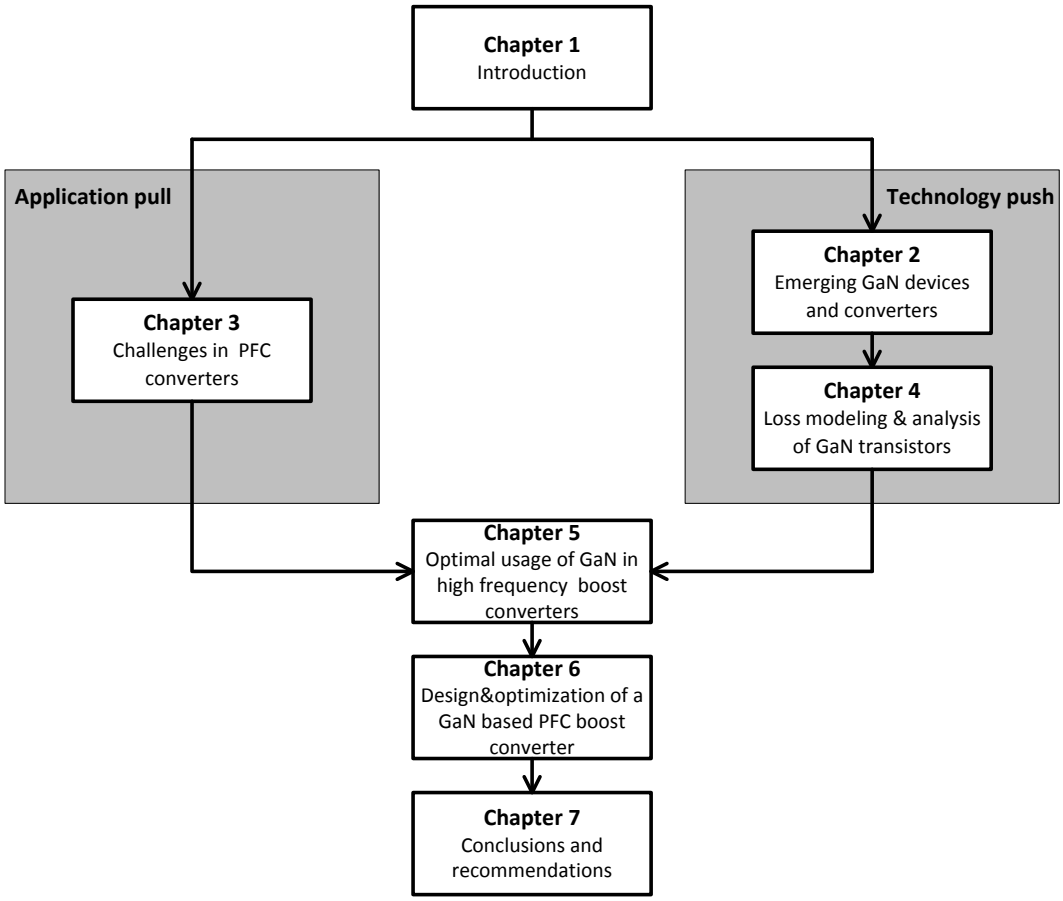


Figure 1.5 Thesis layout

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Chapter 2. Overview of GaN Devices and Converters

2.1 Introduction

It is well acknowledged that advances in power semiconductor technology has consistently been a major force in pushing developments of power electronics technology, although innovations in topologies, control schemes, design of passive components, packaging techniques, etc. also contribute [2-1]-[2-3]. In fact, being a mature and well-established material, the pushes are achieved by Si technology in the vast majority of applications. Through successive improvements and optimization since the late 1950s, the maturity of Si devices has reached such a stage that physical limits of the technology e.g. voltage blocking capability, maximum operation temperature and conduction and switching characteristics, etc. are becoming reached [2-4] [2-5]. The unavoidable physical limits prohibit performances of power converters like efficiency, power density, etc. from be further improved and calls for solutions. Attempts to stretch the theoretical limits through proposals such as ESBT, super-junction, etc. gained limited examples as they are accompanied by substantial extra cost and inconvenience in usage and a more straightforward concept, using a better semiconductor material, is gaining more and more popularity [2-6].

Wide bandgap (WBG) materials generally have greatly improved material properties than Si and among many others, SiC and GaN are promoted as the most promising candidates because they show best trade-off among theoretical characteristics, real commercial availability of the starting material and maturity of their technological processes [2-7]-[2-9]. To date, focuses on semiconductors made from SiC and GaN has shifted from whether the components are realistic or not to practical solutions to problems encountered in manufacturing process and how they should be optimally implemented in various power electronics applications [2-10]-[2-12]. Accordingly, more and more GaN and SiC devices are commercially available and used in power converters.

In this chapter, with the motivation to examine potentials of GaN technology in pushing the development of power electronics converters, attention will be paid to GaN devices and converters to get an overview over status of GaN devices and their applications in power converters. Material properties of GaN their implications of performances of potential GaN devices are promoted firstly in 2.2. State-of-art GaN devices is to be reviewed and summarized in 2.3, with the emphasize on lateral GaN transistors of normally-off mode. Converters using commercialized single-die GaN transistors are then surveyed in 2.4, after which issues with available GaN devices and converter design challenges are highlighted in 2.5. A summary on current status and further development trend of GaN and GaN converters is then given in 2.6.

2.2 GaN material properties and device potentials

The band gap (BG) of a semiconductor material reflects strength of chemical bonds between atoms in lattice and the larger the band gap the stronger the bonds [2-13]. Stronger bonds bring about more stable lattice structure i.e. the material is less susceptible to various mechanisms e.g. electrical ionization, thermal decomposition, etc. that would cause changes of its physical properties and, theoretically, better power semiconductor can be expected in measures of electrical behaviours, thermal performances, etc. Wide band gap (WBG) materials, in general, are the ones having larger band gap than Si, the material currently being used in vast majority of applications [2-14]. Among many others like diamond, Aluminium Nitride (AlN), etc., SiC and GaN are considered as the most promising WBG materials as they show best trade-off among theoretical characteristics (e.g. maximum achievable blocking voltage, operation temperature, etc.), real commercial availability of the starting material (e.g. wafers and epitaxial layers) and maturity of their technological processes [2-7] [2-8]. As listed in Table 2-1, key material properties of GaN and SiC are superior to that of Si and GaN also excels SiC in almost all cases. Between the two, determined mainly by the basic material properties, GaN power devices are more suited for high frequency power conversions while SiC power semiconductors are believed more suitable for high power applications [2-15] [2-16]. In this thesis, the background of which is about consumer electronics, attention will be paid only to GaN and SiC will not be discussed.

The much better material properties of GaN over Si would, in theory, result in GaN power devices with significantly improved static characteristics and dynamic behaviours than their Si counterparts and, in the end, exceed the reach of Si technology in performance in power electronics applications.

- Resulting from the WBG nature, impact ionization will not happen until a much higher electrical field (termed as critical field, E_{crit}) is imposed onto GaN and thus higher breakdown voltages (V_{BR}) of GaN devices are made possible. As indicated by the relationship between breakdown voltage in (2.1), critical field and length of drift region (w_{drift}), with the same lengths of drift regions which is the major part of device thickness, GaN would have more than ten times V_{BR} than a Si device. Moreover, in order to build such critical field in a short drift region, high doping of the region is needed, which means that higher concentration of electrons in the drift zone and, consequentially, lower on-state resistance in a unipolar device. As a matter of fact, with comparable die sizes, on-state resistance of a GaN device could be about one-fifteenth of that in a Si one as implied in (2.2) where ε_0 and ε_r stands for the permittivity of vacuum and relative permeability of a material, respectively. And thus, high breakdown voltage and low on-state resistance could be achieved simultaneously in GaN devices, which makes them

more suitable for high voltage operations. It's worth to be pointed out that the higher electron mobility property of GaN also contributes to the reduction of R_{on}.

$$V_{BR} = \frac{1}{2} \cdot E_{crit} \cdot w_{drift} \tag{2.1}$$

$$R_{on} = \frac{w_{drift}^2}{\varepsilon_0 \cdot \varepsilon_r \cdot \mu_n \cdot E_{crit}} = \frac{4 \cdot V_{BR}^2}{\varepsilon_0 \cdot \varepsilon_r \cdot \mu_n \cdot E_{crit}^3} \tag{2.2}$$

- The higher critical field also promises thinner drift region. For the same voltage blocking capacity, length of drift region can be more than 10 times shorter than that of a Si and thus the device could be ten times smaller while, at the meantime, on-resistance more than 3000 times lower. And thus, smaller size of GaN devices can be obtained while voltage blocking and current carrying capabilities of the devices are at least as good as that of Si ones.
- Ideally, the shrinking of chip size would lead to reductions of parasitic capacitances (C_{gs}, C_{gd} and C_{ds}) and, together with the higher electron saturation velocity caused by the nature of WBG, enable increased switching speed of GaN devices. And, consequentially, GaN power devices could be used for high frequency applications.
- GaN material, because of its WBG nature, inherently have lower intrinsic carrier concentration than Si. So, a GaN die would have more thermal headroom before it is overwhelmed with thermally generated carriers, resulting in a GaN device with increased maximum junction temperature and, when package also allows, making the GaN device suitable for high temperature operation. GaN devices are, in theory, capable of surviving high temperature up to 600°C if packages of the devices also permit [2-17].

Table 2-1 Material properties of Si, SiC and GaN [2-13] [2-18]

Parameter	Si	SiC	GaN
Band Gap E_g (eV)	1.12	3.26	3.39
Critical Field E_{crit} (MV/cm)	0.23	2.2	3.3
Intrinsic carrier density n_i (cm^{-3})	$1 \cdot 10^{10}$	$1 \cdot 10^{-9}$	$2 \cdot 10^{-10}$
Saturated drift Velocity V_s (10^7cm/s)	1.0	2.0	2.5
Electron Mobility μ_n ($cm^2/V \cdot s$)	1500	650	990/2000*
Relative permittivity ε_r	11.8	9.7	9

* Difference between bulk and 2DEG

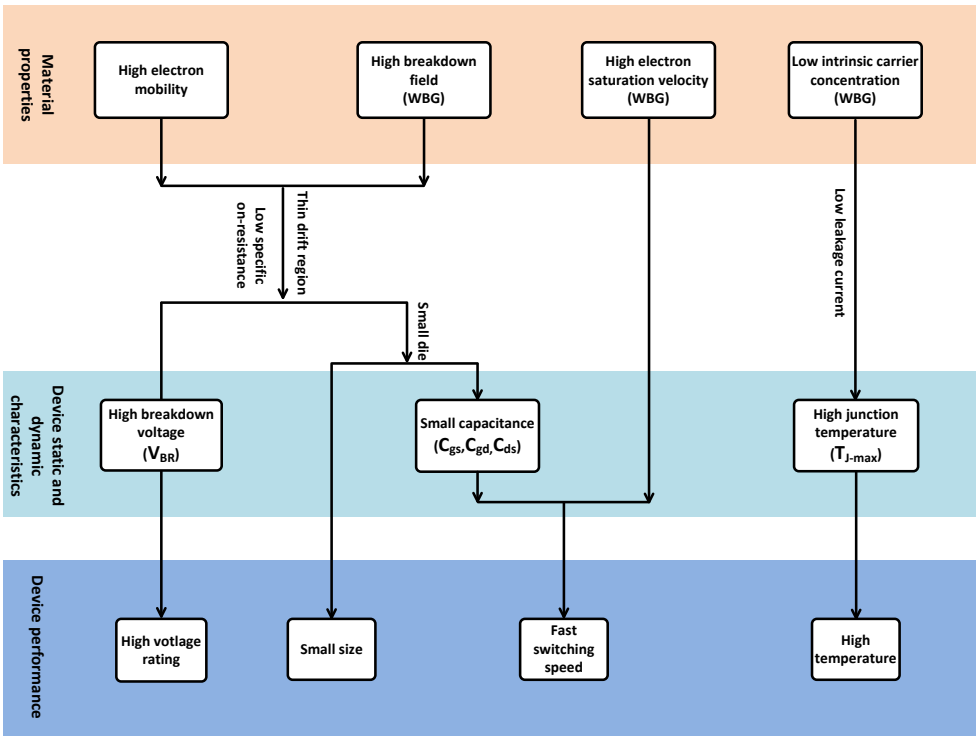


Figure 2.1 GaN material properties and resulting potentials of GaN devices

To summarize, as illustrated in Figure 1, superior material properties of GaN could theoretically be translate into better static characteristics and dynamic behaviours of GaN devices, which would ideally make them capable of working in high voltage, high temperature and high frequency applications. Besides, smaller size could also be achieved. It should be noted that there are also other performances of GaN devices like radiation hardness, low-cost, etc. that also root from basic material properties, which are well described in [2-13] [2-19] [2-20] but are beyond the scope of this work.

2.3 Emerging GaN transistors

2.3.1 Introduction

To take advantage of the promising properties of GaN material, great efforts have been put to design and fabrication of GaN power devices that could translate the promises into reality. It was reported that 11 of the 23 main producers of transistors have research programme on GaN and, at the same time, there are also many newcomers in the field of semiconductors focusing on GaN development [2-11] [2-15]. Emerging GaN devices from these manufacturers are mostly in their first stage of development and material advantages have not been fully exploited yet because of problems such as specific material quality, technology limitations, non-optimized device designs and reliability issues, etc. [2-9]. Nevertheless, with the newly introduced GaN devices, which show diversity in starting materials, basic structures, gate formation approaches, etc., patterns

exist regarding benefits and drawbacks of the devices. And accordingly, remaining challenges to overcome and general trends for future developments of the new technology can be identified.

The developed GaN devices, the majority of which are discrete components rather than modules, can be broadly grouped as vertical ones and lateral ones, according to current flow paths determined by their basic structures. Of the two types, vertical GaN semiconductors are believed having brighter prospects as the growth on bulk GaN layer would allow homo-epitaxy that is exempt from issues like mismatch in lattice structures and thermal expansion characteristics between epi-layer and substrate and thus leading to the best epi-layer quality [2-12] [2-18]. However, due to the lack of high quality, low cost GaN wafers, very limited progress has been made on vertical GaN devices. It was reported in [2-21] that a 1.5kV/2.3A GaN-on-GaN transistor was developed. This high voltage vertical GaN FET, however, has a low threshold voltage of 0.5V and thus is sensitive to noise and prone to unwanted turn-on. Besides, a 1.2kV GaN-on-GaN e-mode JFET was seen from news-release of Avago, but further results have not been published since then. There have also been efforts to fabricate vertical GaN devices on Si substrates e.g. by etching through the Si substrate and buffer layers on the bottom side of the device to expose the GaN drift region of a heteroepitaxial GaN-on-Si structure and putting the drain in direct contact with the GaN layer, a GaN-on-Si FET can be fabricated [2-12]. Four GaN FETs have been successfully developed with this so called “substrate-removal” technique, with the maximum voltage of the FETs up to 650V [2-18].

On the other hand, the shortage of high quality, low cost GaN layers stimulates efforts being devoted to investigation of growing GaN device on non-GaN substrates and, as a consequence, lateral GaN device that are grown on foreign substrates dominates, which is also the focus of this work.

It should be pointed out that plasma GaN devices e.g. p-n diodes, bipolar FETs, thyristors, etc. are not practically useful as: a). GaN p-n diodes and thyristors naturally have higher forward voltage drop than Si and SiC competitors; b). being a direct semiconductor, in which carrier lifetimes are extremely short and not sufficient for plasma operation [2-1] [2-18]. Investigation on fabrication of GaN Schottky diodes have also been conducted, but with limited progress [2-15] [2-22]. Consequentially, in this thesis, focus will be exclusively given to lateral GaN transistors.

2.3.2 Lateral GaN transistors

Lateral GaN devices, especially the commercialized ones, are HEMTs and HEMT derivatives that take advantage of carriers formed by a heterojunction of AlGaN/GaN. The initiation of electrons stimulated by the bandgap difference between AlGaN and GaN and the augment of the formation by both spontaneous and piezoelectric polarization cause a sheet of high density, high mobility carriers, usually termed as two-dimensional electron gas (2DEG), to be confined at the interface [2-10]. This highly conductive 2DEG is the fundamental property of lateral GaN devices and the

root of differences from Si counterparts. As illustrated by the basic structure of lateral devices in Figure 2.2, a native channel between drain and source is formed and lateral GaN HEMTs are, by nature, depletion-mode (normally-on) devices.

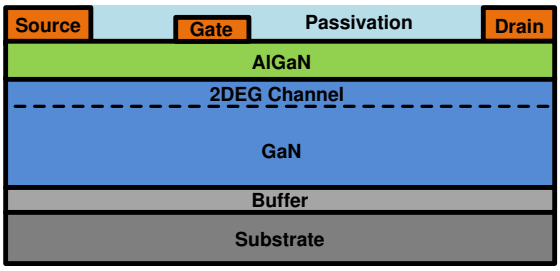


Figure 2.2. Basic structure of lateral GaN transistors

Up to date, GaN HEMTs have been fabricated on substrates of Si, SiC and sapphire [2-23] [2-24]. Buffer layers are usually adopted to provide strain relief and minimize the mismatch between the GaN layer and the foreign substrate [2-13] [2-18]. As Si is considerably cheaper than alternatives, most efforts are therefore devoted to fabricating cost-effective GaN HEMTs on Si [2-11] [2-13]. With the GaN-on-Si HEMTs, focus of innovations is mainly put on how to make the devices as enhancement-mode (normally-off) since normally-on devices are less desirable in power converters due to safety and complicity concerns [2-13] [2-25]. In fact, there do exist normally-on GaN HEMTs e.g. 650V transistor from VisIC, early version of GaN FET from IR, etc., but the devices have received limited popularity. So far, the approaches succeeded in creating normally-off GaN HEMTs can be broadly categorized into two groups: through modification of gate structure in a single-die GaN HEMT and through co-packaging of a normally-on GaN HEMT with other electronic parts.

Modification of gate structure of an inherently depletion-mode GaN HEMT basically are actions of modifying gate structure to deplete the 2DEG underneath the gate structure, effectively lift threshold up to a positive voltage resulting in a normally-off device. Various kinds of gate-modification techniques have been proposed and, according to the consequential actions with the AlGaN/GaN structure beneath gate i.e. keep both layers intact, modifying of AlGaN layer with recess or plasma injection, full removal of AlGaN, the techniques can be grouped as follows:

- *Formation of a gate-channel junction* between gate and the 2DEG channel is the most popular approach to convert a depletion-mode GaN HEMT into a normally-off one, especially with the commercialized ones. By depositing p-type GaN or AlGaN beneath the gate, a p-n junction is formed, depleting the 2DEG in the channel underneath the gate and thus lifting up the potential between gate and channel.

- *P-GaN gate* cap has been successfully used by many in making depletion-mode GaN HEMTs with threshold voltage well above 1V, among which the highest voltage achieved is up to 650V [2-25]-[2-27].
- *P-AlGaN* deposition has also been deployed by several manufactures to fulfill the desire of normally-off GaN device [2-28] [2-29]. In particular, the Gate Injection Transistor (GIT) with p-AlGaN gate from Panasonic is well commercialized and, when it comes to its performance, is reported to have the highest breakdown voltage of 600V as well as the best temperature performance on variation of on-state resistance and transconductance over temperature, although, limited by packaging technologies, the maximum operational temperature of the device is just as good as Si counterparts (150^{o}C).
- *Schottky gate-channel structure* that employs a gate metal over the channel to form a metal-semiconductor junction was used in the early version of the first market-available GaN HEMTs from EPC. Testing and application of GaN HEMTs from EPC are, by far, the most intensively reported, the result of which show that the devices are subjected to low voltage (up to 300V) and thermal performance is not close to the promise of GaN material (Maximum junction temperature is confined to 150^{o}C)

The diode-like gate structures that this group of GaN HEMTs are made from, together with the material properties, bring about unique gate characteristics. Theoretically, the gate-channel diode, may it be either a p-n or a Schottky, would conduct once the gate-channel voltage difference exceeds forward build-in potential of the corresponding junction barrier. The resulting current would inject holes from gate to the 2DEG channel, inducing the same number of electrons in the channel and thereby decreasing on-state resistance.

- *Recessed gate structure*, as was promoted in [2-30], transfers a native depletion mode GaN HEMT into enhancement mode by thinning the AlGaN layer underneath the gate so as to reduce the piezoelectric field at the interface of AlGaN/GaN right below the gate and, as a result, shift gate threshold voltage to a positive value. This method was used in practice by Sanken in making an 800V normally-off GaN HEMT and, resulting from the need of recessing the AlGaN to a precise depth to keep the 2DEG layer intact, a threshold voltage of 0.8V is achieved, which is low and make the device prone to accidental turn-on when used in circuits. It was reported that GaN HEMTs made by HRL introduced a layer of insulator to the recessed region and thus managed to elevate the threshold voltage of more than 1V in a 600V transistor [2-31]. Up to date, GaN HEMTs

with recessed gate has not been launched to the market yet and properties like thermal performance are unknown.

- *Plasma treated gate* technique uses plasma treatment to implant negative charges into the AlGaN layer at the gate of a depletion mode GaN HEMT, effectively depleting the 2DEG underneath. A Schottky gate can then be formed in the plasma treated region of the GaN HEMT and the 2DEG channel will be reformed when sufficient positive voltage is applied [2-32]. The gate can also be made as insulated to prevent gate current flow and minimize gate and driving loss by placing an insulator between the plasma treated region and the gate e.g. AlN used in GaN HEMTs from HRL [2-33]. The developed GaN HEMT with plasma treated gate has achieved a blocking voltage as high as 1.2 kV. The threshold voltage, however, is as low as 0.64V which is not desirable for practical applications. As a result, GaN HEMTs with plasma-treated gates requires further developments before practically used in industry.
- Hybrid GaN HEMT are the ones in which recess of the gate is deep enough that the AlGaN layer below gate is completely etched and the 2DEG beneath is permanently removed while it remains on the drain-side and source-side. A typical MOSFET inversion layer is needed to connect the two sides, leads to a hybrid MOS-HEMT that combines convention gate structure in a Si MOSFET and high density, high mobility of 2DEG. MOS-HEMTs, in some cases termed as MIS-HEMTs, as demonstrated in [2-34]-[2-38] generally show higher voltage blocking capacity (up to 1.7kV), but the devices generally suffers from high on-state resistance. Besides, stability of the devices is a major concern as, attribute to the electrons trapped in the new interface between gate dielectric and GaN, threshold voltages are subjected to significant negative shift over temperature [2-38]. And therefore, the devices are not ready for consumer market.

Co-packaging a depletion-mode GaN HEMT with other electronic parts could also end up with a normally-off GaN device. Under this scenario, the challenge of making a normally-off device is shifted from fabricating suitable gate structures on the GaN HEMT itself to designing of auxiliary circuitries to be connected and integrated with the GaN HEMT. There are, in fact, broadly two kinds of such devices: the ones that are designed specifically to produce a normally-off GaN device and the ones that are developed for other purposes with a normally-off GaN device as a by-product.

- *Incorporating an enhancement-mode, low voltage Si MOSFET with a depletion-mode high voltage GaN HEMT with cascode configuration* is an approach adopted by many e.g. MicroGaN, Transphorm, Infineon, etc. to achieve normally-off GaN devices, of which 650V devices with a maximum junction temperature of 150^{o}C from Transphorm is market-available. In the cascode configuration, the Si MOSFET controls on/off state of

the GaN device as its output clamps the gate input of the GaN HFET, making the device normally-off. The two semiconductor dies share the same channel current while on and the blocking voltage distributes between them in off-state. Cascode GaN devices inherit the gate features of Si MOSFET including rugged structure, high threshold voltage, etc. Besides, driving is made easy as conventional gate drivers for Si MOSFET can be used. The devices, however, are subjected to influences of parasitics: a) package and inter-connection induced parasitic inductance tends to be high, causing high switching loss [2-39]; b) interaction between the two devices may result in instability due to large package parasitic inductances [2-40]; c) mismatch of parasitic capacitance between the two dies may induce undesired features like avalanche of the Si MOSFET [2-41].

- *Integrating GaN HEMT with electronic parts* such as gate driver, control circuitry, etc., is also a way of producing normally-off GaN devices. In fact, in most cases, the motivation of such kind of integration is more about concerns like minimization of parasitics, reduction of cost, etc., under the scenario of accomplishing system in package (SiP). A 600V/12A normally-off GaN power stage that co-packs a depletion-mode GaN HEMT and a gate driver is developed by TI. This device, as reported in [2-42], also includes protection circuits to make it immune from over voltage, current and temperature. A similar concept could also be found in the 650V/50A GaN device from VisIC, in which a normally-on GaN HEMT is integrated with a control block, enabling normally-off operation [2-43]. At this moment, this type of GaN devices are not ready for purchase.

It should be noted that, apart from the commonly seen type of GaN devices as introduced, there are also other reported variations such as four-terminal bidirectional GaN transistor [2-44], double heterojunction field effect transistor (DHFET) [2-45], etc. These variations are only reported in literature and has not been manufactured yet. Besides, with some of the newly introduced normally-off AlGaN/GaN based GaN devices, which are reported as promising products, detailed structures of the device have not been published and therefore not accounted at this moment. For example, it was mentioned in [2-11] that a 650V normally-off GaN HEMT with insulated gate structure was developed by GaN systems. However, there's no publication describing the technique adopted to achieve normally-off operation.

It is worth highlighting the facts that in the developed normally-off GaN devices, especially the market-available ones (single die GIT with p-AlGaN gate, single-die HEMT with Schottky gate and cascode HEMT), high temperature operation capacity and high blocking voltage ability have not been achieved:

- Due to the limitations in packaging techniques, maximum junction temperature is limited to 150^{o}C in commercialized GaN devices, which is just as good as Si counterparts and far from the theoretical thermal limit of GaN material [2-46] [2-47].

- Resulting from the nature of the lateral structure, GaN devices are all low-voltage ones, with the highest blocking voltage of 650V in cascode GaN HEMT.

And therefore, at this moment, material advantages of GaN have not been fully exploited in terms of high blocking voltage and high temperature operation capacities due to issues such as technological process limitations, non-optimized device designs, etc. This is also a natural course as development of GaN semiconductors is still in early stage and, as a comparison, it took more than 30 years before theoretical limits of Si material is approached by Si MOSFETs [2-13]. In fact, research on advanced packaging methods and approaches to make high voltage GaN transistor has already started to improve thermal and voltage-blocking capability of GaN products, respectively. For instance, a novel package has been innovated to enable GaN HEMT operate up to 225°C [2-47]. Besides, high voltage cascode GaN HEMTs up to 1.7kV have also been successfully made, as reported in [2-15].

To summarize, with lateral GaN devices, HEMTs that take advantage of high density, high mobility 2DEG in a AlGaN/GaN heterojunction are the most commonly developed. A GaN HEMT, however, is natively normally-on and great efforts have been devoted to converting it into a normally-off one. Accordingly, various techniques from different manufactures have been proposed, resulting in a diversity of GaN devices that have already been reported or even commercialized. Basically, the devices are of two types: the ones that with modification on the gate structures of the GaN HEMT dies and the ones that keep die of GaN HEMT intact and utilize other electronic parts to generate a normally off device. Far from what is promised by the material properties, high temperature and high voltage capacities are not seen in GaN HEMT yet, particularly with the commercialized ones. In this thesis, which is about exploration of potentials of GaN technology with market-available GaN products, focus will therefore be given exclusively to exploiting high frequency operation potential of GaN.

2.4 High frequency GaN converters

Testing and proving of the fast switching capabilities of market-available GaN transistors has already been performed in Double-Pulse-Tester (DPT) or/and resistive switching setups that could minimize or even eliminate circuit parasitic elements and thus showing switching speed of the transistors [2-48] [2-49]. The results indicated that GaN devices do live up to the expectation of fast switching speed which is promised by material properties: a 200V single-die GaN HEMT exhibited voltage and current slew rates of 18.1V/ns and 5A/ns, respectively in [2-50]; in [2-49], a 600V GIT showed switching ability of ~50A/ns and 2A/ns and both turn-on and turn-off transients of a 600V cascode GaN HEMT are measured in [2-2] as less than 10ns when it is switched with 400V/10A.

So far, usage of the commercially available GaN transistors in real power converters has been carried out by many, especially with the single-die GaN HEMT from EPC and the cascode GaN HEMT from Transphorm as they appeared earlier than GaN GIT in various kinds of existing applications such as POL, wireless power transfer, PFC, motor drives, etc. [2-51]-[2-55]. In these converters, in most cases, the new GaN transistors are simply used as direct replacement of traditional Si transistors. Although there are improvements, since the converters are designed mainly to suit Si devices, the direct substitution i.e. the disregard of switching behaviours and loss characteristics of GaN transistors prohibit performances of the converters e.g. efficiency, power density, etc. from being drastically elevated. Performance improvements of the converters are, in general, limited as GaN devices are not optimally used according to their desired switching conditions.

In this section, from a perspective of investigating the possibility of pushing the development of power converters with the new technology, DC-DC converters with single-die GaN HEMT and GaN GIT will be reviewed to examine their high frequency performance over Si competitors. It should be noted that performance of converters with cascode GaN HEMTs is not presented as cascode GaN transistors are less cost-effective but more complicated in packaging compared to single-die GaN HEMTs and therefore is believed as a transitional solution at the beginning stage of GaN commercialization [2-25].

2.4.1 Single-die GaN HEMT based high frequency converters

The first single-die GaN HEMT has been available from market from 2009 and since then the devices have been adopted in diverse power converters. Being in the first stage of adoption, focus of these converters is mainly given to the consequential effects of loss reduction in switching devices or efficiency enhancements by directly replacing Si MOSFETs with GaN HEMTs. Besides, there are also examples on increasing power density of a converter with the new technology applied, majority of which is also about applying GaN in well-established topologies and packaging the converter with available techniques.

Generally speaking, there are three types of converters with GaN device applied:

- The majority of GaN converters use GaN HEMTs simply as drop-in replacements of Si MOSFETs and consequentially, performance of such converters is affected only by switching devices i.e. the influence of GaN technology on performance of converters is at device level.
- GaN converters operate at frequencies beyond the reach of Si technology have also been built, the efficiency of which are maintained as reasonably high. These converters are designed and implemented with care being taken of circuit and device parasitic elements and efforts being devoted to other issues such as magnetics, control, etc.

Converter level improvements stimulated by applications of GaN technology is therefore demonstrated.

- Illustration of the effects of fast switching capacity of GaN devices at system level has been performed in high frequency, high power density GaN converters, in which, apart from the accommodation of GaN devices and realization of high frequency operation of the converter, also involves packaging of the converter.

Substituting Si MOSFETs directly with GaN devices has been performed in different kinds of DC-DC converters. The converters, according to switching conditions, can be broadly grouped as hard switching ones and soft switching ones. In this section, from the viewpoint of checking the performance of GaN converters in comparison with Si converters, converter examples that are designed and implemented with both GaN and Si will be presented rather than simply listing all the converters that were built with GaN products. In the examples, a GaN converter uses the same topology, have identical layout and are of the same components (except the switching device) as the converter with Si device. These converters are mostly operated at low frequency levels (not higher than 1MHz) as confined by the switching capacity of Si devices.

- In hard switching converters, GaN HEMTs are subjected to hard turn-on and turn-off switching process, under what conditions loss reduction of semiconductors and corresponding efficiency improvements of converters cannot always be achieved.
    - Hard-switched synchronous buck converter with GaN HEMTs have been developed for the application of POL. Compared with Si based solutions, more efficient power transfer can be realized with the usage of GaN. In a 12V/1.2V POL converter that has a load up to 20A, improvements of peak and full load efficiency up to 4% and 3%, respectively, can be obtained when two early-version of 40V GaN HEMTs, rather than 30V Si MOSFETs, are employed at 1MHz [2-54]. Moreover, with the new-version of the 40V GaN HEMT and a new 30V GaN HEMT applied in the same converter, peak efficiency has been further increased from 89% to 91.5% mainly because of the reduced on-state resistance [2-56]. GaN HEMT based CCM synchronous buck converter has also been designed for LED driver. In [2-57], a 48V/28.3V synchronous buck converter with 200V GaN HEMTs being used was compared with a 200V Si MOSFET one with similar setups, which are in CCM and operated from 100kHz to 1MHz with a load of 22.6W. GaN converter presented almost the same efficiency as the Si converter at 100kHz but performed better than Si solution in the rest of the frequency spectrum indicating that GaN have lower switching loss but higher reverse conduction loss during deadtime.

- A two-switch, isolated forward converter was built with 300V GaN HEMTs in [2-58], the efficiency of which was compared with that of a Si MOSFET based identical converter. The converter has an input voltage of 200V and an output voltage of 24V and was assessed at two different operation frequencies (100kHz and 500kHz) in CCM. It was found that, attributed to both lower switching and conduction loss in switching devices, efficiency of the GaN version excels the Si one at both frequencies when evaluated in a load of 100W~500W: at 100kHz, efficiency increment is the range of 0.9%~3.5% across the load while at 500kHz, 4%~6%.
- In two 50V/150V, 100W boost converters with a frequency of 1MHz in [2-59], a 200V GaN HEMT exhibited 2.67 times higher loss than a 200V Si MOSFET when they are operated in CCM. It was revealed that the 200V GaN HEMT used has higher output capacitance than the Si competitor, leading to higher turn-on loss which dominates in total loss.

As can be observed, loss reduction does not always occur when GaN HEMTs are used as direct replacements of Si MOSFETs in hard switching. Switching loss reduction was achieved in some of converters while in others switching loss increment was seen. Besides, less on-state conduction loss would be generated while reverse conduction loss was reported as high. *The inconsistence of loss reduction in hard-switched GaN converters suggested that in-depth knowledge on switching behaviours and loss characteristics of GaN devices are needed so as to find out under what conditions loss reduction of switching devices and efficiency improvements of the converters can be achieved.*

- Soft-switched converters that could enable ZVS or ZCS switching conditions for transistors to lower switching losses have also been built. Performance of the GaN HEMTs converters under soft switching conditions, similar to that in hard switching, did not show consistence in improving the efficiencies from Si converters and, in the converters using GaN do show less loss, efficiency improvement is also limited.
  - A typical 48V/12V Isolated step-down DC-DC converters commonly seen in intermediate bus architectures (IBA) was constructed in [2-60], which is composed by a full-bridge, a transformer and a center-tapped rectifier, makes use of 100V GaN HEMTs as primary switches and 40V GaN HEMTs for secondary switches. The converter employs a soft switching technique to enable ZVS for the primary devices and a resonant approach to achieve ZCS for the secondary devices and, when operated at 1.2MHz with a maximum load of 400W, exhibited 25% decrease in transistor loss as GaN HEMTs have lower on-

resistance and smaller capacitances, leading to 1% improvement in peak efficiency over its Si MOSFETs based competitor.

- Two identical 48V/12V,300W LLC converter resonant converters that can also achieve ZVS for primary side devices and ZCS for secondary side devices are constructed for highlighting the benefits of GaN. Peak and full load efficiencies of the GaN converter are measured as 97.5% and 96.1% at 500kHz, respectively while the values are 97.2% and 95.8% in the Si converter, respectively, resulting in a 0.3% efficiency increase in efficiency curve [2-61]. Contribution of loss reduction from GaN HEMT roots from lower switching loss as the GaN HEMT and Si MOSFET have almost the same on-state resistance.
- In a dual active bridge (DAB) converter that has ZVS switching in transistors of the primary side bridge and synchronous rectification at secondary side was implemented with 200V GaN HEMTs as primary side switches and 30V MOSFETs on the secondary side. And it was revealed that 40% loss reduction can be achieved, which was made possible by reduction in both switching and conduction loss, when compared to the best considered all-Si combination when 150V is converted to 12V at 1MHz with a load of 150W [2-62].
- A flyback-forward with active-clamp circuit achieving ZVS turn-on and ZCS turn-off of transistors was proposed in [2-63] and implemented by both Si and GaN power devices. The converters are tested with a specification of 25V/380V at 200W. A 1.8% efficiency increment that was enabled mainly by the low on-state resistance of GaN HEMTs was seen when the converters are operated at 100kHz.
- In the 1MHz,50V/150V boost converters which compares losses in a 200V GaN HEMT and a 200V Si MOSFET in different operation modes, when ZCS was facilitated, loss within GaN transistor is still larger than that of the competing Si one (3.2 times higher), although conduction loss is lower as on-state resistance is smaller. In a mode of so-called BCM with valley switching under the condition that output voltage is larger than two times the input voltage, where ZCS was maintained and was also activated, more than 54% loss reduction was achieved in the new device compared with loss in the Si device [2-59].

In soft switching converters, simply applying GaN HEMTs as drop-in replacements of Si MOSFETs would not always lead to loss reduction in switching devices. Application of the new devices according to their loss mechanisms is needed, which cannot be realized without thorough investigation on switching behaviours and loss characteristics of the devices.

In both hard-switching and soft-switching converters, replacing of a Si semiconductor with GaN counterpart directly does not always bring about loss reduction in switching devices and consequential efficiency elevation. Besides, in the cases where gain can be obtained, the influence on efficiency is limited. And thus, it can be concluded that more insights of switching behaviours and loss characteristics of GaN transistors is a necessity to find out desirable operation conditions of the devices so as to really take advantage of the new technology.

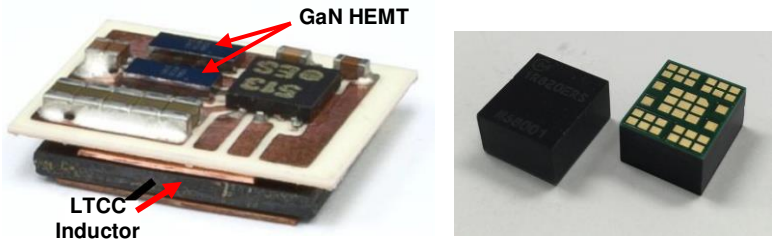
Pushing frequency of a traditionally used converter up to a level that is beyond the reach of Si devices while keeping efficiency reasonably high was also experimentally investigated with GaN HETMs. The trials are all conducted with special efforts to deal with parasitic elements rooted from both GaN transistors and circuit carriers for the purpose of minimizing switching loss. Besides, implementation of the converters is also accompanied by subsidiary actions like design of high frequency magnetics, improved control schemes, etc. The converters are all based on existing topologies that were designed to suit Si devices, the maximum switching frequency of which has reached 10MHz with GaN devices.

- A 5MHz flyback converter employing 200V GaN HEMT as primary side switch and 100V GaN HEMT as secondary side rectifier was built to perform a 48V/12V conversion with a maximum power of 30W. ZVS was provided for both transistors through the usage of resonance between circuit and transistor parasitic elements. Besides, care was also taken to deal with parasitic inductances in the used PCB layout, especially about the so called “common source inductance”, which was minimized to a low value of 0.7nH. Together with the negative voltage applied which is beneficial for speeding up turn-off transient and reducing turn-off loss, peak efficiency of 87% was obtained [2-64].
- A 10MHz isolated DC-DC converter was demonstrated in [2-65], in which a 200V GaN HEMT was applied. The converter consists of an inverter stage and a rectifier stage and the two stages are isolated by a transformer. Utilizing inductance in the circuit and parasitic capacitance of the GaN HEMT, ZVS switching was achieved for the GaN transistor. The converter has converts 50V input to 20V output and has a maximum output power of 10W. A nearly constant efficiency of 69% was measured in the 2~10W range.
- With great attention been put to enhance in-circuit performance of a 65V GaN HEMT by the means of elimination of common source inductance, reduction of loop inductances through flux cancellation, etc., a hard-switched 40W, 48V/12V synchronous buck converter was successfully built. The 10MHz converter, which showed a peak efficiency of over 89%, fostered a new application of envelope tracking that was not possible with Si devices [2-67].

The success of pushing frequencies of GaN based power converters up under the conditions of either utilizing parasitic elements of GaN transistors and circuits or minimizing parasitic inductances in circuit indicated that GaN devices needs to be well accommodated to really take the high frequency operation potential of the new technology. Similar to what was concluded in previous examples, in-depth understanding on effects of parasitic elements in both GaN devices and the circuit carriers they were located is needed. Moreover, converter level design and optimization is needed for the realization of converters operating at such high frequencies.

Take fast switching advantage of the new devices at system level i.e. making high power density converters with the help of GaN transistors has also been carried out. Compared with the attempts of using GaN devices to reduce losses of switching devices and stretch frequency span of power converters, design and implementation of converters with high frequency, high power density demands more than layout design to accommodate GaN devices and optimization of passive components, control schemes, etc., packaging of the converter, which includes disciplines such as passive integration, 3D electromagnetic design, advanced thermal management approaches, etc., is also of great importance. So far, high power density DC-DC converters with GaN HEMTs applied, all of which involve great efforts to deal with circuit and package parasitics to best suit the transistors, have already been demonstrated and the operation frequency excels that of Si products with similar specifications in most cases. To our knowledge, however, power densities of these converters are not as good as the best state-of-art Si products at this moment.

- Using two 40V GaN HEMT, a 12V/1.2V hard-switched synchronous buck converter was built to serve as a POL converter. Frequency of the converter was pushed up to 2MHz, leading to low output inductance which facilitates the integration of the inductor by low temperature co-fire ceramic (LTCC) technology. Together with the usage of direct bonded copper (DBC) instead of PCB to enhance power handling capacity, a power density of the POL converter up to about 900 W/in^3 was achieved with a maximum output current up to 20A. The power density excels most of the commonly seen Si based POL converter with similar ratings, but is lower than the best state-of-art Si ones. A power density of as high as 1125W/in^3 was seen with the product from Murata (MYMGK1R820), which is also a 12/1.2V, 20A synchronous buck converter with a fixed switching frequency of 500kHz.

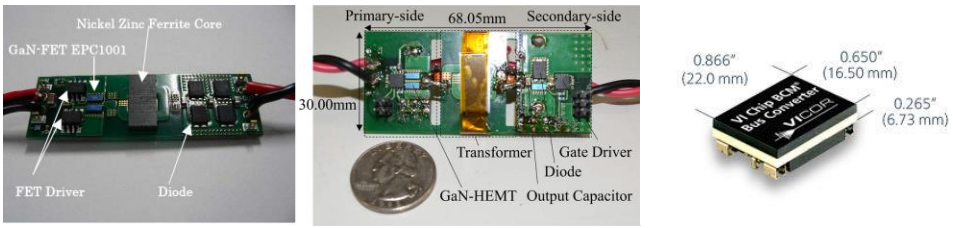


(a) (b)

Figure 2.3 High power density 12V/1.2V POL converters

(a) GaN based [2-54]; (b) Si based [2-68]

- Attempts on improving power density of IBA converters have also been conducted. Employing the architecture of half-bridge GaN HEMTs based inverter and a full Si diodes bridge rectifier with a transformer in between, a 48V/12V converter with a maximum power of 120W was built in [2-69]. By pushing operation frequency of the converter up to 5MHz with the aid of ZVS switching of primary transistors, power density of the converter was quantified as 233W/in^3. A similar structure and operation mode were used in [2-70] with the difference that diodes in the low side arms of the bridge implemented by 40V GaN HEMT, with the same input and output specification as well as switching frequency, a power density of 269W/in^3 was obtained. Although both prototypes operate at a frequency that has not been achieved by Si devices, the power density, however, did not outperform that of a Si solution. In a soft-switching isolated 48V/12V product from Vicor that has a maximum output current of 10A, a power density of 801W/in^3 was seen when it is operated at 1.5MHz. It was promoted that a higher value, 840W/in^3, has already been achieved with the same input and output specifications but a higher frequency of 1.75MHz [2-71] [2-72].



(a) (b) (c)

Figure 2.4 High power density 120W, 48V/12V IBA converter

(a) 233W/in^3 with GaN HEMT [2-69]; (b) 269W/in^3 with GaN HEMT [2-70]; (c) 801W/in^3 with Si [2-71]

Furthermore, a 48V/12V GaN HEMTs based IBA converter with current capability of up to 30A was constructed in [2-73]. The converter consists of a full-bridge and a center-tapped rectifier, which are isolated by a transformer, with ZVS be facilitated for both

primary and secondary devices, operation frequency was increased up to 1.6MHz and a power density as high as 900W/in^3 was accomplished. Contrary to what was claimed in the publication, it failed to surpass the available Si counterparts as Vicor also developed an isolated 48V/12V product that has an output current of 25A, a switching frequency of 1.95MHz, and a consequential power density of 1022W/in^3 [2-74]

(a) (b)

Figure 2.5 High power density 300W, 48V/12V IBA converter

(a) 900W/in^3 with GaN HEMT [2-73]; (b) 1022W/in^3 with Si [2-74]

It is worth highlighting the facts that: a).in all the GaN based high power density converters, the transistors are subjected to natural convections; b) size of the GaN HEMTs are negligibly small as compared to either Si products with similar ratings or the rest part of the circuit they were used in. Comparisons of power densities between GaN converters and Si converters, especially under the scenario that GaN converters generally are operated at higher frequencies than Si ones, thus indicate that better system-level packaging techniques at frequencies higher than what is achievable by Si technology are called for.

As can be seen with the presented examples, GaN HEMT based DC-DC converters are mainly low power (<1kW) ones and the reason is that GaN HEMTs have breakdown voltages from 15 to 300 V and current carrying abilities of tens of amperes, especially with the devices of early version. There are few high-power DC-DC converters built with the help of GaN HEMTs through either paralleling of GaN devices or interleaving of converter units. For instance, an isolated converter with full-bridge on both sides, which are separated by a transformer, was implemented at 50kHz in [2-75] and analysed in [2-76]. In primary side of the converter, each of the switch in the bridge is implemented by paralleling four 200V GaN HEMT while, in the bridge of the secondary side, four paralleled 100V GaN HEMT were used for each switch. The hard-switched 130V/52V converter functions bidirectional as either buck type or boost type and reached 1.7kW with an efficiency of 98.8%. Besides, an interleaved 48V/12V buck converter using 100V GaN HEMTs was developed, in which five commutation cells are connected in parallel [2-77]. The converter has an effective switching frequency of 1.5MHz (each single switching cell operates at 300kHz) and an efficiency of up to 97% for a 1.8kW power converter. Compared with state-of-art converter with similar rating, 40% loss reduction was realized through both the replacement of Si transistor with GaN HEMTs and the optimization of magnetic components. In addition, a 480W,

48V/12V hard-switching synchronous buck converter was demonstrated in [2-78], which contains four 100V GaN HEMTs in parallel for the top switch and the synchronous rectifier (in total eight transistors). This configuration can be considered as paralleling of either device or switching cell (half bridge). The converter presented efficiencies above 96.5% from 35% to 100% load.

To summarize, GaN HEMTs do have the ability of fast switching as characterized in clean-switching environment. GaN HEMTs have already been applied in DC-DC converters for the purpose of taking advantage of such ability. The results suggested that:

- Direct adoption of the GaN HEMTs as substitutes of Si MOSFETs does not always show beneficial in terms of loss reduction, as can be obviously observed in device-level applications of the new technology. In-depth knowledge on switching behaviours and loss characteristics of GaN devices is a must.
- High frequency operation of GaN converters is possible even at a level that is not achievable with traditional Si technology. These converter-level benefits brought about by GaN are made possible with special attention being paid to accommodate GaN devices as well as supplementary actions to take care of other parts of the converter so as to realize high frequency operation. Besides, the converters are all of existing topologies that were developed to suit Si devices and whether these topologies are suitable for pushing up operation frequency of GaN converters were not investigated.
- System-level gain enabled by the new technology are, so far, limited as indicated by the comparisons between power densities of Si converters and GaN ones, although, in most cases, operation frequencies of the former is lower than the latter. Packaging and miniaturization approaches of GaN converters at high frequencies beyond the reach of Si technology, therefore, is pressingly needed. In short, to exploit benefits of GaN technology, all issues involved in design and implementation of high frequency converters should be considered.

2.4.2 GaN GIT based high frequency converters

Attempts to apply GaN GIT in power electronics converters, compared with that of low-voltage GaN HEMT, are limited, as GIT appeared in commercial market only recently. Of the limited trials, efforts were devoted either to improve efficiency of a converter at relatively low frequency (high-power DC-DC converters with high voltage GIT) or to push frequency of a converter up (in some cases even beyond the capability of a Si one) while keeping efficiency reasonably high (low-power DC-DC converters with low voltage GITs). So far, investigations on other performance measures of a converter such as power density, size, etc., with the advent of GaN GIT has not actually been performed, although the necessity and possibility of shrinking size of magnetic components was observed in a high frequency resonant converter enabled by a 600V GIT [2-79].

Efficiency elevation of power converters through replacement of the of old-fashioned Si devices with new GaN GIT was carried out mainly with high voltage GaN HEMTs. Similar to the case with GaN HEMTs, limited gains were obtained in terms of converter efficiency increment at low frequencies (tens of kHz).

- Application of 600V/15A GaN GIT for photovoltaic (PV) system was carried out in [2-49], in which a 50V-350V/350V hard-switching boost converter was built for maximum power point tracking (MPPT) with a power delivery capability of up to 1.5kW. With a frequency of 48kHz, the converter showed better efficiency than that of a Si IGBT based identical converter: at 150V input 1.7% higher and at 250V input 0.9%. Maximum efficiency at 150W was measured as high as 98.6%.
- Using a 600V GaN GIT with flip-chip configuration, a boost converter, which functions as part of a totem-pole bridgeless PFC in a power supply, was made and compared with that of the one with Si super-junction MOSFET [2-80]. The boost converter has a rectified $230V_{ac}$ input and an output voltage of 400V, a peak efficiency of 99.3% was observed at 1kW while maximum power of the converter reached 3kW. The 50kHz converter outperforms the Si one with more than 1% at full load.

Pushing up frequency of GaN GIT based power converters are, up to date, only performed in low-power DC-DC converters, the overwhelming majority of which is POL converters, were developed both with discrete low voltage transistors and with integrated modules. In these converters, circuit parasitic inductances are minimized by means of optimized design or integration. Up to now, maximum frequency of GaN GIT based converters is pushed up to 5MHz, at which frequency reasonably high efficiency was maintained.

- A 12V/1.2V POL converter with hard switching was built in [2-81] with 30V GaN GITs that have an on-state resistance as low as 1.8 mΩ. A single GIT is used for the high-side transistor while two GITs are paralleled for the low side. Performance of the converter was compared with a Si based solution at 2MHz with load current scales from 5A to 50A. It was shown that the GIT based converter reached a peak efficiency of 90% and an efficiency elevation in a range of 7%~14% was observed as load varies. Besides, frequency of the GIT converter was pushed up to 5MHz, at which a peak efficiency of 81% was achieved.
- High frequency POL converters based on integrated GIT modules, which is beneficial for reducing parasitic inductances, have also been demonstrated. A converter IC that consists of two 30V GaN transistors and associated high speed gate drivers was successfully fabricated and used in a 12V/1.8V POL converter. The converter was operated in [2-82] at 1MHz with a maximum power of 18W and a peak efficiency as high

as 92% was reached. The converter was also tested at 2MHz, at which frequency a peak efficiency of 88.2% was achieved [GIT for power switching applications].

Monolithic fabrication of a 30V GaN GIT with a Si Schottky Barrier Diode (SBD) for the purpose of minimizing losses generated in reverse conduction (conduction of current from source to drain when gate-source voltage is below gate threshold) was conducted in [2-83]. The SBD has a forward voltage drop of about 0.85V, which is at least 15% lower than the voltage a single GIT would have when it conducts in reverse direction. When used in a 12V/1.3V converter at 2MHz showed an efficiency boost of more than 1.5% at a full load current of 25A.

To summarize, employment of GaN GIT in power converters have not been widely performed yet due to the relatively late appearance of the products. With the limited applications of them, the high power ones, which are built with high voltage (600V) GITs, are opereated at low frequencies and limited improvements were seen when compared with identical Si coverters. Pushing frequency of a low voltage GaN GIT based converter up have also been performed, in which parasitic elements are dealt with. The examples indicated that accomodating of GITs under the influecne of parasitic elements is also indispensible for high frequency application of them.

2.5 Challenges of GaN transistors and converters

As already introduced, GaN HEMTs and GaN GITs are fundamentally different from traditional Si MOSFETs because of the basic structure of the AlGaN/GaN heterojunction. The resulting benefits e.g. fast switching speed, low on-state resistance, etc. from the high density, high mobility 2DEG, however, is also accompanied by challenges like absence of avalanche capability, current collapse phenomenon, etc., that are also inherently generated by the unique structure. A paradigm shift from conventional practices of designing and implementing power converters is therefore called for to achieve successful application of the new technology: on one hand, to really take advantage of the benefits, proper actions on how to accommodate GaN devices should be taken as indicated by the first converter prototypes with the new devices applied; on the other hand, attention also needs to be paid to the way the GaN transistors are used so as to prevent the problems that are inherent with the devices from occurring. In this section, the shared issues of GaN transistors and challenges in converter design will be highlighted, using single-die GaN HEMT and GaN GIT as case studies. Possible solutions, which implies development trend of high frequency GaN based converters, are also discussed.

Avalanche capability that permits a power semiconductor to be able to survive a limited exposure to voltages beyond device rating is not possessed by lateral GaN HEMT and GaN GIT. Unlike Si MOSFETs, GaN HEMTs do not rely on a p-n junction for voltage blocking and thus do not have the potential for avalanche breakdown [2-12] [2-18]. And consequentially, GaN HEMTs

and GaN GITs are subjected to dielectric breakdown when overvoltage occurs. This breakdown is destructive and non-reversible. Currently, no viable remedy methods exist to combat this problem. Derating of the devices i.e. always applying GaN HEMTs at voltage levels considerably lower than the maximum allowable value is necessary.

Current collapse or dynamic on-state resistance has been widely reported with GaN HEMTs and GaN GIT, a phenomenon that is caused mainly by two mechanisms. The first being the electrons trapped at surface of the passivation layer at the gate edge facing the drain edge. When a GaN transistor is in off-state, because of the lateral structure, gate-drain voltage is reverse biased with the majority of the rail voltage and the unevenly distributed electric field, the strongest of which presents near the gate edge, causes electrons to be trapped in the impure passivation layer. The trapped electrons have longer lifetime than the ones that are intentionally injected directly beneath the gate, as a consequence, the trapped charges act as a "virtual gate", weakening the 2DEG and enlarging on-state resistance after the transistor is switched on [2-12]. The second source being the "hot electron effect" which lead to electrons that are injected into and then trapped at impure deeper layers [2-18]. These trapped charges, in a similar way as the ones in the first mechanism, weaken the 2DEG and increase on-state resistance. Both of the effects are proportional to blocking voltage and the "hot electron effect" has also been shown to increase with higher switching loss [2-11] [2-84].

Noticeable progress has been made to mitigate the current collapse problem. Improved passivation of the AlGaN surface would facilitate fewer impurities and is helpful to alleviate the phenomenon as surface trapped charges can be minimized [2-85]. A more commonly used suppressing method is through the use of field plates to reduce the electric filed strength around the gate edge and distribute it more evenly [2-11]. This approach, however, will enlarge parasitic capacitances of the switching devices, which, as will be shown in chapter 5, is detrimental in hard switching applications. Voltage derating of a GaN HEMT is also an option because both of the charge-trapping effects are field-dependent and will be eased at low voltages [2-18].

Reverse conduction of a GaN HEMT is also different form that in a conventional Si MSOFET. In a MOSFET, resulting from p-n doping of the body and drift region, a body diode exists and conducts current from source to drain when the device is in off-state. In a GaN transistor, however, such a body diode is not present as there is no body region or doping in the drift region [2-12]. Reverse conduction in a cascode GaN HEMT is made possible as conduction of the body diode of the low-voltage Si MOSFET will turn on the channel of the depletion mode GaN HEMT. The overall reverse conduction behaviour resembles that in a MOSFET. Reverse recovery charge in a cascode GaN HEMT is much lower than a that of the body diode in a Si MOSFET with comparable ratings as the MOSFET in the cascode GaN is a low voltage one. Reverse conduction of a single-die GaN HEMT and a GaN GIT, on the other hand, is completely different.

The symmetrical structure of single-die GaN HEMTs or a GaN GIT makes it possible for the 2DEG to become conductive when a sufficient gate-drain voltage is imposed. With GaN HEMT, a forward voltage of 1.7V will be present while, with GaN GIT, 1.3V, which are high compared to forward voltage of body diode in a Si MOSFET (below 0.7V). And therefore, care should be taken to either minimize reverse conduction time to lower associated loss. Besides, when a negative-voltage is applied at turn-off for the sake of reducing switching loss, a trade-off between the reduced turn-off loss and increased reverse conduction loss needs to be considered to find optimal voltage value. Anti-paralleling diodes with low forward voltage could also help to reduce conduction loss but would add up to parasitic capacitance between drain and source of the GaN transistor, which is not desirable in hard switching conditions. A Si Schottky diode on the same die of a GaN GIT was successfully formed by the Si substrate and a metal electrode and is effectively anti-paralleled to the GIT through a via-hole. This diode helps to reduce the forward voltage down to 0.85V when GaN conducts in reverse direction [2-83].

Gate driving requirements of a cascode GaN HEMT are more or less the same as that of a Si MOSFET as driving of the GaN transistor is essentially executed on the low-voltage Si MOSFET, of which the input requirement is rugged e.g. high threshold voltage, high absolute gate voltage, etc. With single-die GaN HEMTs and GaN GITs, however, special attention needs to be paid to driving approaches as most of the devices have a threshold voltage in range of 1~2V while the recommended driving voltage is typically around 4~5V. The low limits make the driving of the transistors demanding as both spurious turn-on and gate rupture, which is a common issue with single-die GaN HEMTs, need to be avoided. In particular, with Schottky gate GaN HEMT and p-AlGaN GaN GIT, steady-state gate currents could be requested because of their diode-like gate structure [2-86] [2-87]. The injection of holes further enhances the conductive channel and reduces conduction loss but introduces losses in gate driver and gate terminal of the transistors. A trade-off should be considered for minimized overall loss. And thus, rigid gate driving requirements on both voltage and current need to be fulfilled.

Up to date, gate driver products or gate driving circuitries customized for GaN HEMT and GaN GIT have already been developed. With GaN HEMT, the gate driver ICs from TI, LM5114 for driving single GaN device and LM5113 to drive both a high-side and a low-side GaN device, are commercialized. The ICs, however, need further improvement to be suitable for wide applications. Isolation between high-side and low-side of the LM5113 is confined to 100V and cannot function beyond and, with LM5114, signal isolation is not provided [2-12] [2-88] [2-89]. Besides, output resistances of the two drivers are too high, causing more switching loss in GaN devices and conduction loss within the ICs [2-88] [2-89]. With GaN GIT, several gate-driving solutions are proposed to meet the driving needs of GIT [2-90] [2-91]. It was reported that a gate driver from the manufacturer of GIT is also to be launched to market, a product that is designed in particular

to drive 600V GaN GIT with high sourcing and sinking currents during both turn-on and turn-off transients and mA sourcing currents in steady state after turn-on [2-92].

Circuit and device parasitic elements affects performances of GaN transistors and that of GaN converters and needs to be dealt with properly to best accommodate GaN devices to achieve high frequency operation. Fast switching ability of GaN transistors have been testified through both characterization of switching transients and efficiency improvements of GaN HEMT and GaN GIT. The significantly increased slewing rate, di/dt and dv/dt, of GaN devices amplify the influences of parasitic inductances and capacitances in device package and circuit carrier, which could potentially lead to failure of GaN devices or malfunction of the power converter if not properly dealt with. Parasitic elements affect performance of a GaN device and function of a GaN converter in many different ways.

- Parasitic inductances that originate from both power loop and gate driver loop affect switching behaviours of a GaN device. In particular, as with a GaN HEMTs and a low voltage GaN GIT, electromagnetic volume of the device is negligibly small in comparison to the rest parts of a power converter and thus layout design is more critical. It was made clear in [2-93] and [2-94] that, similar to that in a Si MOSFET as elaborated in [2-95], gate loop inductance affects switching speed of GaN HEMT and GIT with common source inductance the most critical one, especially in hard switching conditions. Besides, parasitic inductances in both power loop and gate loop resonant with parasitic capacitances arise from devices and circuits, leading to high frequency oscillating currents and voltages. This may deteriorate performance of the converter in different measures: a) overvoltage may occur across a GaN transistor, may it be gate-source or drain-source, triggering breakdown of the device, particularly when the transistor does not have avalanche capacity and is subject to gate rupture, which is true with both GaN HEMT and GaN GIT; b). oscillatory energy circulates in circuits lowers power transfer efficiency; c). the ringing causes radiative EMI and interfere with converter operation. And therefore, minimization of parasitic inductances in both gate loop and power loop is necessary, especially in hard switching converters.
- Parasitic capacitances in GaN transistors, in addition to causing oscillation with parasitic inductances, would affect proper function of a half-bridge configuration. With both GaN HEMT and GaN GIT, the “cross-talk” problem was addressed. During turn-on of the low-side transistor, the fast dv/dt across it would also cause drain-source voltage of the high-side device rises rapidly, inducing a current though miller capacitance and a potential difference between gate and source of the high-side transistor. When this potential exceeds threshold voltage of the upper transistor, inadvertently turn-on of it occurs, leading to a short circuit of the DC link through two GaN transistor channels, which lowers

efficiency and may also lead to failure of the devices and the converter [2-11] [2-96] [2-97]. Besides, during turn-off of the low-side transistor, a negative spurious voltage would also be imposed on gate-source of the high-side one caused by the same mechanism. Although this negative voltage will not lead to a shoot-through like what the positive one could, care should also be taken to make sure that it does not surpass the maximum allowed negative voltage rating of gate-source [2-96].

Conventional methods on how to mitigate such problems e.g. optimizing PCB layout, enforcing negative turn-off voltage, deadtime determination approaches, etc., see their limitations in terms of ensuring proper functioning of the converter, effectiveness in loss reduction, etc., when it comes to GaN devices and more advanced approaches are required. With the devices of GaN HEMT and GaN GIT and the converters utilize them, innovative solutions are emerging to combat the challenges:

- With discrete GaN HEMT and GaN GIT, packages of the devices promise low parasitic inductances are being used. With GaN HEMT, chip-scale packages, as will be illustrated in chapter 4, are used from the very beginning and ultra-low parasitic inductances are guaranteed (In a 200V GaN HEMT, inductances at gate, drain and source terminals are 0.07nH, 0.07nH and 0.08 nH, respectively). With GaN GIT, packaging of a 600V device has evolved from leaded TO220 to a SMD package called Dual-Flat No-lead (DFN) to minimize parasitic inductances on device level. And it was calculated that the flip-chip package enables a dramatic reduction of parasitic inductance of more than 90% from the old-fashioned TO220 package [2-80]. It's worth pointing out that in some GaN devices e.g. products from Transphorm, GaN system and VisIC, a kelvin source connection is provided as a separate connection to source metallization. This kelvin source decouples the gate loop from power loop so as to mitigate the effects of common source inductance [2-98] [2-99].
- Integration is also a way of reducing footprint and, consequentially, parasitic inductances. As already mentioned, co-packaging of a GaN transistor with electronics parts e.g. gate driver, control circuitry, etc. has already been tried out. Moreover, in general, lateral devices are more convenient for monolithic integration than vertical ones and lateral GaN transistors are particularly well suited because they have thin active layers and insulation between individual devices can be easily made [2-18] [2-85]. Currently, integrated modules of both GaN HEMT and GaN GIT have been performed, either through co-packaging or monolithic integration.
    - With GaN HEMT, apart from the co-packing of a single transistor with a gate driver as already introduced in 2.3.2, an integrated power stage solution

consisting of two 80V/10A GaN HEMTs and gate drivers has also been produced by TI [2-100].

- With GaN GIT, integrated solutions for the sake of decreasing circuit parasitic inductances have been successfully demonstrated. For example, in [2-82], a p-AlGaN GIT is grown together with a depletion-mode GaN HEMT, between which the only difference is whether the p-gate is present, and then fabricated with gate drivers to generate a POL converter IC. The 12V-1.8V converter was operated in a frequency range of 1~3MHz and up to more than 20W. It was estimated that minimization of parasitics through monolithic integration contributes to 19% switching loss reduction from a discrete converter. Meanwhile, monolithic fabrication of six GaN GIT as an inverter IC has also been conducted to minimize parasitic inductances [2-101] [2-102].

- The "cross-talk" issue that the turn-on of one transistor will cause un-wanted switch-on of a complementary transistor in a phase-leg configuration is more likely to happen with GaN than with SiC as threshold voltage of GaN devices are generally low. The problem cannot be simply mitigated by slowing down the turn-on process e.g. enlarge turn-on gate loop resistance, parallel external capacitors to gate-source, etc. as switching loss and gate driver loss will be increased, a trade-off between cross-talk induced loss and switching loss need to be considered. Reduction of turn-off loop resistance to avoid gate-source voltage exceeding threshold voltage when high dv/dt induced current flows is also not an easy option as low loop resistance increases the risk of gate overvoltage. Furthermore, the practice used with the case of SiC, enforcing a negative voltage at turn-off and during off-state cannot be applied directly with GaN due to the fact that more loss will be generated when reverse conduction is initiated [2-12]. An active gate driver that could suppress the cross-talk while not affecting switching speed of the transistors was proposed for SiC in [2-103]. This proposal could also work for GaN devices and has already attracted attention of GaN users [2-12].

In-depth knowledge about characteristics of GaN devices e.g. switching and conduction characteristics, loss mechanisms, etc. is, at this moment, not available, especially with GaN GIT. As was clearly shown in the section of 2.4, performance improvements of converters brought about by GaN technology cannot be consistently achieved when GaN devices are simply used as drop-in substitutes of conventional Si devices and pushing-up of GaN converter frequencies are all accompanied with soft switching conditions and actions to minimize or utilize circuit and device parasitics. Comprehensive knowledge that is needed to understand the reasons behind, however, is missing. To guide design and implementation of high frequency GaN converters, full insights into switching and conduction behaviours and associated loss characteristics of GaN devices is a

must. Loss modelling of GaN devices is an effective way to reveal desired switching conditions of the new devices. So far, loss modelling of GaN HEMTs has been performed while, with GaN GIT, modelling of losses in the devices has not been carried out. The developed models for GaN HEMT, however, are not comprehensive. For instance, in the model developed in [2-67], which was used for design and optimization of high power density POL converter, the influences of inductive elements on losses of GaN HEMTs were accounted for while the effects of capacitive elements are not. Better loss models of GaN devices are pressingly needed.

Passive components suitable for frequencies higher than what has been achieved with Si technology are needed to harvest high frequency benefits of GaN technology in practical applications. Ideally, the magnetic materials should have low energy loss at high frequencies. At this moment, in applications where GaN devices are properly used, magnetic components are becoming the limiting factor on performance improvements of high frequency converters. For instance, as was discussed in [2-109], temperature increase on the transformer is much more severe than that of GaN transistors in a 1kW, 1MHz LLC converter. Moreover, it was demonstrated in [2-104] that, with commercially available magnetic materials, downsizing of magnetic components, which usually are the dominating parts in converters regarding weight or volume, cannot only be performed up to 2MHz as confined by loss density of magnetic cores, although with the newly developed samples the achievable frequency could possibly be as high as 10MHz [2-104]. Generally speaking, availability of high frequency magnetic materials is very limited, especially with the commercialized ones and, with the available options, material properties and loss mechanisms are not well understood and modelling and prediction approaches of losses have not been developed. For instance, with NiZn ferrites that are innovated for frequencies up to 10MHz, a so-called DC effect, a term that stands for the phenomenon that core loss increases substantially with dc magnetic flux, was well-documented. However, no general theory or models exists to allow designers to take the effect into consideration [2-105] [2-106].

On-going research focusing on developing new magnetic materials is making progress and materials that could work up to 20MHz with low loss density and constant permeability have been reported [2-106]. Also, more and more data and approaches for quantifying losses in high frequency magnetics are becoming available. For instance, a term of performance factor was proposed to effectively evaluating size scaling of high frequency magnetic cores using only datasheet information and basic Steinmetz parameters [2-105]. Besides, core loss measurement methods suitable for assessing losses in high frequency magnetic materials e.g. the calorimetric approach in [2-107] provides not only data on loss in two different magnetic materials up to 1MHz but also can be used as a platform for generating more measurement results, which could be useful for deriving empirical equations to account for DC effects in certain magnetic materials [2-108]

Packaging of converters is also a discipline that is critical for taking at high frequency application of GaN technology. On one hand, converter or system level packaging is one way of better accommodating GaN devices so that operation frequency of a GaN converter can be increased as much as possible. For instance, in [2-54], 3D design of a POL converter was performed to minimize commutation loop inductance while in [2-48], a converter with coaxial structure was developed to achieve clean-switching i.e. resistive switching environment of GaN transistor. On the other hand, high frequency packaging techniques are demanded to really take advantage of the fast-switching speed character of GaN technology in converter or system level, as illustrated by the comparisons between power densities of Si power converters and GaN HEMT ones in section 2.4.

It should be noted that there are also other challenges with the newly introduced devices and their application in power converters such as qualifying of reliability, thermal managements, etc. which are either beyond the scope of this thesis or highly specific-application dependent, and thus are not accounted for in detail. Reliability of Si devices can be quantified through well-established standards and specifications. Whether these standards are also suitable for GaN devices are unknown and needs to be investigated [2-12]. Besides, thermal managements of a GaN device could possibly adding parasitic capacitances to GaN devices and, depending on the specific switching conditions, this could be either beneficial or detrimental [2-109] [2-110].

2.6 Discussion

To take advantage of the superior properties of GaN material in power electronics applications, great efforts have been devoted to design and fabrication of GaN power semiconductors. As was introduced in 2.3, due to the lack of high quality, low cost GaN substrates, most of the efforts are devoted to grow GaN device on non-GaN substrates. As a result, lateral GaN devices that are grown on foreign substrates dominate. Lateral GaN devices, in particular the commercialized ones, are HEMTs and HEMT derives that utilize high density, high mobility carriers formed by a heterojunction of AlGaN/GaN. With these GaN HEMTs, which are naturally in on-state, focus of innovations is mainly put on how to convert the devices as enhancement-mode (normally-off) since normally-on devices are less desirable in power converters due to safety and complexity concerns [2-13] [2-25]. Currently, approaches on converting a normally-on GaN HEMT into a normally-off one can generally be categorized as two groups: by modifying gate structure in a single-die GaN HEMT and by co-packaging of a normally-on GaN HEMT with other electronic parts, especially with a Si MOSFET (in cascode configuration).

Up to date, GaN products in both categories are market-available:

- Single-die, normally-off GaN transistor products utilize a gate-channel junction between gate and 2DEG channel to lift up potential between gate and channel, resulting in

normally-off operation. Three different junction-forming methods were adopted: deposition of p-AlGaN to form a p-n junction (e.g. in Panasonic GaN HEMTs), deposition of p-GaN gate cap forming a p-n junction (e.g. new version of EPC products) and employment of gate metal over channel to make a metal-semiconductor junction (e.g. early version of EPC products);

- Copackaging an normally-off enhancement-mode, low voltage Si MOSFET with a normally-on high voltage GaN HEMT with cascode configuration is an approach adopted by many to achieve normally-off GaN devices, of which 650V.

It should be noted that, with commercialized products from GaN system, which are also single-die, normally-off devices, the exact gate structure is unknown and could be different from the approach of forming of a gate-channel junction.

- Cascode GaN devices inherit the gate features of Si MOSFET including rugged structure, high threshold voltage, etc. Besides, driving is made easy as conventional gate drivers for Si MOSFET can be used. The devices, however, are subjected to influences of parasitics:

In this work, attention of investigation will be paid to single-die, normally-off GaN transistors that are available from market. Even though cascode GaN devices has features of rugged gate structure, easy to drive, etc., they are not considered in this work as:

- Cascode GaN devices generally are more subjected parasitic elements: a) package and inter-connection induced parasitic inductance tends to be high, causing high switching loss [2-39]; b) interaction between the two devices may result in instability due to large package parasitic inductances [2-40]; c) mismatch of parasitic capacitance between the two dies may induce undesired features like avalanche of the Si MOSFET [2-41].
- From the long run, cost of GaN devices in cascode configuration would be higher as two dies are needed.

Table 2-2 Suppliers of GaN transistors at current stage [2-15]

Manufacture	Transistor type	Maximum operation voltage	Status
EPC	Single-die, normally-off GaN HEMT	450V	Commercialized
GaN system	Single-die, normally-off GaN HEMT	650V	Commercialized
Panasonic	Single-die, normally-off GaN HEMT	600V	Commercialized
Avogy	Normally-off JFET	1200V	Samples available

Table 2-2 Suppliers of GaN transistors at current stage [2-15] (Continued)

Manufacture	Transistor type	Maximum operation voltage	Status
Transphorm	GaN-Si Cascode, normally-off HEMT	650V	Commercialized
		1200V	Under development
ViSIC	Normally-on HEMT	650V	Samples available
Powdec	Polarization superjunction GaN FET	1200V	Prototype
Exagan	Normally-off FET	1200V	Under development
IR+Infineon	Normally-on HEMT	600V	Under development
	GaN-SI Cascode, normally-off HEMT	600V	
MicroGaN	Normally-on HEMT	600V	Under development
Sanken Electric	Normally-off FET	600V	Under development
STMicroelectronics	Normally-off HEMT	200V	Under development

2.7 Summary

GaN material has superior properties than conventional Si material, which makes GaN power semiconductors promising in outperforming well-established Si devices in high voltage, high temperature and high frequency applications. Since development of GaN technology is still in its infancy, practical issues like wafer quality, technology limitations, non-optimized device designs, etc., inhabit the devices from living up to the promises of the material. At this moment, high voltage and high temperature GaN devices are not available, especially with commercialized ones. As a consequence, attention on exploring potentials of GaN products has to be paid only to high frequency operations of the devices.

Currently, application of commercialized GaN transistors, in particular single-die GaN HEMT and GaN GIT, has mainly been conducted in existing power electronics systems where they are used as drop-in replacements of conventional Si devices. In these GaN converters, performance improvements are not consistently achieved, indicating that in-depth knowledge on switching behaviours and loss characteristics of GaN devices is needed to make use of the fast switching ability of the new devices. Besides, GaN converters operating at frequencies beyond the reach of Si technology have been demonstrated and high frequency GaN converters aiming for high power density has also been built, operation frequency of which are generally higher than Si counterparts while the power densities are generally lower. Performance of these converters suggests that, to take advantage of GaN technology in real applications i.e. at converter or

system level, more disciplines e.g. accommodation of GaN devices, high frequency magnetics design, packaging of converters, etc. needs to be considered.

To really benefit from the new technology of GaN devices in power converters, not only the aforementioned challenges e.g. unknown performance of GaN devices, design of high frequency magnetics, etc. that should be overcome through approaches such as loss modelling, exploration of high frequency magnetic materials, etc., but also issues with GaN devices e.g. lack of avalanche capacity, current collapse problem, gate driving requirements, etc. should also be dealt with properly.

2.8 References

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Chapter 3. Overview on PFC converters

3.1 Introduction

As introduced in previous chapter, GaN products are emerging and demonstrations have already been performed to show benefits of the new devices in existing power electronic systems. In this thesis, of which the purpose of investigating potentials of GaN devices in an existing application platform, the new devices are to be evaluated and their benefits are to be demonstrated in Power Factor Correction (PFC), which is commonly used in AC/DC converters.

In this chapter, the concept of PFC technique is introduced firstly in section 3.2 to provide insight on what is PFC and why the technique is needed. A review on available topologies to realize the technique then follows in section 3.3. The review is made by separating the topologies into different groups according to the conversion characteristics and, within each category, representative topologies that are widely investigated are presented. Pros and cons of each single topology are also discussed. Alongside with the discussion on the interactions between different stages in an AC/DC converter, namely EMI filter, PFC stage and DC-DC stage in section 3.4.1, overall effect that one PFC topology would bring on the whole AC/DC converter are made clear. Qualitatively comparisons of existing PFC topologies are then carried out in section 3.4.2 according to certain criteria that covers both the PFC stage and its interactions with other stages. With the view to select a suitable platform for exploring potentials of GaN devices, influence of pushing up operation frequency on properties of PFC topologies are assessed in section 3.4.3 and boost converter, which is still superior to others with GaN technology applied, is selected. Finally, a summary of the chapter is given in 3.5.

3.2 PFC technique

3.2.1 Power factor correction

Switch mode power supplies (SMPSs) connected to the power line, deliver electric power to loads from the line by rectifying AC voltage (V_{in}) into DC voltage and, depending on applications, converting the DC voltage into either AC voltage again by an inverter or a DC voltage with different level through a converter to suit the loads [3-1] [3-2]. Conventionally, a rectifier implemented by a diode-bridge is employed to achieve the conversion and a capacitor input filter is used to reduce the ripple of the DC voltage, as shown in Figure 3.1. In this configuration, voltage on the input capacitor C_{in}, V_{Cin}, will stay at approximately the peak value of the AC input voltage and current is drawn from the input only when the instantaneous line voltage is higher than V_{Cin}. As a result, the input current waveform is a short pulse with high amplitude, as illustrated in Figure 3.2. To make things worse, the holdup time requirements, which is important in AC/DC applications to power the load in case of line drop-out, demand a larger C_{in} than the needed value for filtering and further reduces input current conduction angle and increases the current peak. The distorted input current of a SMPS is in phase with the line voltage and it contains rich odd-order harmonics which causes the power factor (PF) to be as low as 0.5~0.65 [3-3] [3-4]. The distorted input current of a SMPS causes inefficient power utilization which

means additional power is needed to run the system, imposing some cost and lifetime burdens in power generation and distribution facilities [3-5].

A variety of standards and regulations on performance of SMPSs have been issued to combat the problems introduced by current distortions. In EU, the standard of EN61000-3-2 limits maximum allowed amplitude of line-frequency harmonics up to 39th harmonic for application with input currents less than or equal to 16 A. The legislation, in fact, specifies harmonic limitations in four classes of equipment: A, B, C for appliances, power tools, and lighting respectively, and D for PCs, computer monitors, and TVs rated between 75 and 600 W [3-6]. In US (United States), Energy Star program demands a PF of at least 0.9 at 100% of rated output on external SMPSs with a nameplate output power greater than or equal to 75 W [3-7]. In other countries, such as China, Japan, etc., harmonic current regulations have also been developed, which are evolved from EN 61000-3-2 [3-8].

Power Factor Correction (PFC) technique, which shapes input current of a SMPS to smooth out the current peak so that input current is a replica of the input voltage, is capable of making a SMPS satisfying all the aforementioned regulations simultaneously and therefore is commonly applied in SMPSs [3-1] [3-5]. In this thesis, PFC technique employed in AC/DC SMPSs which are widely used in applications such as laptop adaptors, LED drivers, etc., is investigated. The AC/DC converters has a DC-DC stage cascaded with the PFC stage and, given the fact that DC-DC stage provides both regulation and isolation, only non-isolated PFC technique is considered [3-9].

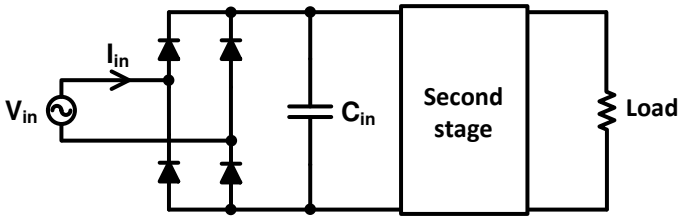


Figure 3.1 Capacitor-filtered AC/DC converter

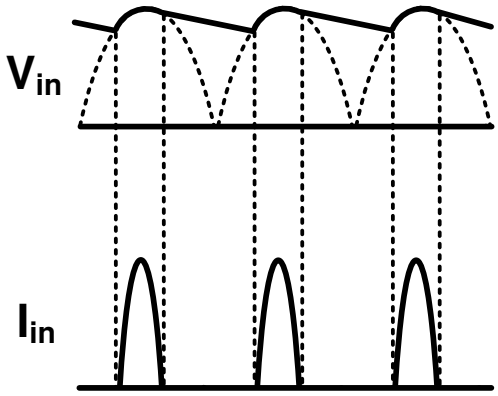


Figure 3.2 Waveforms of capacitor-filtered AC/DC converter

3.2.2 Types of PFC technique

Generally speaking, two different kinds of solutions exist to actualize PFC, namely passive and active, and a variety of choices are available within each type.

Passive PFC techniques, as the name implies, utilizes passive components to spread the input current out through the whole operation cycle so that current harmonics are reduced. Many different types of passive solutions were proposed, ranging from simple input passive filter (implemented in either AC-side or DC-side [3-10]) to resonant passive filters (connected with rectifier input either in series or in parallel [3-11]), to remove the most prominent harmonic content (3^{rd} harmonic), of which the simplest solution was to place a proper inductor between the rectifier and the filter capacitor to reduce input current peak and extend current conduction time well enough so that the regulations can be met [3-5][3-12]. The developed passive solutions have shared merits such as simple to implement, reliable, etc. while they also have common demerits such as large size and weight, not suitable for universal line voltage (90~265V_{ac}, 50/60 Hz) that prohibit them from wide applications in commercial products [3-5] [3-9] [3-11].

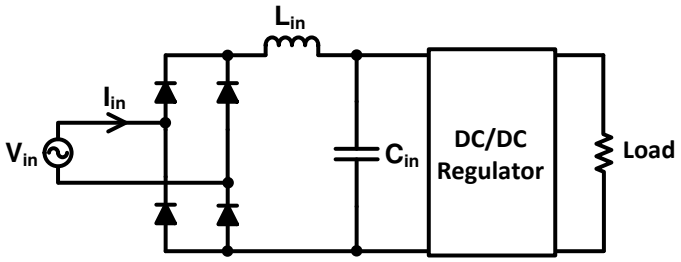


Figure 3.3 Simplest passive solution

Active PFC techniques employ either active filter or switch-mode converters, DC-DC converters in most cases, to shape the input current. And accordingly, there are two different kinds of active solutions for actualizing PFC: active filtering method, and DC-DC converter current shaping method [3-13]:

- *Active filters* inserted between input and diode-bridge implemented by transistors, sometimes combined with passive components, with proper control schemes have been developed to filter out input current harmonics in a SMPS [3-13]. Two types of active filters, of which basic principles differs from each other, exist: parallel active filters (in parallel with harmonic source, as introduced in [3-14]) compensate harmonic current by injecting a current of the same amplitude but reverse phase to input side while series active filters (in series with harmonic source, as discussed in [3-15]) isolate harmonic current by presenting high impedance and blocking the current from flowing between input and harmonic source[3-12][3-14][3-15].
- *DC-DC converters* interposed between diode-bridge and smoothing capacitor, utilizing active switches (together with proper control schemes) and passive components, force the input current to be direct instantons proportional to the input voltage so that input current, at least in a large portion of one line cycle, would be a replica of input voltage and thus making current waveform in-phase with that of voltage and eliminating harmonics i.e. achieving unity PF [3-5] [3-12]. Although harmonic content in capacitor-charging current is minimized, as these DC-DC converters usually operate at frequencies much higher than line frequency i.e. high slew rate of current and voltage, the converters also behave as sources of Electromagnetic interferences (EMI) [3-16]-[3-18]. The EMI has to be minimized because: a) it may lead to

problems such as malfunction of transistor control circuitry, interfering surrounding equipment, etc. [3-19]; b) there are EMI standards that a SMPS need to comply e.g. EN55022 and CISPR22 [3-20] [3-21]. Apart from the needed actions to mitigate EMI problem in the design of the DC-DC converter e.g. reducing stray capacitance, minimizing parasitic inductance, controlling rate of switching current with snubbers, etc., EMI filters are commonly adopted in SMPSs, as illustrated in Figure 3.4 [3-17] [3-22].

A variety of DC-DC converter topologies has been investigated to implement PFC, ranging from existing topologies to newly proposed ones, from basic topologies to hybrid/combined ones, etc., each with their benefits and drawbacks. Depending on requirements of applications, as will be discussed in 3.3.4, choices of PFC converter differ.

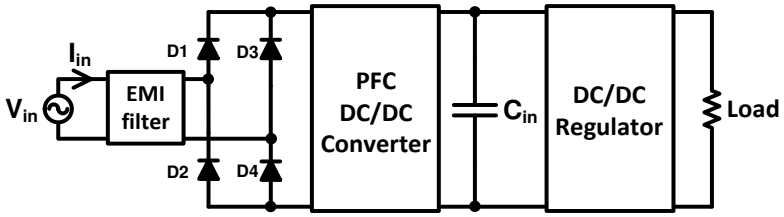


Figure 3.4 A typical AC/DC SMPS

Compared with passive approaches, active PFC solutions are more compact and suitable for universal line applications, at the expense of higher cost, which is not likely to be decisive even in cost-sensitive applications given recent market trend of rising cost of copper and magnetics and falling cost of semiconductors [3-5] [3-9]. Of the two different types of active PFC techniques, active filters are rarely used in commercial applications because of the fact that at least four transistors and their attendant circuitries for control and driving are demanded, which makes the systems high cost, high complexity and low reliability [3-9] [3-12]. DC-DC converters, on the other hand, are widely adopted as fewer transistors are needed and performance is better, especially with the availability of specialized IC (Integrated Circuit) for realizing PFC function of the converter [3-9] [3-23] [3-24].

It should be noted that there are some approaches for achieving PFC which do not belong to any of the aforementioned groups such as AC-DC converter current shaping method [3-25], combined passive and active filtering method [3-26], etc. These approaches seldom investigated as they involve sophisticated design and are relatively difficult to realize. Moreover, performance of the approaches, in terms of power factor improvement, is not superior to that of DC-DC converters. And therefore, these approaches are not considered in this thesis.

3.3 Overview of PFC converters

The architecture of a SMPS illustrated in Figure 3.4, where front-end PFC stage ensures a high PF and establishes a loosely regulated DC bus voltage while downstream DC-DC stage provides isolation and a tightly regulated output voltage, is usually termed as two-stage AC/DC converter in that the two stages are separated and independently controlled. There are, in fact, also single-stage AC/DC converters where the circuitries of PFC stage and DC-DC regulation are combined together so that

input current shaping, isolation and regulation of outputs are achieved in one stage using one switch (or sometimes, one set of switches [3-27]) under control of one signal [3-28]-[3-31]. Compared with two-stage solutions, PFC function are supposed to be naturally achieved i.e. PFC switch and corresponding controller for PFC stage are eliminated in single-stage AC/DC converters and therefore, cost and complexity of the system are expected to be lower [3-32] [3-33]. In practice, boost converter integrated with Flyback (BIFRED) is the most popular single-stage topologies because of its simplicity, although there are also other options like boost integrated with Forward [3-34], buck integrated with buck-boost [3-35], Sheppard-Taylor [3-27], etc. The topologies, however, have shared problems that prohibit them from being widely applied in PFC:

- Applicable power range of single-stage AC/DC converters are limited. In almost all single-stage topologies, the single switch handles both the PFC current and the dc/dc current i.e. the switch is subjected to high current stress [3-35]- [3-37]. And therefore, single-stage approaches have been employed mainly in low power applications (<100W) such as LED drivers, ballast circuits and low-power battery chargers, etc. so that components with higher current rating (and higher cost) remains affordable [3-28] [3-39] [3-40].
- High voltage, large value smoothing capacitors are demanded. In single-stage AC/DC converters, DC voltage on the energy storage capacitor, which is indispensable for both buffering imbalance of instantaneous power between AC source and output load and fulfilling hold-up time requirement, is no longer regulated and the voltage varies with line and load. The varying DC voltage has detrimental effect on the required value, eventually size and cost, of the capacitor to meet hold-up time requirement. Moreover, as the storage capacitor balances instantaneous input and output power, in many single-stage topologies DC voltage across it can be extremely high (up to 1kV [3-36] [3-40] [3-41]) at light load, which is highly undesirable. Actions can be taken to suppress the high voltage stress e.g. through voltage feedback concept [3-32], auxiliary circuit [3-31] [3-37] [3-42], variable frequency control [3-34][3-36] , etc. , at the expense of added complexity and cost , which diminish the benefits of single-stage approaches.

The undesirable demand of high voltage and/or large value storage capacitor, and therefore, is regarded as the main obstacle that prohibits single-phase PFC solutions from wide application [3-34] [3-41]. The emerging GaN devices, as introduced in chapter 2, could have lower R_{dson} than Si counterparts with the same blocking voltage capacity and therefore are promising for pushing up power of single-stage AC/DC schemes. The main issue of single-stage AC/DC solutions, however, cannot be eased by the new semiconductor technology.

Two-stage AC/DC converters, as already discussed, have a cascade structure of one DC-DC converter to realize PFC (termed as PFC preregulator in this thesis) and one DC-DC converter to achieve regulation and isolation of output (termed as voltage regulator in this thesis). Two-stage AC/DC converters are commonly used as they have better performance over single-stage ones in terms of efficiency, THD reduction, dynamic response and cost-effectiveness, especially in higher power (>100W) applications [3-28] [3-38]. Many different converter topologies have been used as a

preregulator, of which maintaining both high PF and high efficiency across the entire load and input voltage range is the main challenge [3-3]. The challenge can be translated into different design and application concerns in different topologies depending on various factors such as cost, simplicity, form factor, etc. Besides, choice of the PFC topology affects design and implementation of other parts such as size of EMI filter; diode bridge, design and implementation of the downstream DC-DC converter, etc. in a two-stage AC/DC converter, and therefore, interactions between PFC topologies with these parts should also be considered in implementing the AC/DC converter.

At present, boost converter is the most popular topology for actualizing PFC among many others, all with Si devices applied [3-9] [3-22]. In this section, topologies that have been developed for implementing PFC stage in low-power two-stage AC/DC converters are reviewed to reveal pros and cons of each topology and examining the major features that makes one topology preferable (in case of boost) or undesirable (in case of other topologies) for industrial applications. Moreover, identification of whether the features are semiconductor-technology related or not are carried out, with the purpose of investigating the influence of the GaN technology on choice of topology for implementing PFC.

3.3.1 Common properties of DC-DC converters for implementing PFC

Broadly, according to conversion characteristics between input voltage and output voltage, existing topologies that have been used as PFC preregulators can be categorized into three groups: step-up, step-down and step-up/step-down. Each group of topologies were developed from one of the three most basic DC-DC topologies (boost, buck and buck-boost) and the developments were driven by need of performance improvements in many different aspects such as efficiency improvement, PF increment, etc. There are, in fact, a few shared properties when these topologies are used as PFC preregulators:

- The PFC regulator operates at a frequency much higher than the line and the active switch(es) is controlled in such a way that input current of the regulator varies in direct instantaneous proportion to the input voltage in at least part of a switching cycle [3-5] [3-44].
- Apart from the shaping of input current i.e. current shaping, output voltage is also regulated. And therefore, unlike in single-stage AC/DC converters, constant output voltage, is maintained on the smoothing capacitor.
- Theoretically, all the developed topologies could work in different operation modes such as CCM, DCM and BCM, and, in fact, many topologies had been successfully operated in different operation modes. Different operation modes not only provide different switching and conduction conditions of switches in the topologies, as will be elaborated in chapter 5, but also affects design and implementation of other parts such as EMI filter, control schemes, sensing approaches, etc. In this section, the influences of different operation modes on topological selection are not considered because: a) characteristics of one topology that are critical for PFC application, as will be shown later, are dependent mainly on the specific topology itself rather than on the operating mode; b) with very few properties important for implementing PFC that are affected by operation modes, the influences show similar trend in different topologies.

For example, it has been well demonstrated that in all three different types of PFC topologies, CCM operation would result in smaller DM filter compared to DCM, in which mode inherent current shaping can be achieved i.e. control and sensing tasks are eased [3-5] [3-45]-[3-53].

- Maximizing efficiency while complying with harmonic current limits is a general goal of the topologies, although there are also examples of improving performances in other aspects such as optimal design of inductive parts, simplifying control algorithms, etc. [3-45] [3-54] [3-55].

In the following sections where different topologies are introduced, only CCM operation is used for illustrating operation principles. Besides, it should be noted that the waveforms are only demonstrative as they are not showing exact reality e.g. switching frequency is much higher than line frequency (at least tens of kHz compared to tens of Hz) in real applications.

3.3.2 Step-up DC-DC converters as PFC preregulators

A step-up preregulator topology, as the name implies, produces a higher output voltage than the input voltage. The output voltage, as SMPSs are usually designed for universal line inputs (90 V_{ac} ~265V_{ac}), is usually no less than 380V. Of the step-up PFC preregulator topologies, boost converter is the most basic one and the rest ones can be regarded as variations or modifications of the boost converter.

3.3.2.1 Boost converter as PFC preregulator

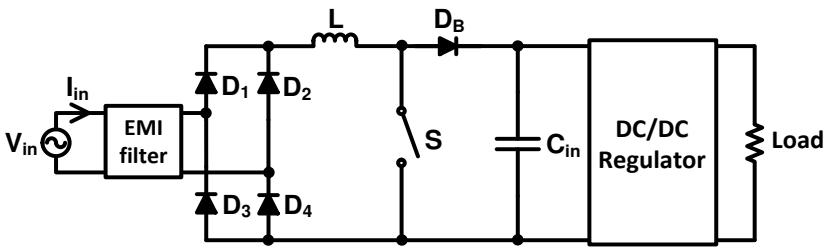


Figure 3.5 AC-DC converter with boost converter as PFC preregulator

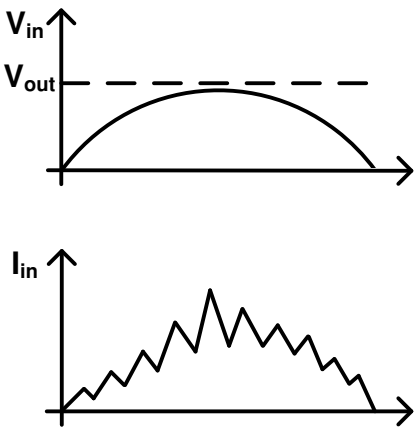


Figure 3.6 Waveforms of boost PFC preregulator in CCM

In theory, when a boost converter is used as a PFC preregulator, the converter can operate through an entire universal input half line-cycle i.e. input current can be shaped in the whole cycle, as long as

the output voltage is properly set, as shown in Figure 3.6. And therefore, theoretically, unity power factor can be achieved regardless of is operation modes, control methods, etc. Due to the unnecessity of achieving very high PF to meet the regulators and practical issues such as trade-offs between PF and efficiency, close-to-unity PF instead of unity PF are commonly achieved in PFC boost converters [3-9] [3-56]. The satisfactory high PF, in fact, is achieved in a simple way. As one of the most basic DC-DC topologies, a boost converter calls for minimum number of components to implement and, when used as a PFC preregulator, circuit locations of components in the converter also brings benefits: the transistor is easy to drive given the fact that it is grounded; input current is not switched which is beneficial for EM noise suppression; the boost inductors absorbs line spikes and thus increases reliability of the AC/DC converter [3-44].

Although PFC boost converter has distinguished characteristics of inherent current shaping and simplicity that makes it the most preferred one, the demerit of high output voltage hinders the topology from being applied as a PFC preregulator in some applications. The output voltage of a PFC boost converter, which has to be set higher than the peak of the high line, has detrimental effect on loss of the switching device and thereby efficiency of the converter, especially in hard switching. In fact, as being pointed out by many, a PFC boost converter would have lower efficiency at low line compared to that at high line. Drop of efficiency is attribute to increased input current with a high voltage that leads to higher losses in the switching device [3-45] [3-57] [3-59].

3.3.2.2 Variations of boost converter as PFC preregulator

Variations of the basic PFC boost converters have been developed for the purpose of improving performance of the PFC stage or even performance of a whole AC/DC converter. Among many different modifications of the basic PFC boost converter, bridgeless PFC boost converters and interleaved PFC boost converter are the two typical topologies that have been investigated to achieve loss reduction, high efficiency and high power density at the same time, respectively.

Bridgeless PFC boost converters

Bridgeless PFC boost converters were developed to reduce conduction loss of the bridge rectifier and improve efficiency of the AC-DC converter. Traditionally, as was introduced in 3.2.1, a diode-bridge preceding the PFC stage rectifies the AC input voltage into a DC sinusoidal voltage. The rectifying is made possible as diodes D1 and D4 (in Figure 3.4) conducts in positive half line while D2 and D3 (in Figure 3.4) takes over the conduction in negative half line. And therefore, the input current has to flow through two diodes before being processed by the PFC stage, which leads to conduction loss. As illustrated by one of the basic bridgeless PFC boost converters shown in Figure 3.7**,** bridgeless PFC boost converters combine the conventionally separated diode bridge and PFC boost converter together, so that one diode in line current path is eliminated. In the exampled bridgeless PFC boost converter, D_1 and S_1 in positive half line cycle while D_2 and S_2 in negative half line cycle. In each half line cycle, body diode of the inactive transistor is utilized. As the number of diodes in line current path is reduced, conduction loss of the AC/DC converter, therefore, is decreased [3-60] [3-61].

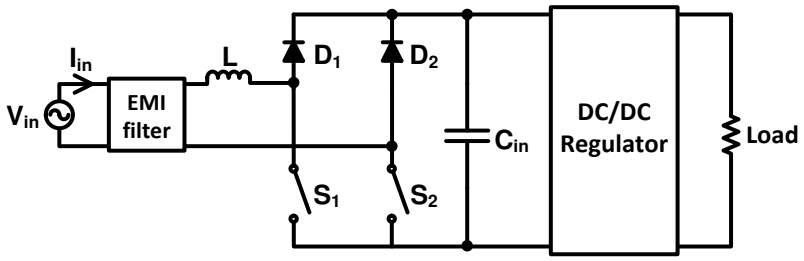


Figure 3.7 Bridgeless PFC boost converter

The basic bridgeless PFC boost converters, however, have significant CM noise that makes them not a practical solution. Different from the conventional PFC boost converter where the output ground is always connected to AC source ground through diodes of the bridge rectifier, the ground of the output in a basic bridgeless PFC boost converter is a floating one: in positive half line cycle, output ground is connected to AC source ground through the body diode of S_2; in negative half line cycle, output ground is pulsating with an amplitude equal to output voltage and a high frequency the same as the switching frequency of the transistors. This high frequency pulsating high voltage source charges and discharges parasitic capacitance between output ground and AC line ground, producing significant CM and imposing great difficulty in EMI filter design. Besides, compared with the basic PFC boost converter, two transistors are needed instead of one and so does the control circuitry. The benefit brought by the fact that one diode is eliminated is diminished by the needed additional parts, from cost point of view.

Modifications of the basic bridgeless PFC boost converters have been investigated to suppress the CM noise of the converters while maintaining low conduction loss. Basically, the modified bridgeless PFC boost converters were designed to provide low-frequency path between AC source ground and positive or negative terminal of the output [3-22]. Although EMI performance of the modified bridgeless PFC converters such as a basic bridgeless PFC boost converter employing bidirectional switch, basic bridgeless PFC boost converter with two dc/dc boost circuits, etc., can be improved for practical application, complicated control schemes are required and extra components are needed, which makes the solutions more difficult to implement and less cost-effective compared to the PFC boost converter.

Interleaved PFC boost converters

Interleaving two or more boost converters as PFC preregulator has been proved as an effective approach to achieve both high efficiency and high power density of PFC preregulators at the same time [3-62]. In essence, interleaving converters, as demonstrated by a PFC preregulator with two interleaved boost converters, are paralleling identical converters together so that current, and power thereof, handling capabilities can be increased [3-62]. Compared to the basic PFC boost converter, benefits of the interleaved PFC boost converter can be summarized as:

- As multiple paralleled converters share input current, lower loss can be expected at the same power level or more power can be processed with satisfying efficiency maintained.

- Since switching instances of the transistors are phase shifted in the identical converters, current ripple reduction is achieved in both input and output. When the same current ripple is assumed in both a basic PFC boost converter and an interleaved PFC boost converter, size reduction of DM filter and ESR related loss reduction in output capacitor is possible.
- For the same operation frequency of the overall PFC stage, switching frequency of a single converter in a interleaved PFC boost converter is effectively increased, which further decreases size of the CM filter and, together with approaches such as coupling the inductors, downsize of the boost choke can also be achieved.

The interleaved PFC boost converters are mainly applied in CCM/DCM boundary mode, in which mode a basic PFC boost converter has high efficiency but large current ripple, so that the benefits of the technique can be maximized, although there are also examples of CCM mode ones [3-62] and DCM mode ones [3-63] [3-64]. Despite the benefits the interleaved PFC converters bring, the topology also has drawbacks that make it less attractive for industrial application:

- The topology calls for complicated control approaches, which makes it difficult to implement. As multiple paralleled converters need to be controlled in such a way that each converter is switched at its own rhythm while at the same time stay synchronized to the rest ones, sophisticated control schemes are required, especially in the most commonly applied CCM/DCM boundary mode where switching frequency varies in half-line cycle.
- The topology requires large component count, leading to high material and assembly cost and low reliability.

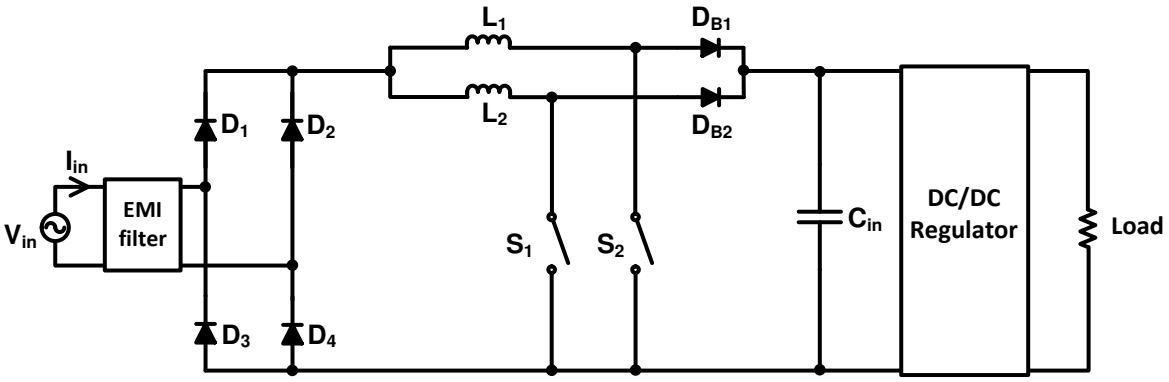


Figure 3.8 Interleaving two boost converters as PFC preregulator

Apart from bridgeless PFC boost converters and interleaved PFC boost converters, there are also other variations of the basic PFC boost converter such as bridgeless interleaved PFC boost converter [3-65], basic PFC boost converter with different types of snubber circuits to reduce transistor switching loss [3-22], etc., of which the main purpose is to improve efficiency of the PFC stage. These topologies have larger component count and calls for advanced control methods (for bridgeless interleaved boost converters and boost converters with active snubbers), and therefore are less cost-effective, less reliable and less convenient to implement than the basic boost converter.

3.3.2.3 Summary

To summarize, of the step-up PFC DC-DC converters, boost is the most basic one and others are essentially variations of the boost converter, of which performance improvement is the common goal.

- Boost converter is the most commonly used topology as preregulator mainly because of its simplicity and satisfactory current shaping performance, although it suffers from low efficiency in low input line conditions.
- Bridgeless boost converter combines a PFC boost converter with the preceding bridge rectifier so that number of semiconductors in input current path is reduced and conduction loss of the AC/DC is lowered. Unfortunately, due to the nature of the topology, significant CM noise would be generated, which is not practically acceptable.
- Interleaved boost converter enable higher efficiency and high power density of the AC/DC converter by effectively increasing switching frequency and reducing current amplitude and ripple of paralleled boost converters so that size of EMI filter and boost chokes can be minimized and switching and conduction loss of semiconductors, magnetic parts and capacitive parts can be reduced. The topology, however, calls for large component count and sophisticated control schemes resulting in high cost and complexity.

3.3.3 Step-down DC-DC converters as PFC preregulators

Step-down DC-DC converters used for PFC stage, similar to the step-up counterparts, also follow the trend that the basic step-down converter i.e. buck converter is the initial and basic one in this group and the rest ones are, in fact, variations or modifications of the buck converter to improve performance of the AC/DC converter with a buck type converter as PFC preregulator. Due to the step-down nature, output voltages in these converters are all set at a level that is less than the peak AC voltage at low line (90 V_{ac}), so that the converter can function in at least part of a half-line cycle under the universal input conditions.

3.3.3.1 Buck converter as PFC preregulator

When a buck converter is used as a PFC preregulator, it only operates partly in a half-line cycle: when instantaneous rectified AC voltage is greater than the output bus voltage, PFC stage is active and current is drawn from the input; when the rectified AC voltage is lower than the output voltage, the PFC stage is inactive and no power is drawn from the AC line. Hence, there are dead angles in input current waveforms around zero crossings of the rectified AC voltage where the current is not shaped, leading to a so-called “cross-over” distortion in line current. The resulting conduction angle, as shown in Figure 3.10, is a function of both the rectified AC voltage and output voltage and, with universal line input, a lower output voltage would lead to less line current distortion. Lower output voltage, on the other hand, would mean higher inductor current and higher switching current i.e. lower efficiency of the PFC stage [3-66] [3-67]. And therefore, a trade-off exists between distortion of input current and efficiency of the PFC stage. Choice of the output bus voltage, accordingly, is regarded as the most important design parameter for PFC buck converter [3-45] [3-58] [3-68]. Even the properly designed PFC buck converters, however, are not widely used in AC/DC applications mainly because:

- The “cross-over” distorts input current and causes high THD and low PF, especially at low line input. The inherent current distortion limits practicability of buck converter as a PFC preregulator as either additional circuitry and complex control methods might be needed to make sure that harmonic standards can be met [3-57] [3-66] [3-70] or the input power has to be confined to low power range [3-57] [3-58] [3-69].
- High side driving of the transistor and/or bus voltage sensing, which are not preferable in applications, are needed [3-58] [3-67].

Consequentially, very limited number of ICs has been developed to implement buck converters as PFC preregulators [3-24]. Although there are many publications addressing advantages of PFC buck converter technology, the potential benefits that the technology could bring are, in fact, limited:

- Low voltage swing across the transistor. Voltage swing in a PFC buck converter is smaller compared to that in a PFC boost converter leading to less CM noise and ease the task of corresponding filter design [3-45] [3-70]. Since voltage of the transistor in a buck converter is clamped to input i.e. maximum voltage is peak voltage of high line input (375V) and output voltage of a PFC boost converter device is set to be higher than peak voltage of high line input (380V~400V), the gain in CM filter design and the freedom in selection of transistor, compared to those in boost converter, is limited.
- Inherent current limitation capability. In a PFC buck converter, the switch is located between the input and the smoothing capacitor; input inrush current during start up can be controlled. This capacity was considered as a critical property over boost converter where uncontrolled direct path exists between input and output and are emphasized by many [3-59] [3-71] [3-72]. Although it is true that the direct path between input and output in a boost converter would lead to large inrush current at start-up, the addressed potential of damage of PFC stage may not happen given the fact that the current peak only occurs for a short time [3-73] [3-74]. Moreover, care has been taken in PFC boost converter to avoid possible failure caused by the inrush current, of which the solutions are quite simple [3-74] [3-73] [3-75]. And therefore, the merit of inherent inrush current control in buck converter is not so appealing as promoted.

It should be noted that, although it was mentioned by many that, when used as PFC preregulator, buck converter would have higher efficiency than a boost converter in low line conditions, very limited work have been performed to prove and demonstrate the potential. In available examples on efficiency comparisons between PFC buck converters and PFC boost converters, depending on many different issues such as operation modes selected, components selection approach, etc., the conclusions differ. In [3-71], performances of a PFC buck converter and a PFC boost converter, both in BCM, are compared using two prototypes of 100W, and it was showed that in low line ($<170V_{ac}$) PFC buck converter has a higher efficiency than the boost counterpart, while with higher input line ($170V_{ac}$~$270V_{ac}$), the trend was reversed. In [3-45], a 94W PFC buck converter with clamped current control was evaluated with respect to a PFC boost converter in BCM with the same power at $100V_{ac}$ input, and it was revealed that: a) buck converter has higher loss than boost converter in PFC stage; b) loss in diode bridge and EMI filter would be larger if buck converter rather than boost converter is

applied as preregulator; c) overall efficiency of the buck based “EMI filter-diode bridge-PFC” system is higher than the boost based. Besides, differences of low line efficiency between PFC buck converter and PFC boost converter in both examples are limited, which makes the results less convincing given the existence of measurement or calculation errors: in 100W prototypes, maximum efficiency difference is ~1% and in 94W comparisons, efficiency gap is 0.83%. And therefore, in this thesis, the possible benefits of buck converter in measures of low line efficiency, as assumed by many [3-66] [3-70]-[3-72], is not considered.

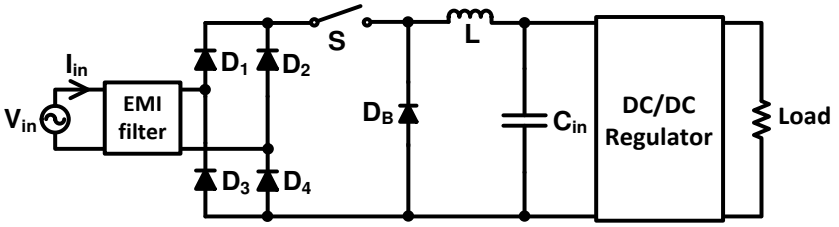


Figure 3.9 AC-DC converter with buck converter as PFC preregulator

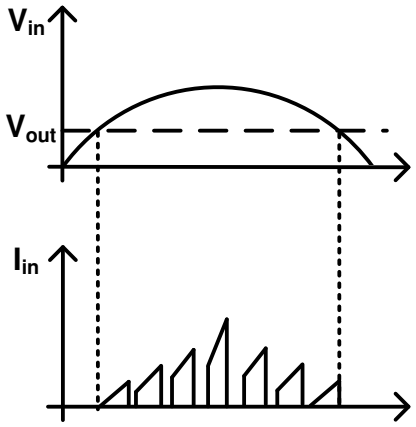


Figure 3.10 Waveforms of buck PFC preregulator in CCM

3.3.3.2 Variations of buck converter as PFC preregulator

Efforts on improving performance of PFC buck converter has been devoted to many different aspects, such as maximizing efficiency of the converter while keeping harmonic current in control, combating the discussed drawbacks of the converter, etc. These efforts have resulted in topological modifications and variations of the basic PFC buck converter. In this section, representative modified buck converter as PFC preregulators, namely PFC buck converters with low side transistor, bridgeless PFC buck converters and interleaved PFC buck converters are introduced.

PFC buck converter with low side transistor

Repositioning the transistor in the buck converter, as has been discussed in [3-71] and implemented in [3-66], could help to avoid the undesirable high-side driving need and allows easier and more robust design of the PFC stage. The modification, however, leads to a floating output bus voltage, which makes sensing and control circuitry of the downstream DC-DC converter challenging and the AC/DC converter as a whole more complicated [3-72].

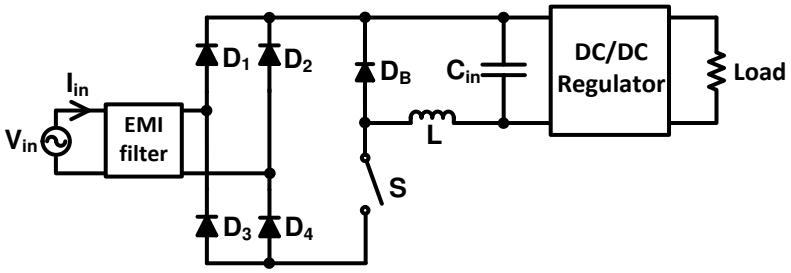


Figure 3.11 PFC buck converter with low-side transistor

Bridgeless PFC buck converters

Similar to the concept of bridgeless PFC boost converter, bridgeless PFC buck converter reduces loss of a AC/DC converter through minimization of the number of simultaneously conducting semiconductor components. Several different bridgeless PFC buck topologies have been investigated, with the one illustrated in Figure 3.12 as the original [3-68] [3-76]. The PFC buck converter in Figure 3.12 combines two buck converters (back-to-back connected) with the diode bridge. The two back converters functions alternatively in one line cycle: the upper buck converter, as demonstrated in Figure 3.13 (a), is active during positive half cycles of input regulating an output voltage on capacitor C_{in1} while the lower buck converter operates in negative half cycles of input with an output voltage on capacitor C_{in2}. Output voltage of the bridgeless PFC buck converter, therefore, is two times the output voltage of one sub-converter [3-68].

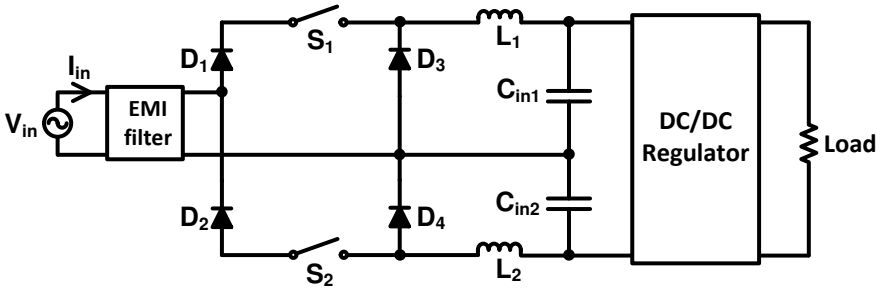
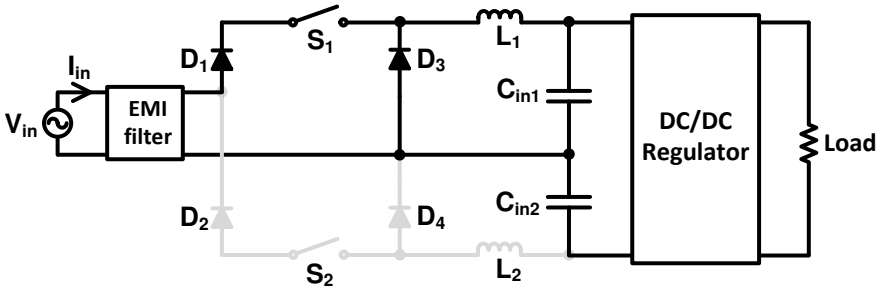
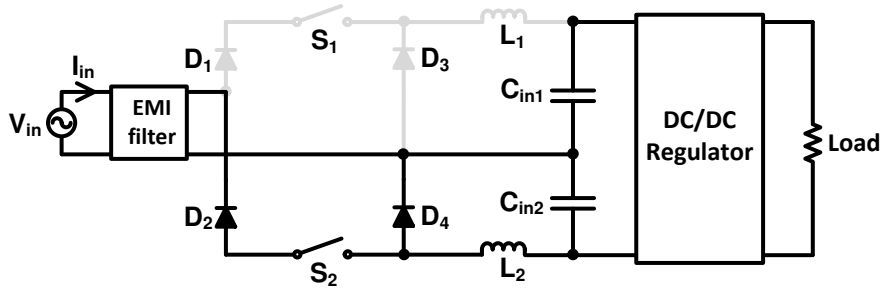


Figure 3.12 Bridgeless PFC buck converter



(a)



(b)

Figure 3.13 Operation of bridgeless buck PFC converter during the positive line voltage (a) and negative line voltage (b).

Apart from the benefit that number of diodes in current conduction paths are reduced and efficiency is improved, the bridgeless buck PFC also features as a voltage doubler as the output voltage is two times the output voltage of each buck converter [3-68]. And therefore, with the same output voltage specifications, bridgeless PFC buck converter have larger conduction angle in input current, and better PF thereof, as voltage in each sub-converter is halved, compared to the basic PFC buck converter. Despite of the benefits of improved efficiency and PF, bridgeless buck converter requires two transistors and corresponding control and sensing circuitry, which translates into increased cost and complexity than the basic buck converter. Besides, the unfavourable need of high-side driving has to be satisfied.

Research on improving performance of PFC buck converters has also been conducted to compensate the inherent dead time in input current, the essence of which is to add extra circuitry to the buck converter so that the modified converters could operate as a step-up one when input voltage is lower than the output voltage and a buck in the rest of one half-line cycle, which are categorized as step-up/step-down topologies in this thesis and will be elaborated in 3.3.4. Besides, there are also variations like interleaved PFC buck converter [3-77], interleaved bridgeless PFC buck converter [3-78], each with very limited examples of its spice. Both of the converters are helpful in improving efficiency, increasing power scaling capability and reducing size of EMI filter of the buck converter in PFC stage, at the expense of greatly increased component count and, consequentially, increased cost, complicity and reduced reliability.

3.3.3.3 Summary

Step-down DC-DC converters used for implementing PFC are basically buck converter and its variations.

- With buck converter, line current is not shaped during intervals when line voltage is lower than the output voltage. The inherent input current distortions, together with the need of high side driving and high side sensing techniques and the demand and lightning surge management, inhibit buck converter from being widely applied in PFC.
- Modified versions of the basic PFC buck converters all have reserved the benefit of the topology such as low output voltage, inrush current limit capability, low voltage swing across

transistor, and can help to elevate performance from different aspects, the modifications also introduce problems.

- Repositioning the transistor to a low side one eases design for driving and sensing of a PFC buck converter but producing a floating output voltage and imposing challenges on sensing and control circuitry in downstream DC-DC converters.
- Bridgeless PFC buck converter, which merges two buck converters together with the diode bridge into one, not only reduces loss of a AC/DC converter by reducing number of semiconductors in input current path but also enables better PF as output voltage in each buck converter can be halved with the same output voltage requirement on the PFC buck converter and dead time in input current can be reduced. With bridgeless PFC buck converter, on the other hand, the demerit of high side driving still exist. Besides, two transistors and their auxiliary circuitries are demanded to fulfill the concept, leading to increased cost and complexity.

3.3.4 Step-up/Step-down PFC topologies

As discussed in 3.3.1 and 3.3.2, step-up PFC topologies features input current shaping property throughout a whole half-line cycle but with high output voltage, which has negative effect on transistor loss, CM noise and design of downstream DC-DC converter, while step-down PFC topologies enables lower output voltage but has lower PF due to inherent dead time in input current. Step-up/step-down PFC topologies are developed, as a matter of fact, to have step-up and step-down function in one converter so that benefits of both step-up and step-down topologies can be maintained whereas some drawbacks of the topologies are eliminated. Essentially, the step-up/step-down PFC converters operates as a boost PFC when input voltage is lower than the output voltage and functions as a buck converter in the rest part of a half-line cycle so that, theoretically, input current can be shaped across the whole line and load conations and output voltage is regulated at a low level.

Step-up/Step-down topologies that have been investigated to implement PFC stage ranges from existing ones e.g. buck-boost, cuk, etc. to newly proposed ones e.g. buck-boost in cascade structure, integrating buck with buck-boost, etc., of which buck-boost converter is the simplest one.

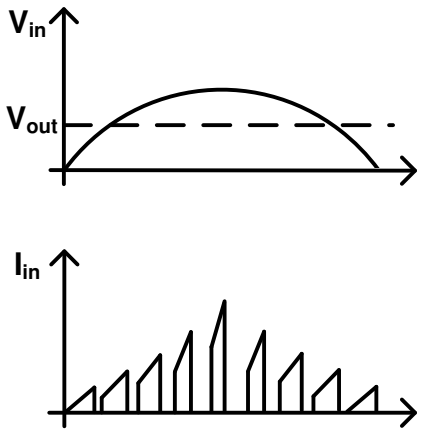


Figure 3.14 Waveforms of step-up/step-down preregulator in CCM

3.3.4.1 Single-switch step-up/step-down PFC preregulators

Single-switch step-up/step-down PFC DC-DC converters, depending on specific electrical criteria considered, can be grouped in many different ways e.g. isolated ones and non-isolated ones, inverting ones and non-inverting ones, etc. [3-79] [3-80]. In this section, the converters are, from topological point of view, categorized as the step-up/step-down converter i.e. buck-boost converter and its variants.

Buck-boost converter as PFC preregulator

When a buck-boost converter is used in the PFC stage, similar to a PFC boost converter, input current can be shaped in a whole input cycle and, theoretically, unity power factor can be obtained by through proper control. The buck-boost PFC converter, however, produces an output voltage, which can be either higher or lower than input voltage, with negative-polarity in respect of the common terminal at input [3-79] [3-80]. Moreover, as indicated by Figure 3.15, high side driving of the transistor and, in some cases, high side sensing is needed in a buck-boost converter. Despite of the fact that, in comparison to that of a boost converter, a lower output voltage on the smoothing capacitor, higher voltage stress is imposed on the transistor calling for high voltage device and leading to increased loss and cost [3-81]. Similar to the boost and buck when used in PFC, variations of the buck-boost converter were developed to improve performance of the PFC stage, or even the whole AC/DC converter such as efficiency, power scaling capacity, etc., at the price of increased cost and complexity and reduced reliability [3-82]-[2-84]. The unfavourable feature of inverting output in the buck-boost topology, however, has not been well dealt with and the achievement of non-inverting output were mainly made as by-products of efficiency improvement in its variations [3-85]. Due to the demerits of the topology, it is hardly applied in industrial products.

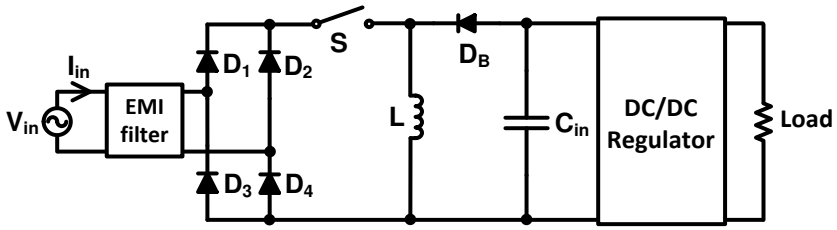


Figure 3.15 Buck-boost converter as PFC preregulator

Variants of buck-boost converter

Many other single-switch step-up/step-down converters have been proved capable of implementing PFC, of which Cuk, SEPIC, Zeta and Flyback are typical examples. The converters are generally considered as buck-boost variants as they can be topologically derived from buck-boost through basic electric circuit theories such as duality principle, electrical isolation mechanisms, etc. [3-79] [3-80]. Demonstrations on design and implementation of these converters in PFC stage have been performed, each with pros and cons [3-86]-[3-89]. Performance improvements of these converters were carried out mainly to increase efficiency through approaches such as reducing conduction loss by making the AC-DC converter bridgeless [3-90]-[3-92], achieving soft switching of the converters by adding extra

components in circuits and proper control [3-93]-[3-96]. Focuses of other variations of these converters in application of PFC was devoted to several different aspects such as increase power handling capacity, reduction of electrical stress on transistors, etc. [3-97] [3-98]. These variants basically function as the buck-boost, but with benefits such as non-inverting output, inherent electrical isolation, etc., with the sacrifice of increased component count, and consequentially, high cost and complexity and low reliability.

The variants of buck-boost converter, like the basic buck-boost, suffer from high electrical stress, both current and voltage, in transistors because, unlike the boost or the buck where the input power is transferred partially directly to the output without being processed, there's no direct path for power delivery in the buck-boost and its variants. All the input power has to be processed through switching devices, resulting in high component stress, low efficiency [3-99] [3-100]. Moreover, requirement of energy storage in buck-boost and its variants are high as all the input power must be stored before being processed. Although there had been efforts to ease electrical stress through approaches such as paralleling, multilevel technique, etc., reduction of both voltage and current stress simultaneously has not been achieved as the fundamental problem of lacking direct power transfer mechanism were not solved [3-99] [3-100].

3.3.4.2 Two-switch step-up/step-down PFC preregulators

Two-switch step-up/step-down PFC preregulators are developed mainly to provide direct power transfer paths between input and output so that electrical stresses on transistors and requirements on energy storage capacity can be mitigated. In essence, the two switching devices are operated independently to achieve either boost or buck operation, depending on input and output conditions, with minimum indirect power processing [3-84]. The two-switch converters are basically derivations of the buck-boost converter through combination or integration of different topologies such as boost, buck, buck-boost, etc. by means of different techniques e.g. cascading, interleaving, integration, etc.

Cascaded connection of a buck and a boost converter has been proved as an effective approach to reduce indirect power and thus minimize electrical stress in switching devices. The cascading, determined by different implement approach, has been performed in two different ways: buck cascade with boost (BuCBo), boost cascade with buck (BoCBu) [3-99]. Regardless of the cascading pattern, the cascaded converters have the same operation principles: when instantaneous input voltage is lower than the output voltage, the boost converter part operates as a switching regulator, while transistor of the buck converter is kept on; when instantaneous input voltage is greater that output voltage, the buck converter is PWM controlled and the boost transistor is kept off [3-100].

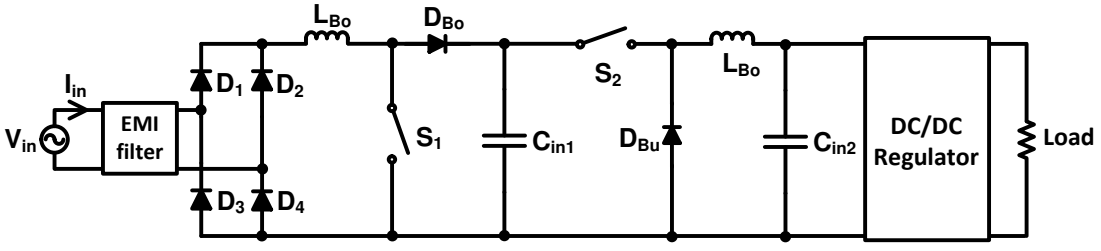


Figure 3.16 Boost-cascade-buck as PFC preregulator

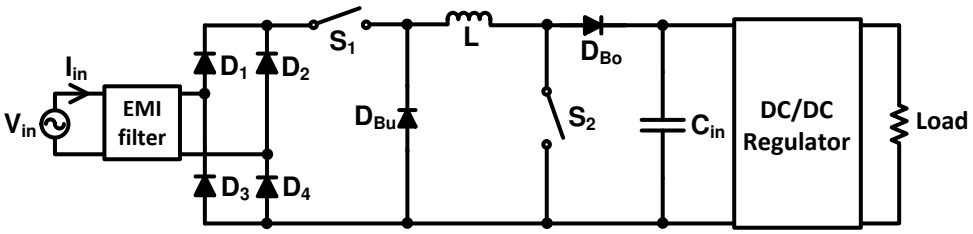


Figure 3.17 Buck-cascade-boost as PFC preregulator

Interleaved connection of a buck and a boost converter as a PFC preregulator can also provide both step-up and step-down operations throughout a half-line cycle by controlling the two switches independently. Two kinds of topologies are derived from interleaved connection, as illustrated in Figure 3.18 and Figure 3.19, namely boost interleaved buck-boost converter (BoIBB) and buck interleaved buck-boost converter (BuIBB). Similar to the operation principles of the cascaded step-up/step/down converters, interleaved converters essentially function as either a buck or a boost converter and thus have minimum indirect energy processing [3-99]. In a BoIBB, for instance, the boost cell is separated from the buck converter. The BoIBB functions as boost with S_2 kept on when input voltage is less than the output while functionality of buck is activated with S_1 kept off when input voltage is higher than output voltage [3-101].

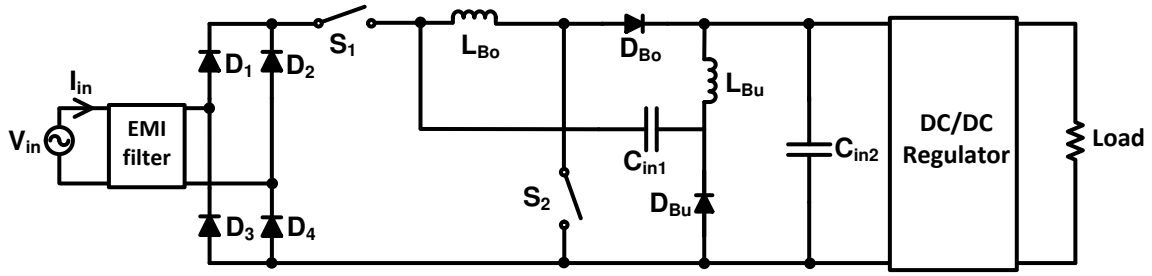


Figure 3.18 Buck-interleaved buck-boost (BuIBB) as PFC preregulator

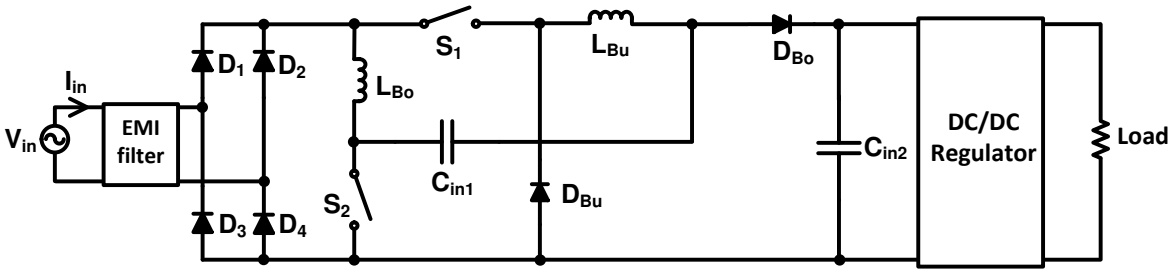


Figure 3.19 Boost-interleaved buck-boost (BoIBB) as PFC preregulator

Integrated step-up/step-down topologies merges different basic converters into one and thus, through proper control schemes, have two different conversion characteristics in a half-line cycle. Up to date, two different integrated converters has been investigated for application of PFC, both were derived by modifying the conventional buck converter. A novel integrated buck-Flyback was proposed in [3-50] by adding both passive and active components to a buck converter and, as the name suggests, can be operated as either a buck converter or a Flyback converter. An integrated converter that works either

as a buck or as a boost was discussed in [3-57]. Both converters have been reported having satisfying PF with low electrical stress on switching devices.

All two-switch step-up/step-down topologies, as indicated in Figures 3.16 to 3.19, achieves high PF, low voltage and low electrical stress in switching devices at the expense of added passive components, active components and corresponding control circuitry. The consequential high cost and complexity, low reliability nature of these topologies prohibit them from being widely adopted by industry [3-102].

3.3.4.3 Summary

The step-up/step-down topologies for implementing PFC achieves shaping of input current through a whole half-line cycle and low output voltage simultaneously, but with problems of their own.

- Single-switch topologies generally have high electrical stress in switching devices and require large energy storage element as there are no direct power delivery paths in the topologies and all the energy needs to be stored before processed by switching devices.
- Two-switch topologies are developed to facilitate direct power delivery path so that at least part of input power is transferred to output directly and thus reducing electrical stresses in switching devices and ease the pressure of energy storage, at the expense of increased component count, complexity and cost.

3.4 Discussion

In previous section, the existing PFC topologies are reviewed, with pros and cons of each topology be clarified under certain criteria, which involves both the PFC stage and the EMI filter. The interactions between the PFC stage and the DC-DC stage, however, are not considered. In this section, the interactions between the selection of the PFC topology and design and implementation of the DC-DC stage are discussed. Properties of the reviewed topologies are then summarized and qualitatively compared under certain criteria. Furthermore, the influence of high frequency operation of PFC topologies that is made possible with GaN devices applied are discussed and the effect of possible changes in characteristics of the topologies are compared relatively. Boost converter, which is likely to remain as a preferred option for implementing PFC even with GaN devices applied is then selected as a platform for further exploration of potentials of the new technology.

3.4.1 Interactions between PFC stage and DC-DC stage

In an AC/DC converter, the output of the PFC stage serves as the input of the DC-DC stage and the latter is usually designed with the input voltage as an important factor, as it affects many aspects of the regulator stage such as selection of transistor, design of the isolation transformer, etc. [3-103]. Although it was promoted that lower voltage on the smoothing capacitor i.e. input voltage of the DC-DC stage could potentially lead to loss reduction with adoption of lower voltage semiconductors and size reduction of the isolation transformer, comprehensive analysis on the interactions between the two stages has not been well investigated [3-45] [3-68] [3-71] [3-78] [3-104].

On one hand, as electrical isolation is usually expected in the DC-DC stage, characteristic of the DC-DC stage e.g. load conditions of this stage hardly have any effect on the design of the PFC stage. On the other hand, as introduced in 2.3.3, regardless of the specific topology selected for PFC stage, voltage on the smoothing capacitor will be either high (typically, 385V~400V in step-up type topologies) or low (normally, 80V~100V in step-down and step-up/step-down topologies). The different voltage levels, and corresponding current levels when the same power delivered, affects loss in transistors and size of isolation transformer in a similar way:

- Loss of the transistor(s) in DC-DC stage is not necessarily affected by the PFC stage. With higher input voltage of the DC-DC stage, transistors with higher voltage ratings and consequentially higher on-state resistance are needed. At the same operation frequency, switching loss of transistor(s) might be larger with state-of-art transistors (200V~600V MOSFET) where switching loss is mainly capacitive, while conduction loss of the transistors could be either increased or decreased as RMS current is lowered whereas higher on-state resistance is introduced. Specially, with the introduction of superjunction MOSFETs where the on-state resistance is almost linearly related, conduction loss is likely to decrease. In other words, depending on the specific current level and properties of the selected transistors, loss in the transistors in high input voltage DC-DC converter might be higher, comparable or even lower than that with low input voltage.
- The PFC stage has limited influence on size of the isolation transformer in DC-DC stage. With higher input voltage and lower input current, larger inductance is needed to store similar amount of energy. The required higher inductance, however, does not necessarily lead to larger magnetic core size as increasing number of turns in windings, which is likely to happen in order to deal with the increased voltage conversion ratio in typical DC-DC regulator topologies such as Flyback, can fulfill the demand on the same core as used in low input voltage conditions without saturation. Apart from practical implementation point of view, theoretically, when the same amount of energy needs to be stored, size of the energy storage elements would stay approximately the same. Besides, size of isolation transformers in DC-DC stage is also greatly affected by electrical insulation distance needed between primary and secondary windings to meet safety standards [3-105]. In particular, in the most commonly used topology for PFC stage, namely the Flyback converter, all the energy needs to be stored in the transformer before being transferred to output and thus, with the same power delivery need, the same size of the transformer is needed. And therefore, size of the isolation transformers in high input voltage DC-DC converters are likely to be comparable with that in low input voltage ones.

To sum up, as the output of the PFC preregulator is also input of the DC-DC regulator, output properties of the former stage have influences on performance, particularly loss in transistors and size of isolation transformer, of the latter stage. The influences, unlike was believed in literature, may not be decisive. Besides, with the presence of the electrical isolation, output properties of the DC-DC regulator have hardly any effect of design and implementation of the PFC stage. It worth be pointed

out that, as the two stages interacts only through the output characteristics of the PFC stage, almost no relevance exists between operation frequency of the PFC preregulator and performance of the DC-DC regulator.

It should be noted that, the floating or inverting output of PFC stage as discussed in 3.3.3.2 and 3.3.4.1 respectively, will have detrimental effect on the DC-DC stage if they are applied. However, as the two kinds of topologies are not feasible for application, their effects are excluded. Moreover, the effect of design and implement of the DC-DC stage on that of the EMI filter in a AC/DC converter is also not considered in this thesis. Designing of the EMI filter in an AC/DC converter usually happens after the design of both the PFC stage and the DC-DC stage as the purpose of the EMI filtering, ideally, is to mitigate high frequency noise from these two stages. CM noise needs to be filtered comes from both stages while DM noise originates only from the PFC stage as the smoothing capacitor functions as a low-pass filter. CM noise generated in DC-DC stage, in many cases, may be regarded as a constant factor on EMI filter design of the whole AC/DC converter as higher voltage on transistors in DC-DC converter is usually accompanied by lower current, which makes dv/dt smaller when other factors e.g. driving circuitry, parasitic capacitance are more or less the same. In topologies that have both high voltage and high current stress on transistors in DC-DC stage, like the commonly used Flyback, CM noise suppression methods are usually applied. In fact, many different CM noise suppression methods have been developed and adopted in DC-DC stage in commercial SMPSs [3-106]-[3-109]. Accordingly, CM noise generated in the DC-DC stage is usually not considered in designing the EMI filter for the AC/DC converter i.e. filter design is determined only by high frequency noise of the PFC stage as demonstrated in [3-17] [3-103].

3.4.2 Qualitative comparisons of PFC topologies

The step-up type and step-up/step-down type topologies, with suitable control schemes, can shape input current throughout a whole half-line cycle and therefore have high PF (both types of topologies have PF well above 0.9 in most cases [3-56] [3-60] [3-110] [3-111]). Step-down type topologies, although only shaping input current partly in a half-line cycle, can also pass regulations through proper design and control [3-24] [3-71]. Differences of the topologies, accordingly, differ mainly in properties of the topologies such as power component count, number of switching devices, driving requirement, electrical stress on transistors, energy storage demand and the EMI noises that come along.

Quantifying and comparing features of PFC topologies and corresponding EMI performances requires extensive investigations on design, optimization and implementation of each topology and the results can be controversial as properties of a topology depends highly on many different aspects such as power levels, operation mode of the topology, specific control schemes, etc. The topologies discussed in 3.3 are mostly developed for low power PFC (below 1kW) while investigation on topologies for high power (above 1kW) PFC applications mainly focuses on boost converter and interleaved boost converter. As will be made clear later, step-down and step-up/step-down topologies, in nature, would generate much higher DM noise than step-up ones while the level of CM noise may be comparable. In high current, i.e. high power PFC applications, driven mainly by the need of low conducted EMI and thus simplified design and implementation of EMI filters, step-up type converters are used. In fact,

discussed in 3.3.3.2, the CM noise inherently induced in a bridgeless boost converter makes it not practically applicable, boost and interleaved boost are mainly used as PFC preregulators in high power range. Investigations of high power PFC converters are therefore focus on performance optimization of boost and interleaved boost converters. For instance, to achieve loss reduction, boost and interleaved boost converters are operated in different operation modes (boost in CCM and interleaved boost in CCM and BCM) [3-9] [3-22] [3-54] [3-112]. Besides, as already discussed in 3.3.1, choice of operation mode greatly affects requirements of a PFC topology concerning DM noise filtering, sensing technique, etc.

In this thesis, attention is paid to low power PFC topologies and qualitative comparisons of the topologies are made according to characteristics of a PFC topology and its influence on EMI filter design. EMI noise generated is usually measured by both DM and CM noise levels, with DM noise the resultant of switching current waveforms and CM noise the outcome of switching voltage(s) of transistor(s) [3-16]. Performance of a PFC topology, on the other hand, can be evaluated from many different perspectives such as cost, efficiency, size, reliability, complexity, etc., which are greatly affected by specific implementation approach that involves various practical issues e.g. power components used, auxiliary circuit required, level of control algorithms demanded, etc. Although it might not be feasible to compare performances of different topologies without thorough investigation on design and optimization of each topology under the same input and output specifications, fundamental properties of the topologies that leads to the practical issues can be qualitatively summarized. For instance, instead of comparing possible sizes of passive components in different topologies that are highly dependent on practical actualization methods, level of energy storage requirement or value of passive elements in different topologies, which would lead to reasonable estimation on volumes of passives, can be compared.

Characteristics of the PFC topologies and associated EMI behaviours are summarized in Table 3-1 under the selected criteria, with boost converter and corresponding EMI performance as a reference. The criteria include power component count, driving requirement, electrical stress of transistors, energy storage demand in a PFC topology and EMI noise generated. The criteria cover requirements on major properties of both active (electrical stress, which affects component ratings and loss) and passive components (energy storage demand, which affects size of passives), auxiliary circuit (driving requirement of transistors) needed and influence on EMI filter design (level of DM and CM noise). Characteristics of boost converter are marked as “0” and with performance of other topologies better or worse than boost under one criteria illustrated by “+” or “-”, respectively.

Power component count. As illustrated from Figure 3.5 to Figure 3.19, the basic buck, buck-boost and the modified buck with low side transistor have the same amount of component as that in a boost and, with reduction of conducting semiconductors in current paths, bridgeless boost and bridgeless buck requires fewer components. All other topologies need larger component count than boost, especially the ones of two-switch step-up/step-down type.

Number of switches. The three basic topologies, boost, buck and buck-boost have one transistor, and so does the modified buck converter and buck-boost variants. The rest topologies all requires two transistors.

Driving requirement. The grounded transistor in a boost converter facilitates simple implementation as low-side driving is made possible, which is also true in bridgeless boost converter and interleaved boost converter even though the number of transistors doubled and complexity of control increased. Major variants of buck-boost converter, namely Cuk and SEPIC converter, also have grounded transistors. The modified buck to repositioning transistor in a buck converter as a grounded switch avoids undesirable high-side driving need, which is common to all other topologies in step-down type and all topologies in two-switch step-up/step-down type.

Electrical stress of transistors. In step-up type topologies, output voltage needs to be set higher than peak of universal input and transistors in these topologies has to stand the high voltage (385V~400V). In step-down topologies, transistors are connected to input directly and thus highest voltage across transistors equals peak of universal input, which is slightly lower than that in step-up converters. For the same input current, switching currents in step-down topologies are higher than that in step-up converters due to their discontinuous nature, as indicated in Figure 3.6 and Figure 3.10. Of step-up type topologies, transistors in boost and bridgeless converters have the same switching currents while in interleaved boost converter, because of the current sharing property enabled by the paralleling of converters, transistors have lower current stress. Single-switch step-up/step-down topologies, resulting from the fact that all the power delivered need to be processed through transistors, both voltage and current stress are higher in these topologies than the boost converter where part of power transfer occurs directly from input to output. Two-switch step-up/step-down topologies that are developed to provide direct power transfer paths while maintaining step-up/step-down capacity and low output voltage, regardless of specific technique adopted, function partially as a boost converter and partly as a buck converter in an input cycle. Accordingly, voltage stress on transistors are subjected to peak of universal input while switching currents would be comparable to that in a boost converter in switching cycles when input voltage is lower than output voltage but higher than that in a boost converter in the rest part of a input cycle. And therefore, in two-switch step-up/step-down topologies, transistors would have slightly lower voltage stress but higher current stress than in a boost converter.

Energy storage requirement. Two different types of energy storage requirement exist in a non-isolated PFC stage, energy storage in output capacitor for powering the downstream stage (line frequency related) and energy storage in either inductor or capacitor within the topology for proper functioning of the PFC converter (switching frequency related).

- *Line frequency related energy storage*. For the same holdup time requirement in case of input failure of a AC/DC converter, capacitors with much higher value are needed in step-down and step-up/step-down types of topologies than that in step-up ones as output voltage is lower.

- *Switching frequency related energy storage*. Comparisons on values of energy storage elements in PFC topologies is not so straight forward as that of output capacitance because adopted energy storage technology may differ in different topologies. For instance, in most of the topologies energy are stored in inductive elements while in topologies like Cuk and SEPIC energy storage are also achieved in capacitors. Besides, in some topologies e.g. boost, bridgeless boost, buck, etc. single energy storage element are demanded while in topologies like interleaved boost, bridgeless Cuk and most of the step-up/step-down topologies multiple elements are necessary to fullfill the need of energy storage. And therefore, energy storage requirement within PFC topologies are qualitatively assessed by the level of energy need to be stored when the same power needed to be delivered. Energy storage requirement may be interpreted in two different ways: the maximum amount of energy needs to be stored and the maximum net amount of energy that is stored and released within one switching cycle. The two types of requirements actually is positively correlated in PFC application as value variation of current ripple and peak current follows the same trend in different switching cycles through a half-line period. Basically, single-switch step-up/step-down type topologies demands that much more energy stored than step-up type or step-down ones as there's no direct power delivery path and all the energy needs to be stored before being delivered to output. In step-up and step-down type topologies, energy is partially transferred to the output directly and partly stored and released by passive components in each switching cycle. In both step-up and step-down type topologies, indirect power transfer is determined by the input voltage, current and duty cycle when they are operated at the same frequency. Accordingly, the same energy storage requirement is called for within each group of topologies and, when performing PFC with universal input with the same power delivery capability at the same fixed switching frequency, step-down type topologies have higher energy storage requirements than step-up type ones in terms of maximum energy to be stored and released in switching transients of transistors.

CM noise. CM noise generated by switching devices in PFC topologies is greatly affected by practical implementation issues such as level of voltage to be switched, value of parasitic capacitor between active area of a switching device and earth, driving conditions of switching devices, etc., and therefore is not possible to judge levels of this type of CM noise in different topologies without presumptions on aforementioned issues and through analysis of noise generation. CM noise, in fact, can also be induced by operation nature of PFC topology, which is the focus of this work. As introduced in 3.3.3.2, bridgeless boost converter, due to the fact that output ground of the converter is a floating one that pulsates with high voltage and high frequency, significant CM current would be generated from charging and discharging parasitic capacitance between output ground and input ground. Any other converter introduced would not produce CM noise topologically.

DM noise. DM noise that is determined by the waveform of switching currents are worse in step-down and step-up/step-down topologies than the boost because, as illustrated in Figure 3.10 and Figure

3.14, the currents are discontinuous and has higher amplitude. In step-up topologies, bridgeless boost has comparable current as the basic boost while interleaved boost effectively lowers switching current and thus has less DM noise.

As can be seen in Table 3-1, under the selected criteria, single-switch step-up/step-down converters generally have worse topological properties and EMI performance than step-up ones. Two-switch step-up/step-down topologies only outperform step-up ones with lower voltage stress with limited difference (peak of universal input voltage in comparison to output of step-up type converters) while, when it comes to any other property, they have worse performance. Step-down type converters, in general, also perform not as good as step-up types in measure of most of the selected properties, although they all feature lower voltage stress with limited margin (the same as in step-up/step-down type converters). Of step-up type, the converters have the same voltage stress, energy storage and driving requirement but performance differs when evaluated with other characters. Interleaved boost converter promises lower current stress in transistors and lower level of DM noise at the expense of increased power component count while bridgeless boost converter demands least power components but generates CM noise. With state-of-art technology, as discussed in [3-60][3-62], the aforementioned merits of bridgeless boost converter and interleaved boost converter are overwhelmed by their demerits and the converters are not suitable for practical application. And thus, boost converter, from qualitative comparison point of view, would be the most proper choice for implementing PFC, which corresponds well with the widely-adopted practice of using boost converter as PFC preregulator in industrial products.

It should be pointed out that, except the selected ones, there are also other aspects that differs in different PFC topologies, which either are coupled with at least one of the criteria or are not so critical. For instance, different control schemes are needed to achieve regulation of both output voltage and input current. The complexity in control, generally, is affected greatly by the number of transistors as in two-transistor topologies more advanced control approaches e.g. complementary operation, synchronization of switching actions are needed. Besides, features like inrush current limiting capacity, level of sensing need etc. are considered as less important since these factors have little effect on major performance of the PFC stage such as efficiency, power density, etc., especially when they are properly dealt with.

3.4.3 High frequency operation of PFC topologies

The qualitative summary and comparisons of PFC topologies are made based on the assumption that the converters are operated at the same frequency with application of state-of-art Si devices. With the advent of new semiconductors that can operate beyond the capability of Si devices in terms of switching speed, high frequency operation of the PFC stage is made possible. It is therefore necessary to examine, relatively, changes in performance of the discussed topologies that would be brought about by the increase of frequency. To conduct the examination, effects of pushing up operation frequency on fundamental properties of PFC topologies should be carried out.

Pushing up switching frequency of PFC converters would affect fundamental properties selected as criteria for assessing performance of the topologies differently:

- Operation frequency of a converter would not affect whether CM noise will be generated topologically or not. And therefore, the increase in switching frequency would not change the fact that bridgeless boost converter would lead to CM noise generation because of the operation nature of the topologies and CM noise would not be topologically induced in other topologies.
- Level of DM noise generated in a PFC topology, as discussed in previous section, is determined by the switching of currents, which is the resultant of operation mechanism of a topology. Pushing up operation frequency of different topologies equally would increase level of DM noise evenly and, because of the discontinuous and high amplitude nature of switching currents, step-down type and step-up/step-down topologies would still have higher DM noise than step-up type ones.
- Variation of switching frequency would not affect power component count and number of switches in a topology as no active or passive component can be excluded for proper functioning of the topology regardless of working frequency, values of passive components are affected though.
- Level of driving requirement is determined by the location of transistors in a topology, which would not be changed by the elevation of operation frequency.
- Given the fact that step-up and step-down type converters are subjected to the output voltage and peak of input voltage, respectively, voltage stress in the two types of converters are therefore independent of frequency. Besides, the continuous (in step-up type converters) and discontinuous (in step-down type converters) nature of currents is independent on switching frequency of the currents. And thus, the trend that step-down type converters have slightly lower voltage stress but higher current stress than step-up ones will not be shifted by elevating frequencies of the converters. Furthermore, for the same power delivered, one-switch step-up/step-down converters would still have both higher voltage and higher current stresses than step-up converters as more energy needs to be processed. Two-switch step-up/step-down converters, with voltage on transistors subjected to input and current in transistors determined by the discontinuous nature, would remain its characteristics of having slightly lower voltage stress but higher current stress than step-up converters.
- As discussed in previous section, demand of output capacitance is determined by the level of voltage across the smoothing capacitor and independent of operation frequency of the PFC stage. The level energy storage requirements within PFC topologies, which are determined by the power needs to be delivered and conduction time of transistors, would not be shifted by increasing of operation frequency equally.

And therefore, it can be concluded that, pushing up frequency will not change the shape of Table 3-1. In other words, when evaluated with the selected criteria in Table 3-1, boost converter will remain as the preferred choice when operation frequencies are pushed up equally. It should be noted that properties of PFC topologies are assessed qualitatively by considering the net effect after pushing-up

of operation frequencies, and it is possible that one of other topologies would achieve more quantitative gain in measures of certain criterion than boost converter even though the final performance is still inferior to that of boost. It should also be pointed out that the characteristics that were regarded as less important in Si based topologies generally are not affected by operation frequency and thus are neglected when analysing the influence of high frequency operation of the topologies.

Table 3-1 Properties of PFC topologies

Topology			EMI Performance		PFC stage						
								Electric stress on transistors		Energy storage	
			CM Noise	DM Noise	Power Component Count	No. of switches	Driving Requirement	Voltage	Current	Switching frequency related	Line frequency related
Step-up		Boost	0	0	0	0	0	0	0	0	0
		Bridgeless boost	-	0	+	-	0	0	0	0	0
		Interleaved boost	0	+	-	-	0	0	+	0	0
Step-down		Buck	0	-	0	0	-	+	-	-	-
		Modified buck with low side transistor	0	-	0	0	0	+	-	-	-
		Bridgeless buck	0	-	+	-	-	+	-	-	-
Step-up/ Step-down	Single-switch	Buck-Boost	0	-	0	0	-	-	-	-	-
		Buck-boost variants	0	-	-	0	0	-	-	-	-
	Two-switch	Cascaded	0	-	-	-	-	+	-	0	-
		Interleaved									
		Integrated									

3.4.4 Boost converter used for exploring potentials of GaN devices

GaN devices, as suggested by their material properties in chapter 2, have the potential of greatly improved Figure-of-Merit (FOM) and therefore would reduce loss substantially. To facilitate the exploration of whether GaN devices really can live up to the promises of the material properties, the devices need to be tested and analysed. Accordingly, a topology that could enable different switching and conduction conditions is needed. In theory, as elaborated in 3.3.1, all the PFC topologies can operate in different operation modes that, in essence, provides different switching and conduction conditions for transistors in the topologies, and therefore, theoretically, any of the discussed topologies in 3.3 can be used for assessing performances of GaN devices. Given the fact that, with the operation of the PFC stage pushed up, boost converter will remain as preferred option, exploration on potentials of GaN devices for high frequency application is to be carried out in PFC boost converter in this thesis.

It should be noted that "high frequency" in this work, the focus of which is on exploring potentials of GaN technology in existing topologies, is limited to the range of a few MHz. As illustrated by the example of a boost converter to be used for implementing PFC in chapter 5, limited by the nature of the topology and conventional driving approach, benefits of available GaN devices cannot be achieved when frequency is increased beyond 9.4 MHz, even when both ZCS and ZVS switching (turn-on) are enabled. To overcome the frequency boundaries, topological innovations and new driving schemes might be needed, like the case with very high frequency power conversions where novel resonant topologies are proposed [3-113]-[3-116] and the self-oscillating resonant gate drive circuit that was developed [3-117].

3.5 Summary

In this chapter, overview of PFC converters is performed with the purpose of providing background of the platform for evaluating and demonstrating potentials of GaN devices, PFC. The concept of PFC is introduced first to make it clear why the technique is needed in AC/DC converters and, generally, two groups of PFC techniques, passive and active, are discussed. After which focus is given to the widely-adopted approach, PFC DC-DC converters.

DC-DC converters that have been used for implementing PFC are overviewed with the attention paid mainly to the converters in two-stage AC/DC converters rather than the single-stage where PFC is combined together with DC-DC regulation as single-stage AC/DC converters are limited to low power range and demands high voltage, large value storage capacitors. In two-stage AC/DC converters where the PFC stage and the DC-DC regulator are in cascade configuration, various DC-DC converters have been investigated to actualize the function of PFC. Broadly, the DC-DC

converters used in PFC stage, according to conversion characteristics, are categorized into three groups, namely step-up, step-down and step-up/step-down, with each type of topologies root from one of the basic DC-DC converters, boost, buck and buck-boost, respectively. The topologies are introduced with their basic behaviours on fulfilling PFC and with merits and demerits of each topology discussed. Although these topologies can all shape input current of a AC/DC converter so that standards and regulations can be passed, they differ a lot from each other in properties such as component count, number of switching devices, driving requirement, electrical stress on switching devices and energy storage demand. Besides, the topology used for PFC also interacts with the downstream DC-DC regulator and affects EMI filtering task. And therefore, properties of the PFC topologies and associated EMI performance are qualitatively summarized and interactions between PFC stage and DC-DC regulator stage are discussed. Finally, after the examination on influence of high frequency operations on properties of PFC topologies, boost converter, which is likely to be the preferred choice for implementing PFC with GaN technology applied, is selected for exploring potentials of GaN devices.

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Chapter 4. Loss modeling of GaN transistors in a boost converter

4.1 Introduction

As discussed in Chapter 2, from the perspective of material properties, GaN transistors would greatly improve FOM and reduce loss compared to their Si counterparts. Losses in a transistor, however, are determined by more than just the properties of the material. Issues such as die design and fabrication approaches (which relates directly to device parasitic capacitance and R_{dson}) and device packaging technology (which, in many cases, determines device parasitic inductance) also affect capabilities of GaN transistors. Furthermore, in-circuit performance of GaN transistors are subjected to the circuit environment i.e. topology and operation mode of the circuit, parasitic elements of the adopted circuit carrier, etc. In particular, as shown previously in chapter 3, electromagnetic volume of the normally-off GaN HEMT is negligibly small in comparison to the rest parts of a power converter and circuit parameters have profound influence on losses of the transistor. Therefore, it is necessary to evaluate performance of GaN transistors, with both device characteristics and circuit parameters being accounted for, so as to uncover the capabilities and limitations of the transistors for high frequency applications.

In order to perform evaluation of GaN transistors, loss modelling of the devices is needed. Generally speaking, three different types of approaches exist for modelling losses in Si devices: physics-based loss modelling, behaviour-based loss modelling and analytical loss modelling [4-1]. Physics-based loss modelling method takes various physical parameters of a transistor, such as geometry, doping profile, etc. into consideration to calculate loss. In spite of the satisfying results, this approach demands access to detailed data about the transistor that is usually not available for electrical engineers and in the cases the data is accessible, the calculation is time-consuming [4-2]. Behaviour-based loss modelling utilizes behaviour models e.g. Spice models of the transistor provided by device vendors to analyse switching and conduction behaviours, as well as switching and conduction loss, of the devices. This method gained its popularity mainly because it is fast and easy to implement. Unfortunately, as switching loss is estimated by integrating voltage and current waveforms in switching transients, which is not necessarily the actual loss in the transistor, accuracy of switching loss calculation is not always satisfactory [4-3]. Moreover, loss mechanisms in transistors i.e. electric elements that affect voltage and current waveforms cannot be revealed. Analytical loss modelling, based on equivalent circuits with assumptions and simplifications, derives expressions of voltage, current and loss in both switching transients and on-state of the transistor. This approach is quite rewarding once reasonable accuracy is achieved: convenient loss breakdown to uncover dominating loss in the transistor and analysis of the reasons behind is enabled; identification of effects of circuit and device parasitic elements is

made easy [4-1] [4-3]. In this thesis, to model loss in the newly developed GaN devices, of which the characteristics and behaviours are unknown, a combination of analysing behaviours of the devices from their physical structures and analytically modelling of the devices accordingly is employed.

4.2 Equivalent circuit of a GaN based boost converter

To perform analytical loss modelling of a GaN transistor, an equivalent circuit is needed to analyse voltage and current during switching transients and on-state to calculate loss in the transistor using circuit laws. The equivalent circuit should include a proper circuit model of the transistor and critical components, which contributes to functioning of the circuit and/or affect switching or conduction behaviours of the transistor. Transistor circuit model should reflect physical structure of the die (which results in operation mechanisms and electrical characteristics of the device) and package technology adopted for the device (which contributes to parasitic elements). Given the fact that GaN transistors are to be operated in high frequency applications, parasitic elements originated from both transistor package and the circuit should be accounted for.

4.2.1 A general circuit model for normally-off GaN HEMT and GaN GIT

Circuit models of two different kinds of normally-off GaN transistors, GaN HEMT and GaN GIT, are developed, through the approach of using a combination of existing discrete electric components to approximate electric characteristics, reflect operation mechanisms and indicate packaging technologies of the transistors.

4.2.1.1 Circuit model of normally-off GaN HEMT

As discussed in [4-5] operation of a normally-off GaN HEMT resembles that of a conventional, enhancement mode Si MOSFET. Similar to a Si MOSFET, parasitic elements inherent with the die (e.g. parasitic capacitances) and package (e.g. parasitic inductances) of a GaN HEMT limits its capabilities in terms of switching speed, thermal limit, etc. Apart from the similarities, differences between Si and GaN technologies lead to some unique characteristics of GaN HEMTs.

Basic operation mechanisms of a normally-off GaN HEMT, resulting from its die structure, is analogous with that of a typical enhancement Si MOSFET: with a 2DEG channel generated in the AlGaN/GaN interface and a gate metal over the channel to form a metal-semiconductor junction to lift up the potential between gate and channel, the transistor has a depleted region underneath the gate; a positive bias from gate to the AlGaN/GaN interface (shown in Figure 4.1) is required to attract electrons underneath the gate so as to form and enhance a bidirectional channel between drain and source; with a removal of the positive bias from gate, the electrons underneath are dispersed into GaN layer and the depletion region is recovered to block the voltage between drain

and source [4-6]~[4-8]. And therefore, basic operation mechanism of the device is represented by a symbol of an ideal n-channel enhancement-mode MOSFET.

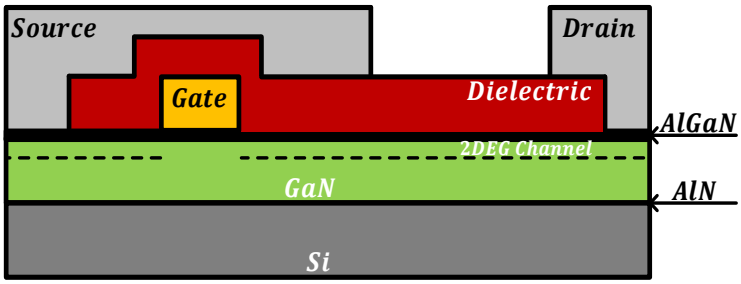


Figure 4.1 Structure of a normally-off GaN HEMT [4-5]

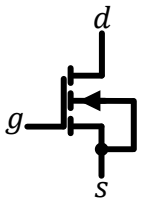


Figure 4.2 Basic operation mechanisms represented by a symbol of MOSFET

Gate-channel diode, resulting from the fact that a metal-semiconductor structure (gate metal layer to AlGaN layer) to ensure a normally-off feature, exists in GaN HEMT. Unlike the commonly seen insulated MOS-gate in a Si MOSFET, the metal-semiconductor junction in GaN HEMT forms a Schottky barrier between gate and AlGaN/GaN interface. Given the nearly symmetrical geometry of the transistor, either a positive gate to drain bias or a positive gate to source bias can overcome the barrier and enable current flow from gate to drain or source, respectively. As is clearly illustrated in Figure 4.3, expansion of drain-side channel is longer (higher resistance) than that of source-side. As a result, current conducted through gate-channel diode to drain would be smaller than the current to the source for the same value of V_{gs} and V_{gd}. To include the effect of gate-channel diode and its conduction characteristics, two different Schottky diodes D_{gs} (between gate and source), D_{gd} (between gate and drain) are placed between in circuit model of GaN HEMT (shown in Figure 4.4). The two diodes have the same build-in potential, which is determined by the metal-semiconductor barrier. On-state resistance of D_{gs} (including resistance of gate-channel junction and that of drain-side channel) is smaller than that of D_{gd} (consists of gate-channel junction resistance and source-side channel resistance).

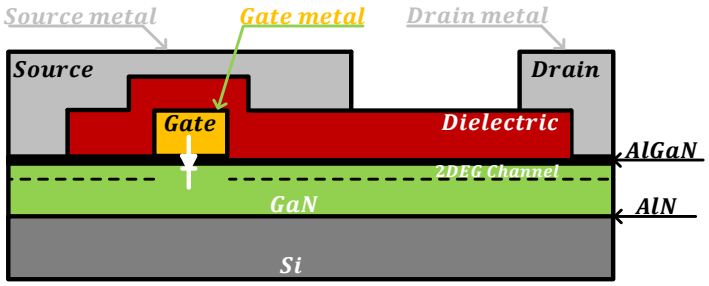


Figure 4.3 Schottky junction between gate and 2DEG channel in GaN HEMT

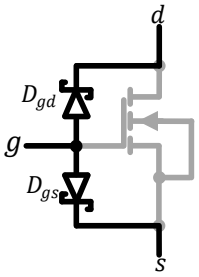


Figure 4.4 Equivalent diodes in circuit model of GaN HEMT

Parasitic capacitances, as lumped from physical structure of a normally-off GaN HEMT in Figure 4.5, originate from multiple sources. Capacitances between metal layers of the three terminals (C_{gs1}, C_{gd1}, C_{ds1}) can be treated as constant, whereas capacitances formed between metal layers and transistor channel (C_{gs2}, C_{ds2},C_{gd2}, C_{gc}) are voltage-dependent resulting from depletion characteristics of the channel. It should be noted that gate-channel capacitance C_{gc}, due to the nature of nearly symmetric geometry of the device, can be gate to source, gate to drain or even shared, depending on the node conditions [4-6]. For instance, when drain is negative while source and gate are grounded e.g. in BCM-VS in the case of $V_{out}>2V_{in}$ as introduced in chapter 2, C_{gc} will add up to gate-drain capacitance as the channel underneath gate will be formed when V_{gd} swings beyond V_{th} (gate threshold voltage). Given the fact that different capacitors between two terminals are in parallel, they can be lumped further into three capacitors of C_{gs}, C_{ds} and C_{gd}, as commonly seen with Si MOSFET. It should be noted that parasitic capacitances also exist between metal layers/transistor channel and Si substrate, which also contribute to effective capacitance values of the transistor.

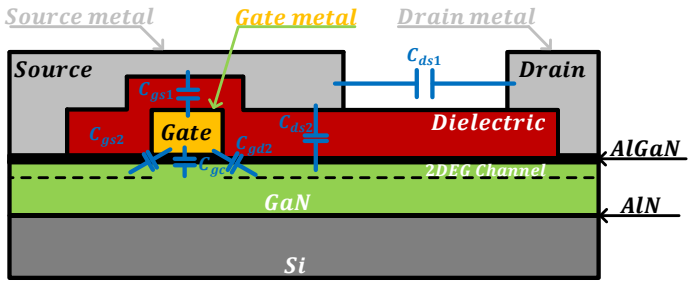


Figure. 4.5 Schematic of capacitance sources in GaN HEMT [4-6]

Table. 4-1 Parasitic capacitances in a normally-off GaN HEMT

Capacitance	Description	Value
C_{gs1}	Gate metal to source metal field plate capacitance	Constant
C_{gs2}	Gate metal to source side channel capacitance	Voltage-dependent
C_{ds1}	Drain metal to source metal field plate capacitance	Constant
C_{ds2}	Source to drift region capacitance under the field plate	Voltage-dependent
C_{gd1}	Gate metal to drain metal capacitance	Constant Not shown in Figure 4.5
C_{gd2}	Gate to drain side drift region	Voltage-dependent
C_{gc}	Gate to channel capacitance	Voltage-dependent

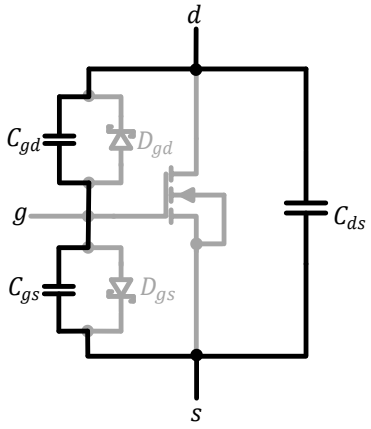


Fig 4.6 Parasitic capacitances represented by capacitors between terminals

Reverse conduction of normally-off GaN HEMT has different mechanism but similar function in comparison to Si MOSFET. Since the GaN HEMT is a lateral device, there's no parasitic bipolar junction i.e. body diode in the transistor. Conduction of current in reverse direction (from source to drain) in GaN HEMT when it is off ($V_{gs}<V_{th}$) is made possible with a positive bias between gate and drain (drain drift region, to be exact). Due to the nearly symmetric nature of transistor structure, a positive V_{gd}, as a positive V_{gs} does, attracts electrons underneath the gate. Once V_{th} is reached, there are sufficient electrons to form the channel and conduct current from source to drain. Before the transistor is fully on, resembling the dependence of on-state resistance on V_{gs} in forward conduction, resistance of the channel depends on the value of V_{gd}. When it is fully on, unlike in forward conduction where voltage across GaN HEMT depends on R_{dson} and the value of current through it, voltage drop on GaN HEMT (V_{ds}) is affected by both V_{gs} and V_{gd}, as expressed in (4.1).

$$v_{ds} = v_{gs} - v_{gd} \tag{4.1}$$

Given the facts that transistor is off (V_{gs} usually is zero or even negative) and it demands at least a threshold voltage to make transistor channel conductive, V_{ds} is higher than the voltage drop on

a body diode in Si MSOFET. On the other hand, the benefit brought by this mechanism is that no minority carrier is involved in the conduction process, and thus no reverse recovery loss will be generated [4-9].

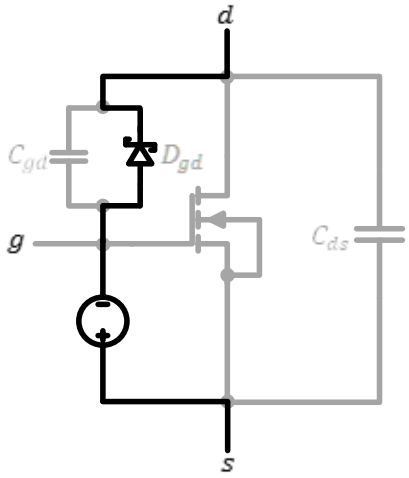


Figure 4.7 Reverse conduction feature of GaN HEMT

Parasitic inductances in a transistor stem from both die and packaging of the device, with contribution form the former usually negligible compared to the latter. Packaging is needed for purposes of providing electrical connections between transistor die and outside circuits, improving robustness of the device, enhancing the convenience of handling the product, etc., and therefore is unavoidable in most cases [4-10]. Packaging of a transistor, however, degrades performance of a transistor in terms of increased on-resistance and inductance, etc. Package parasitic inductances affects switching behaviors of a transistor, resulting in increased switching loss and voltage and current stress in the transistor. For instance, when a 30V MOSFET is used in a 12V/1.2V, 20A POL converter at 600kHz, share of package related loss is reduced by 25% by replacing the initial SO8 package to Dr. MOS (integrated Driver-MOSFET) while keeping the same die [4-11]. The normally-off GaN HEMT, as shown in Figure 4.3, has three layers of metal to connect the active device to the outside world and all the three layers are on top side of the chip. The top metal layer of a GaN HEMT die is used as a foundation for placement of solder bumps as shown in Figure 4.8. This configuration allows the GaN HEMT to eliminate unnecessary elements of traditional Si MOSFET packaging e.g. wire-bonds that contribute to increased inductance, thermal and electrical resistance, etc. Furthermore, the LGA (Land Grid Array) package adopted by GaN HEMT, demonstrated in Figure 4.9, uses interleaved drain and source terminals to minimize parasitic inductance and resistance of the package [4-10]. As a result, a normally-off GaN HEMT has low parasitic inductances [4-48]. The parasitic inductances of GaN HEMT are lumped in to three different inductors (L_d, L_s and L_g), which are placed at the terminals of the circuit model of the transistor.

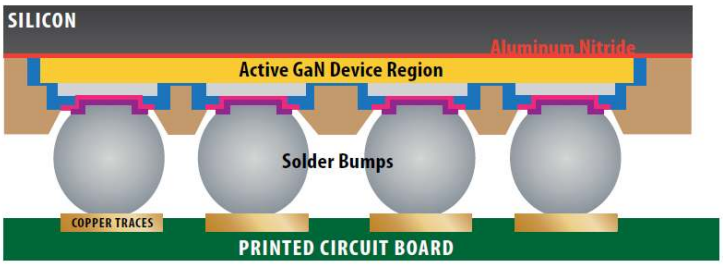


Figure 4.8 Flip chip connection of normally-off GaN HEMT [4-5]

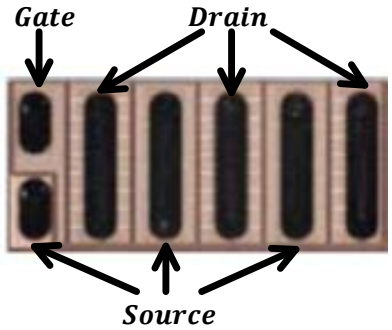


Figure 4.9. A 200V LGA packaged normally-off GaN HEMT [4-5]

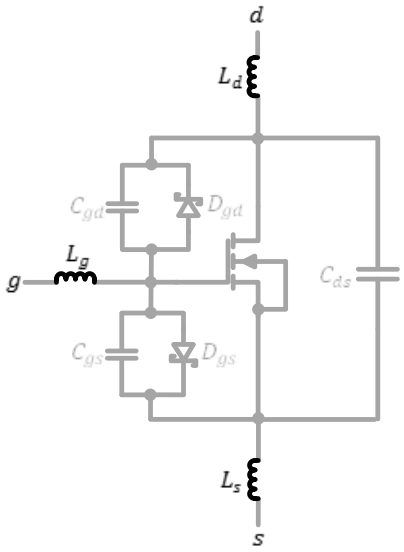


Figure 4.10 Parasitic inductances of GaN HEMT lumped into L_d, L_s and L_g

Parasitic resistances that source also from both die and package of GaN HEMT would result in conduction loss and cause increased switching loss, and therefore should also be accounted for in circuit model of the device. Resistance of the transistor between drain and source terminals when it is conducting in forward direction (including drain and source terminal package parasitic resistances, channel resistance, etc.) can be lumped as R_{dson} (which is not shown in Figure 4.11, but will be accounted for in calculation of conduction loss), while parasitic resistances root from gate terminal package and gate to channel resistance (R_{gc}) is lumped into one resistor R_g.

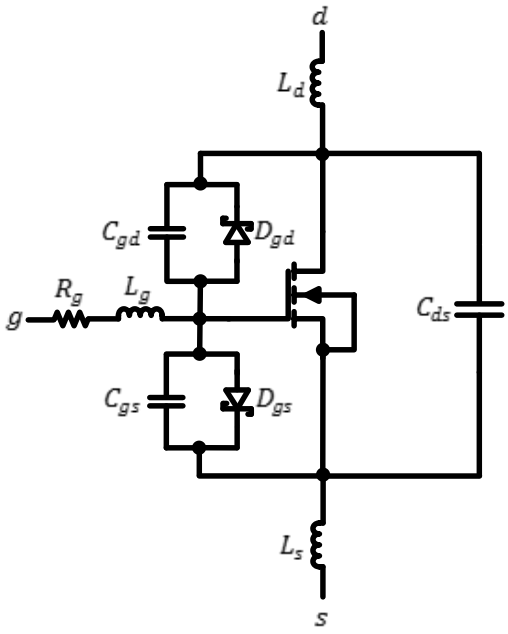


Figure 4.11 Circuit model of normally-off GaN HEMT

To summarize, a circuit model of a normally-off GaN HEMT (shown in Figure 4.11) is developed in accordance with the physical structure of the die and packaging approach taken for the device: basic operation mechanism of the device is represented by an ideal n-channel enhancement-mode MOSFET, while the parasitic capacitances in the die are added in the form of lumped capacitors between different terminals; two different Schottky diodes are added to features of current conduction through gate-channel diode to drain and source, respectively; reverse conduction of the transistor when it is in off-state is possible with a positive bias between gate and drain; lumped parasitic inductances, originate mainly from the LGA package of the transistor, are included as inductors in series with the three terminals; parasitic resistances arises from die and package of GaN HEMT are also lumped and included in the circuit model.

4.2.1.2 Circuit model of GaN GIT

The basic operation principles of GaN GIT, as introduced in [4-14], resembles that of either a Si JFET or a Si MOSFET, with additional features of its own caused by differences in GaN and Si technologies. Apart from the basic operation mechanisms, similarities and differences in other electric characteristics such as parasitics, reverse conduction behaviors, etc. also arise between GaN GIT and Si MOSFET/JFET, attribute to both the designed die structure and adopted packaging technology for GaN GIT.

Fundamental operation mechanisms of GaN GIT, determined by its die structure, can be considered as either an enhancement-mode JFET or an enhancement-mode MOSFET, with the ability of conductivity modulation. With a positive bias between gate and the AlGaN/GaN interface, GIT operates as a FET and conducts current, once gate threshold voltage (V_{th}) is exceeded. As

demonstrated in Figure 4.12, GaN GIT utilizes an p-AlGaN layer over the AlGaN/GaN interface to lift up the potential of gate with respect to transistor channel i.e. enable the normally-off operation, a p-n junction is formed thereby between p-AlGaN and n-AlGaN layers [4-12]. The transistor stops behaving as a FET when the positive bias reaches the forward build-in voltage of the gate p-n junction, further increase in V_{gs} overcomes the p-n barrier leading to current flow i.e. hole injection from gate to transistor channel; the injected holes induce the same number of electrons and thereby results in increased drain current with lowered on-resistance (conductivity modulation); removing the positive bias would stop the hole injection and cause drop of V_{gs}, which starts turn-off of the transistor [4-13] [4-14]. Fundamental operation mechanisms of GaN GIT are represented by an ideal enhancement mode MOSFET together with an ideal p-n diode between gate and source. It should be noted that, resulting from the symmetric-like geometry of GaN GIT, the transistor will operate as a FET with the characteristic of conductivity modulation by either a positive V_{gd} or V_{gs}. Circuit modeling on the fundamental operation mechanisms shown in Figure 4.13 stands for the case of operating GIT with a bias of V_{gs} i.e. forward conduction. The case of a positive bias of V_{gd} is considered in conduction of gate-drain diode and reverse conduction of the device, which will be discussed later.

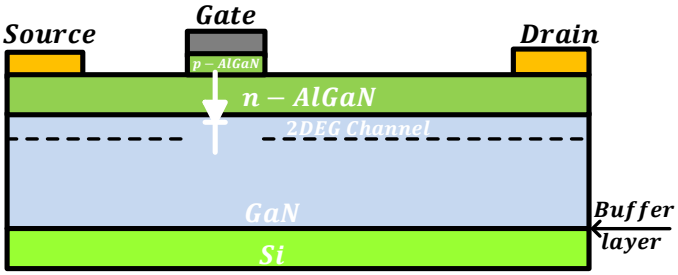


Figure 4.12 P-N junction between gate and 2DEG channel in a GaN GIT [4-13]

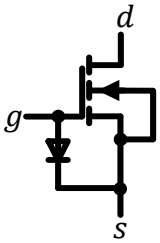


Figure 4.13 Circuit model representing fundamental operation mechanisms of GaN GIT

Gate-channel diode of GaN GIT, as already explained, can also conduct current from gate to drain if a positive bias beyond V_{th} is placed between the two terminals. Furthermore, similar to properties of the two different diodes in normally-off GaN HEMT, as length of drain-side channel is not exactly the same as that of source-side, conduction of current from gate to source and drain can be treated as two separate diodes (as illustrated in Figure 4.14). Similar to the case with GaN HEMT, the two diodes in GaN GIT have the same build-in potential but different on-

state resistance. The build-in potential depends on the p-n junction at between gate and the 2DEG channel. On-state resistance of D_{gd} (involves gate-channel junction resistance and drain-side channel resistance) is higher than that in D_{gs} (comprised by gate-channel junction resistance and source-side channel resistance)

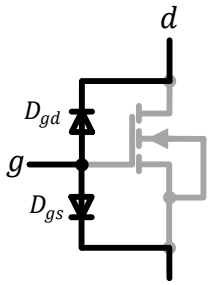


Figure 4.14 Equivalent diodes in circuit model of GaN GIT

Parasitic capacitances, lumped as discrete capacitors as illustrated in Figure 4.15, can be found between terminal metal layers (C_{gs1}, C_{gd1}, C_{ds1}), which is regarded as constant with V_{ds}, and between metal layers and transistor channel (C_{gs2}, C_{ds2}, C_{gd2}, C_{gc}), which are voltage-dependent. Gate-channel capacitance C_{gc} in GaN GIT is lumped from both gate metal to transistor channel and p-AlGaN layer to transistor channel. This capacitance, similar to the counterpart in GaN HEMT, can be gate to source, gate to drain or shared, depending on the node conditions [4-14] [4-15]. As the approach taken with GaN HEMT, the capacitances are lumped as represented by capacitors C_{gs}, C_{gd} and C_{ds} in the circuit model of GaN GIT. Similar to the case of normally-off GaN HEMT, parasitic capacitances also present between metal layers/transistor channel and the Si substrate, contributing to effective capacitance values of the transistor.

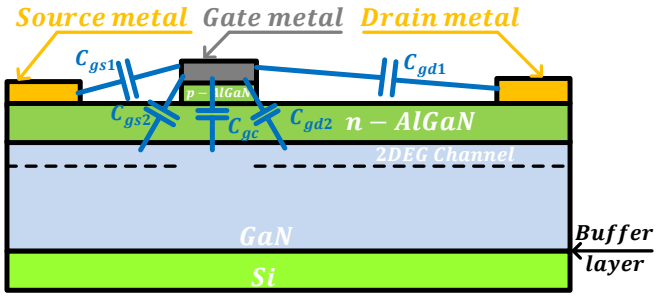


Figure 4.15 Schematic illustrations of capacitance sources

Table. 4-2 parasitic capacitances in a GaN GIT

Capacitance	Description	Note
C_{gs1}	Gate metal to source metal capacitance	Constant
C_{gs2}	Gate metal to source side channel capacitance	Voltage-dependent
C_{ds1}	Drain metal to source metal capacitance	Constant Not shown in Figure 4.15
C_{ds2}	Source to drift region capacitance	Voltage-dependent Not shown in Figure 4.15
C_{gd1}	Gate metal to drain metal capacitance	Constant
C_{gd2}	Gate to drain side drift region	Voltage-dependent
C_{gc}	Gate to channel capacitance	Voltage-dependent

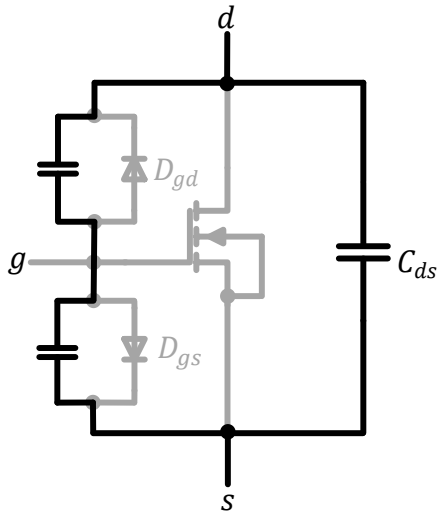


Fig 4.16 Parasitic capacitances represented by capacitors between the terminals

Reverse conduction of GaN GIT is made possible with a positive V_{gd}, as already explained. This positive bias should also be beyond V_{th} so that sufficient electrons are accumulated to conduct current in reverse direction. Besides, conductivity modulation also happens when transistor is conducting in reverse direction. Once the positive V_{gd} overcomes the p-n barrier, gate diode starts to conduct current from gate to drain, injecting holes to transistor channel and consequently leads to conductivity modulation. Like the case with a normally-off GaN HEMT, voltage across GaN GIT when it is conducting current in reverse direction can be estimated through (4.1). The advantage of exemption from reverse recovery loss in reverse conduction is also true with GaN GIT.

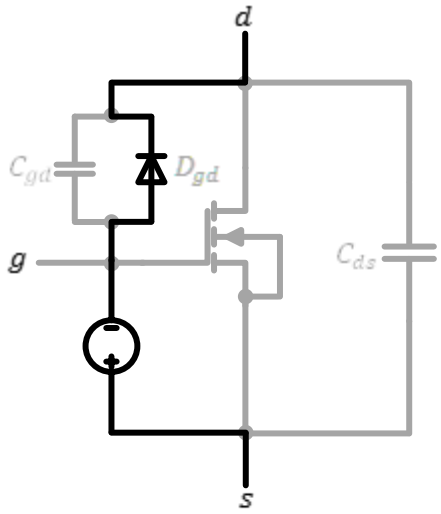


Figure 4.17 Reverse conduction mechanism of GaN GIT

Parasitic inductances and resistances of GaN GIT, like counterparts in a normally-off GaN HEMT and a Si MOSFET, origin from both the die and package of the device**.** GaN GIT, as shown in Figure 4.18, is packaged in standard TO-220, a through-hole packaging approach that is commonly used for Si MOSFET [4-16]. A TO-220 packaged Si MOSFET is traditionally executed by the approach illustrated in Figure 4.19: transistor die is attached to a lead frame, which provides electrical connection for drain, mechanical support for the die and a heat path for dissipating heat in the die. Source and gate connections to outside circuit are accomplished through wire-bonds between the MOSFET die and the lead frame [4-17]. Both the lead frame and wire bonds contribute to parasitic inductance and resistance, of which the parasitic inductance from the former dominating. Since a TO-220 package brings long leads which are closed placed, with a time-varying (in both amplitudes and directions) current, magnetic coupling effects between the leads will also contributes to effective parasitic inductances in a MOSFET. Parasitic inductances in GaN GIT, considering similarities in packaging approaches between Si MOSFET and GaN GIT that leads to similar sources of parasitic elements, are modeled as lumped self and mutual inductances as illustrated in Figure 4.20. Moreover, parasitic resistances that source also from both die and package are lumped into R_{dson} (not shown in Figure 4.20, but will be included in conduction loss calculation) and R_g, as treated of counterparts of GaN HEMT.

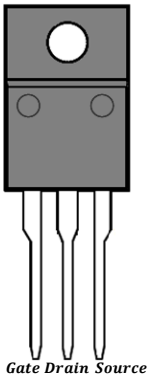


Figure 4.18 TO-220 packaged GaN GIT [4-16]

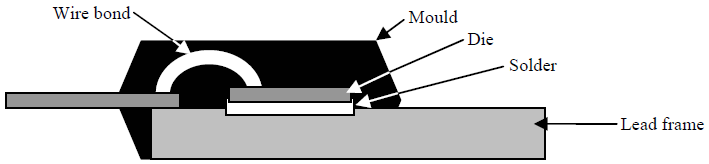


Figure 4.19 Cross-section of a conventional packaging approach [4-17]

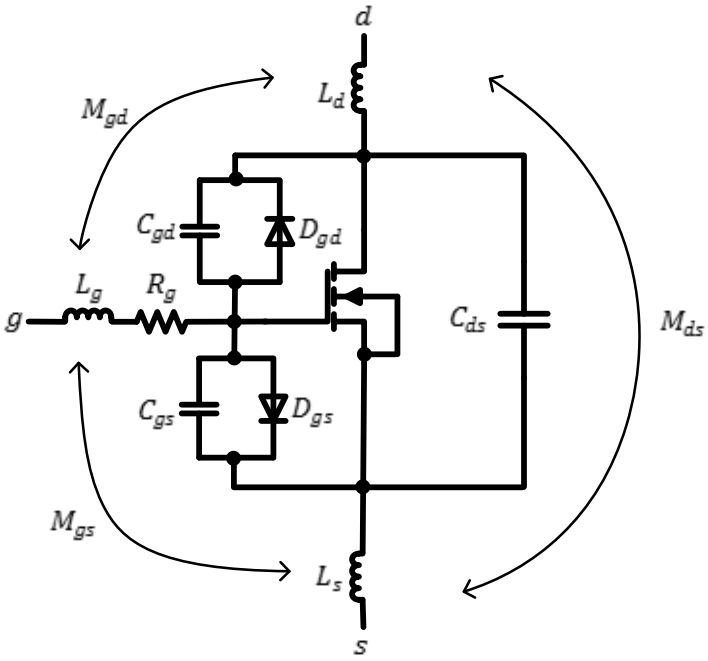


Figure 4.20 Circuit model of GaN GIT

To sum up, following the approach of circuit-model development of normally-off GaN HEMT, a circuit model of GaN GIT is built (shown in Figure 4.20) according to die and package properties of the device: basic operation principles of GIT is represented by a circuit model of an enhancement-mode MOSFET together with a p-n diode between gate and source. Current conduction property from gate to drain is symbolized as a diode between the two terminals. Parasitic capacitances are lumped between different terminals of the transistor. Self and mutual

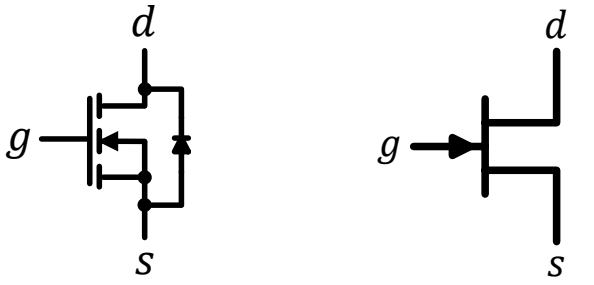
parasitic inductances of the TO-220 package leads and bonding wires are lumped and placed in terminals. Like with GaN HEMT, parasitic resistance that stem from both die and package of the transistor are also included.

4.2.1.3 A general equivalent circuit model for both normally-off GaN HEMT and GaN GIT

Comparing the circuit model for normally-off GaN HEMT in Figure 4.11 with that for GaN GIT in Figure 4.20, the two circuit models resemble to each other. The main differences between the two models come from characterization of gate-drain and gate-source diodes and accounting of the inductive elements. In GaN HEMT, the metal-semiconductor junction between gate and 2DEG channel leads to a Schottky gate-channel diode and, accordingly, both gate-drain and gate-source diodes in GaN HEMT are Schottky ones. On the other hand, determined by the p-n junction between gate and the 2DEG channel, gate-channel diode and thereby gate-drain and gate-source diodes in GaN GIT are of p-n type. From the perspective of circuit operation, a p-n diode and a Schottky diode has the same function and differences of in-circuit performance lie mainly in the electric parameters (such as on-state resistance and built-in potential) of the two devices. And thus, in the circuit model of GaN HEMT, the Schottky diodes can be replaced by p-n ones, with its original parameters be maintained. With parasitic inductances, magnetic coupling effects also exist in package of GaN HEMT. The developed circuit model for GaN HEMT in Figure 4.11 did not include magnetic coupling effects because, with the particular GaN HEMT package exampled in Figure 4.9, values of coupling factors are negligible. This actually is one special case i.e. the coupling coefficients M_{gd}, M_{gs} and M_{ds} are set to be zero. A more general circuit model for GaN HEMT should include the magnetic coupling effects. And therefore, the circuit model developed for GaN GIT in Figure 4.20 can be regarded as a general equivalent circuit for both devices.

The developed general equivalent circuit model is different from the models provided by producers of the devices. Circuit model of GaN HEMT provided by manufactures, as shown in Figure 4.21 (a) uses a MOSFET to represent basic operation mechanism and an anti-paralleled diode to indicate the capability of reverse conduction. This model in Figure 4.21 (a) resembles well with the general circuit model in Figure 4.20, main differences are: a) existence of the gate-channel diode, which in theory would conduct but in practice will not (as will be explained in 4.2.1.4); b) parasitic elements are not included in the circuit model, although they are accounted for in the spice model provided by the manufacture [4-18]. Circuit model for GaN GIT is also available from provider, which is shown in Figure 4.21 (b). The model consists only of a symbol of JFET, which is not a reflection of actual operation principles, as GIT is a normally-off device. The model does not imply reverse conduction property of the transistor and the characteristic of gate-channel diode. Moreover, parasitic elements are missing from the circuit model. And thus, models from manufactures did not include all electric characteristics of the devices, especially the ones

that affect loss in the transistor. Given the fact that, in this thesis, the circuit model is to be used for the purpose of analytical loss modeling of GaN transistors, the developed model in Figure 4.20 is adopted.



(a) **(b)**

Figure 4.21 GaN transistor circuit models provided by manufactures

(a) Normally-off GaN HEMT [4-7]; (b) GaN GIT [4-15]

4.2.1.4 Discussion

Conductivity modulation of normally-off GaN HEMT

It should be noted that, theoretically, GaN HEMT also has the capability of conductivity modulation when built-in potential of its gate-channel diode is overcome and holes are injected into transistor channel by a positive bias of either V_{gs} or V_{gd}. The property of conductivity modulation in GaN HEMT is not considered because: a) due to large transconductance of the transistor, a V_{gs} smaller than build-in potential of the gate-channel diode is sufficient to conduct high current with low R_{dson}; b) conduction of gate-channel diode requires a bias close to the maximum allowed gate voltage, which is, in most cases, avoided. To give an example: a 200V GaN HEMT has a built-in gate-channel potential of ~5V while it can conduct a current as high as 60A with an R_{dson} of about 25mΩ when V_{gs} is around 4V [4-19]. Meanwhile, the absolute maximum gate voltage is 6V. And thus, the conductivity modulation character is not considered when it comes to GaN HEMT in this thesis.

Limitations of the general equivalent circuit model

It should also be pointed out that not all electric characteristics of the device are included in the circuit model e.g. the nonlinear transconductance of the device [4-1] [4-20]. For the electric features of the transistor that are involved in the circuit model, characteristics such as parasitic capacitance of the package are also omitted. The developed circuit model for GaN transistors is to be used for analytical loss modeling so as to, as already discussed in introduction part of this chapter, perform loss analysis of the transistors. And thus, reasonable simplifications are acceptable as long as satisfying accuracy can be achieved. Besides, critical electric elements that were believed to affect switching or/and conduction loss are all accounted for in the circuit model

[4-3] [4-21] [4-22]. What is more, despite the separation of die-related and package-related parasitics in developing the circuit model for GaN transistors, practical measurements on voltage and current results can only be performed on/through device packages. Consequently, the measured voltage and current values are not always in line with the actual corresponding values on the die, although the measured and calculated losses should be.

4.2.2 Equivalent circuit of a GaN based boost converter

It has already been well acknowledged that performances of GaN transistors e.g. switching loss, voltage and current stress, etc. are greatly influenced by electric properties of the circuits such as circuit operation modes, parasitic elements, etc. in which the transistor operate [4-3] [4-22]. As a result, clarification of the electromagnetic environment of a GaN transistor should be a prerequisite in characterizing switching transients of the device [4-23]. In particular, electromagnetic volume of the GaN HEMT is negligibly small compared to the rest parts of a power circuit, environment has profound influence on switching behaviors and losses of the transistor and must be well defined and specified [4-23].

Two different types of hardware platforms, Double Pulse Tester (DPT) and demonstrative converter, are commonly used for evaluating switching characteristics and losses of GaN transistors. As detailed in [4-24], a DPT basically is an inductive load buck converter, which utilizes a two-pulse train in one relatively long switching cycle to drive the transistor. With the widths of both pulses and the interval in-between adjustable, the devices can be tested at any desired voltage and current levels. It is believed that DPT have merits of simple design of layout, low thermal stress on device under test (DUT), convenient for excluding temperature-dependent characteristics, etc. [4-20] [4-25]. In a DPT, switching behaviors of DUT are supposed to be characterized without the influences of circuit parasitic elements i.e. minimization of circuit parasitic elements is needed, which may leads to a loss of the benefit of simple design [4-26]. Moreover, DPT enables only a mimic of operations of a DUT in real applications, whether operation patterns of the DUT will be the same (in a DPT and a real converter) is questionable, especially with the newly developed GaN transistors, of which the properties are unknown. On the other hand, in demonstrative converters, transistors are operated in line with reality and more insights into performance of the transistors in real applications can be offered once electromagnetic surroundings of the devices are properly defined and characterized.

A boost converter, which is the most popular topology in PFC solutions as demonstrated in Figure 4.22, is employed as a platform for exploiting potentials of GaN devices in this thesis. Similar to the case with GaN transistors, the rest components in a PFC boost converter i.e. boost inductor, freewheeling diode and output capacitors, are also not ideal and have parasitic elements with them, which may affect losses in GaN transistors. Parasitic elements in these components

originate from various kinds of sources such as semiconductor die properties and package, manufacturing approach of passive components, etc.

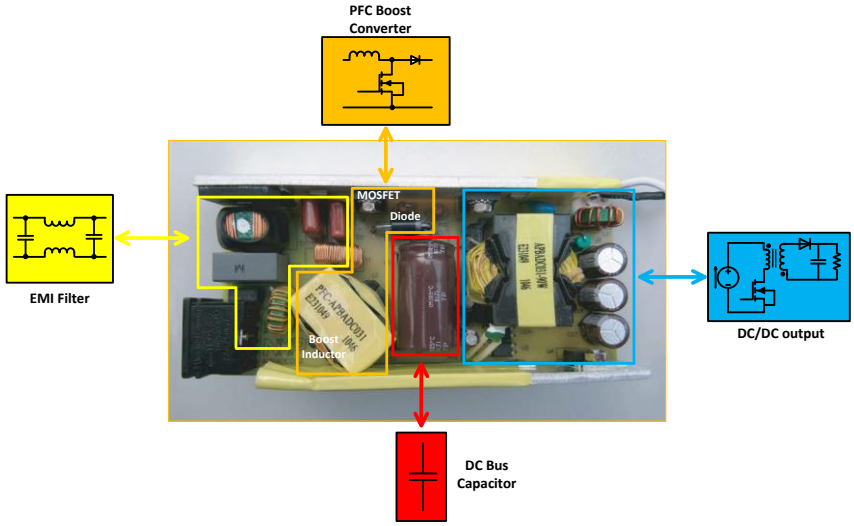


Figure 4.22 A 90W AC/DC converter with boost converter as PFC stage [4-27]

Inductor in a PFC boost converter can be implemented in many different ways. The inductor is usually realized as a discrete device, although there are also approaches of integrating the inductor with other parts such as EMI filter as proposed in [4-28]. With a discrete inductor in PFC boost converter, different implementation methods are made available by a variety of technologies involved such as magnetic core material, shape and size, winding type and material, etc. [4-27] [4-29] [4-30]. In a discrete inductor, parasitic capacitances distribute between the winding turns (turn-to-turn capacitance), winding layers (layer-to-layer capacitance), and between the winding and the core of the inductor (winding-to core capacitance) [4-31]. Besides, conductor of the winding has resistance that is, due to skin effect and proximity effect, frequency dependent and cause losses. Loss in the inductor will also be induced in its magnetic core with the flow AC current through the inductor. As discussed in both [4-31] and [4-32], a simple model as shown in Figure 4.23 can be used to characterize properties of an inductor in high frequency operations. In inductor circuit model, L represents the inductance while C_L indicates the equivalent lumped capacitance and R_L stands for winding and core loss that are generated with flowing of AC currents. It worth be pointed out that C_L can be minimized by actions such as constructing single-layer inductor to avoid layer-to-layer capacitance, connecting multiple inductors in series to reduce effective overall capacitance, etc. [4-33] [4-34].

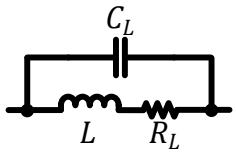


Figure. 4.23 Circuit model of inductor

Freewheeling diode in a traditionally Si transistor based PFC boost converter is also a Si one, which inevitably introduce reverse recovery charge in CCM, leads to increased turn on loss and current stress in the transistor and deteriorate EMI performance of the converter [4-35]. When it comes to application of GaN transistors in CCM PFC boost converters, the situation got even worse given the facts that GaN has a fast switching speed (high di/dt) and maximum reverse-recovery current, recovery time, and recovered charged all increases with the increment of current-changing rate. Advances in alternatives diodes using other materials, in particular the commercial availability of the reverse-recovery-charge free SiC diodes, help to combat the problems. In fact, a SiC diode usually needs a displacement current to charge the metal-semiconductor-junction capacitance when it is forced- off and thus still affects turn on loss of the transistor [4-36]. Besides, SiC diodes have higher conduction loss than Si counterparts (regular p-n type) in the same operation conditions as they show larger forward voltage drop. Consequently, when operated in BCM and BCM-VS where no reverse-recovery current will be generated, Si diodes are preferred. Regardless of the type of diode adopted, the circuit model in Figure 4.24 can be used to characterize behaviors of the diodes. The model consists of a diode D (which could be Schottky or p-n with certain build in voltage and on-state resistance), a capacitor (C_D) paralleled to the diode to indicate the reverse recovery effect of Si diode or the junction that will be charged (when it is switched off) or discharged (when it is switched on) in a SiC diode. Besides, parasitic inductance caused by both die and package of device is lumped in the circuit model as L_D.

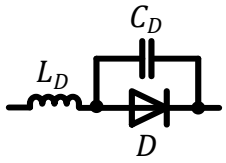


Figure 4.24 Circuit model of the freewheeling diode

Capacitor paralleled to the output stage of a PFC boost converter has multiple functions: balancing the pulsating (at twice the line frequency) input power and the constant output power, reducing output voltage ripple, storing energy in case of line drop-out (in the measure of hold-up time) [4-37] [4-38]. Size and value of the capacitor, accordingly, are affected by these factors, of which hold-up time requirement is the major determinant. Lots of efforts have been devoted to provide proper circuit models for capacitors and investigate boundaries of the models. A capacitor, according to results from the efforts, can be modelled in a variety of ways such as lumped RLC, lumped high order RLC network, distributed model, transmission line model, etc. depending on issues such as capacitor manufacturing and packaging technology, operation frequency of application, design criteria of the application, etc. As discussed in [4-39] ~ [4-42], some general guidelines on determining the proper modelling approach exist. When parasitic inductance of

capacitor package and/or connection (with the rest parts of a circuit) dominates over the inductance caused by the current path through the capacitor, a lumped RLC model in Figure 4.25 is adequate to characterize performance of the capacitor even at high frequency. When both package and connection inductances are low in comparison to the current-path inductance of the capacitor itself, if the switching transient time of capacitor current is long (far beyond the time period of capacitor's first resonant frequency), the lumped RLC model is still sufficient; otherwise, more advanced circuit model e.g. distributed model [4-41] and transmission-line model [4-39] is needed.

Nowadays, capacitors with low-inductance packages e.g. SMD electrolytic capacitors, leadless multilayer capacitors (MLC), etc. are increasingly common. Besides, low interconnect inductance designs, such as low-inductance laminated bus bars and careful low-inductance PCB layout to mount capacitors as close to the rest parts of the circuit as possible, are also becoming more popular, especially for high frequency applications [4-39]. In implementation of PFC boost converters, however, leaded electrolytic capacitors (as exampled in a commercial 90W AC/DC notebook adapter in Figure 4.22) are widely used mainly because of its large capacity and low cost, although there are also attempts of using alternatives e.g. film capacitors combined with an active power decoupling circuit [4-37] [4-43]. Moreover, in practice, the output capacitor is not placed directly between cathode of the freewheeling diode and source terminal of the transistor as design trade-offs may exist between placement of the capacitor and other components. Accordingly, connection inductance is also not negligible. And thus, in an equivalent circuit of a typical PFC converter, the simple RLC model can be used. In this thesis, multiple multilayer ceramic capacitors (MLCC) are paralleled as output capacitor in a PFC boost converter. The paralleling leads to reduced effective inductance in the capacitors, although the value is already quite small in each single MLCC. Furthermore, the MLCCs are connected to the circuit through PCB traces leading to parasitic inductance that is larger than effective self-inductance in the capacitors. And therefore, the simple RLC model is also adopted for circuit modelling of MLCC.

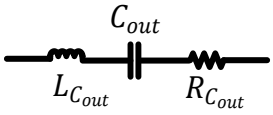


Figure 4.25 Circuit model of output capacitor in a PFC boost converter

To operate as a converter, the components need to be properly connected by certain circuit carriers such as PCB, DBC (Direct Bonded Copper), etc. Circuit carriers provide mechanical support for the components and implement electrical interconnections between them. The interconnections e.g. conductive traces, pads, etc. have parasitic inductances and resistances that may influence switching behaviors of the transistor in a similar way as the corresponding elements of the device package, especially in high frequency operations. Furthermore, in a

multilayer circuit carrier, parasitic capacitance arises among conductor traces between different layers and, depending on factors such as material properties and thickness of the intermediate dielectric layer, values (and influences) of the capacitors varies. In a PFC boost converter, the most commonly used circuit carrier (and also, what is used in this thesis) is PCB and interconnections are fulfilled by copper traces, pads and vias. Parasitic inductances of the interconnections are lumped as inductors between the main components (boost inductor, transistor, diode, output capacitor) in the equivalent circuit of the PFC boost converter in Figure 4.26. It should be noted that driving part of the GaN transistors is modeled as an ideal pulse voltage source (resembling output of the gate driver) in series with a resistor (representing output resistance of the gate driver). Parasitic inductances originate from conductors connecting the transistor to its driving source are also added. Parasitic capacitances caused by the interconnections are not shown (but will be considered according to their physical locations and values in GaN based PFC boost converters that are to be built in this thesis), while resistances of interconnections are omitted as the values are usually negligible.

Table. 4-3 Parasitic inductances of interconnections on PCB of a PFC boost converter

Inductance	Description
$L_{L\text{-}A}$	Inductance of connection between boost inductor and switching node A
$L_{A\text{-}D}$	Inductance of connection between freewheeling diode and switching node A
L_{cd}	Inductance of connection between GaN transistor and switching node A
$L_{D\text{-}Cout}$	Inductance of connection between freewheeling diode and output capacitor
L_{cs}	Inductance of connection between GaN transistor and switching node B
$L_{dr\text{-}g}$	Inductance of connection between gate driver and GaN transistor
$L_{dr\text{-}B}$	Inductance of connection between gate driver and switching node B
$L_{Cout\text{-}B}$	Inductance of connection between output capacitor and switching node B

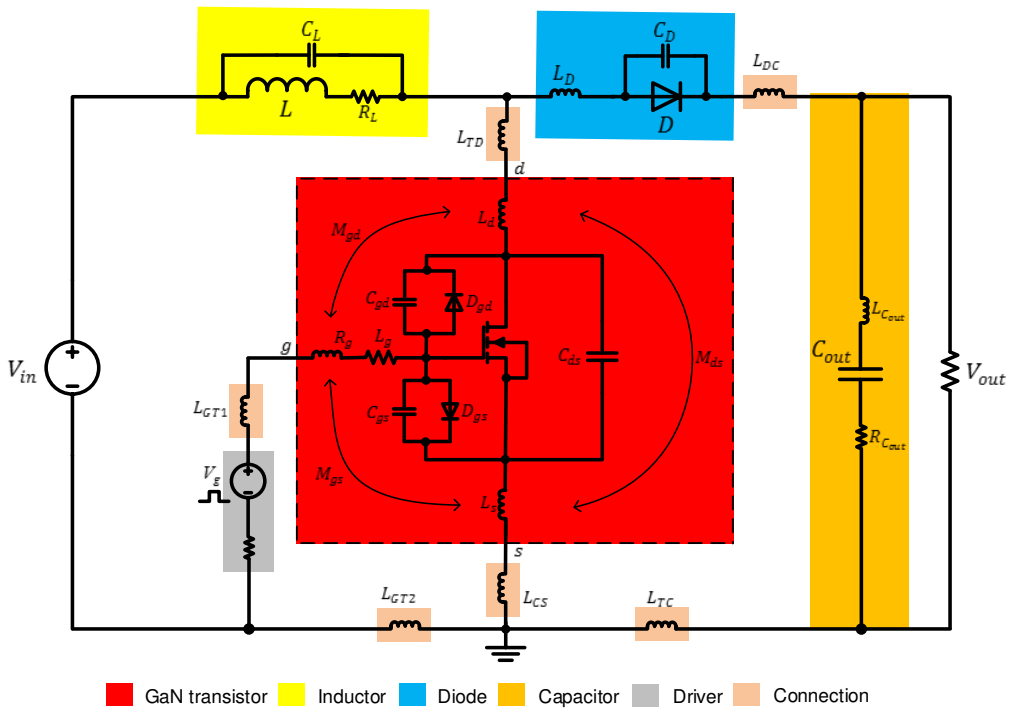


Figure 4.26 Equivalent circuit of a GaN-transistor based PFC boost converter

Moreover, to properly run the converter, issues such as thermal management, EMI performance, etc. have to be taken care of. Corresponding actions on these issues may affect behaviours of the transistor and performance of the converter, and the effects need to be examined and included after the practical implementation of the converter. For instance, mounting a heatsink to a TO-220 packaged GaN transistor that has a 3 cm^2 copper pad on drain terminal would result in a parasitic drain-source capacitance that is comparable to that in the device itself [4-23].

4.3 Analytical loss modelling of GaN transistors in a boost converter

With the developed equivalent circuit of a GaN based boost converter, expressions of voltage on GaN transistor and current flowing through the device, and switching and conduction losses therefore, can be derived using circuit laws. The derivations should be conducted in accordance with operation mechanisms of the transistor as well as that of the converter during switching transients and on-state. Besides, in many cases, reasonable simplifications and assumptions made to the components and them in-circuit operations in terms of switching behaviours, values of parasitic elements, etc. would relieve the complexity of the loss model and ease the task of uncovering critical device and circuit elements affecting losses in the devices, at the expense of certain accuracy.

4.3.1 Loss modelling of GaN transistors in a boost converter

4.3.1.1 Loss modeling approach

Switching loss and conduction loss of a GaN transistor are to be modeled by deriving voltage and current expressions in switching transients and conduction period of the transistor, respectively. Basic operation mechanisms of the transistor can be briefly described as: when transistor is off, current i_L flows from input through the inductor and freewheeling diode to the output, charging the output capacitor and supplying load current; during turn-on, the transistor takes over the inductor current from the freewheeling diode and voltage across the transistor falls; throughout on-time, current through the transistor increases linearly; during turn-off, voltage on the transistor increase up to V_{out}, inductor current commutates from transistor to diode. In turn-on and turn-off transients, switching currents are assumed to be constant as I_{on} and I_{off}, respectively, because of the facts that: a) the currents flow through a large boost inductor and therefore cannot change instantly; b). GaN transistors are fast-switching devices (in the range of nanoseconds), the periods of switching transients are small compared to the switching cycle of the converter even at high frequency (MHz).

The developed equivalent circuit in Figure 4.25 is a relatively comprehensive one that includes proper high frequency models of the main components in a boost converter as well as circuit parasitic elements. Given the purpose of performing loss modeling of GaN transistors, the equivalent circuit can be further simplified on the basis of characteristics of the transistor, operation mechanisms and practical implementation of the converter:

- Loss in the boost inductor is considered not relevant to that of the transistor and therefore, the element R_L is omitted; parasitic capacitance of the inductor is to be minimized by using multiple single-layer inductors connected in series, the values are negligible small compared to the capacitances of the transistor and are therefore neglected.
- MLCCs, of which parasitic resistance (ESR) and inductance (ESL) are small, will be used as output capacitors. Furthermore, multiple MLCCs are paralleled together to provide the required inductance and further reduce effective ESR and ESL. As will be discussed during loss model validation, the estimated value of parasitic inductance is not comparable to the connection inductance. Besides, since, during current commutations, switching currents also flow through the output diode that have a much higher resistance than the parasitic inductance in the MLCCs, influence of ESR can be disregarded. In extreme conditions where parasitic inductance of circuit connections is negligible and inductance of the capacitors may need to be considered, as the example in [4-23] where capacitors are directly mounted onto a transistor, estimation on the inductance value in MLCC capacitors can be performed through the same approach applied in [4-23].

- SiC diode, which has no reverse recovery effect, will be used in both modelling and validation. As already discussed, the metal-semiconductor-junction needs to be charged when a SiC diode is forced-off and discharged when it is switched-on by displacement current. And therefore, the capacitor in the circuit model of the freewheeling diode stands only for the capacitance of the diode.
- In switching transients, as inductor current is constant, current commutates between transistor and diode, and $L_{L\text{-}A}$ has no effect on switching loss. In conduction, where variation of current is determined by effective inductance of the current loop, boost inductance dominates over the parasitic inductances, contribution of $L_{L\text{-}A}$ on the current and conduction loss therefore can be neglected. In a word, $L_{L\text{-}A}$ can be excluded as it hardly has effects on transistor loss.
- Temperature-sensitive characteristic of GaN devices, such as on-state resistance, gate threshold voltage, etc., would make losses in the device are temperature-dependent. With V_{th}, in GaN HEMT, the value increases nearly linearly from 1.4V at 25°C, by only 4%, to 1.46V at 125°C (the maximum-allowed temperature) while in GaN GIT, corresponding information is not available. The effects of temperature on gate threshold voltage in GaN transistors are therefore not considered in the loss model. With R_{dson}, both transistors showed linear-like dependence on temperature (GaN HEMT from ~25 mΩ at 25°C to ~40 mΩ at 125°C, GaN GIT from ~75 mΩ at 25°C to ~155 mΩ at the maximum allowed temperature of 150°C). The effects of the temperature on on-state resistance and conduction loss are included by using the average values of resistance over the aforementioned temperature span.

Moreover, in loops of both gate current and drain-source current during switching transients, some parasitic resistive and inductive elements can be combined into one. Gate current loop (gate loop) consists of the driving source V_g, capacitor-diode/gate-source and parasitic inductance $L_{g\text{-}GaN}$, $L_{dr\text{-}GaN}$, $L_{dr\text{-}B}$ (can be combined as L_g) and L_{cs}, $L_{s\text{-}GaN}$ (merged as L_s). Drain-source current circulating loop (commutation loop) is comprised by the transistor (drain-source), freewheeling diode, output capacitor and parasitic inductances $L_{d\text{-}GaN}$, L_{cd} (combined as L_d), $L_{A\text{-}D}$, $L_{D\text{-}Cout}$, $L_{Cout\text{-}B}$ (treated together as L_{out}) and L_{cs}, $L_{s\text{-}GaN}$ (shared with gate loop, termed as common source inductance L_s). The final simplified equivalent circuit in Figure 4.27. It should be noted that, to ease description of voltage and current, g,d, and s are rearranged so that when it comes to variables such as v_{ds}, actual voltage/current across/in transistor die are denoted. Parasitic elements that are included in the final equivalent circuit and the loss model are summarized in Table 4-4.

Table 4-4 Parasitic elements included in loss model

Parasitic element		Model in equivalent circuit
Transistor parasitic capacitances	Gate-source capacitance	C_{gs}
	Gate-drain capacitance	C_{gd}
	Drain-source capacitance	C_{ds}
Transistor package inductances	Parasitic inductance of gate terminal	Part of L_g
	Parasitic inductance of drain terminal	Part of L_d
	Parasitic inductance of source terminal	Part of L_s
	Mutual inductance between transistor terminals	M_{gs}, M_{gd} and M_{ds}
Transistor parasitic diodes	Gate-source diode	D_{gs}
	Gate-drain diode	D_{gd}
	Drain-source diode	D_{ds}
Circuit parasitic inductances	Parasitic inductance of interconnection between transistor and freewheeling diode	Part of L_d
	Parasitic inductance of interconnection between gate driver and transistor gate terminal	Part of L_g
	Parasitic inductance of shared interconnection between gate driver- transistor source terminal path and output capacitor-transistor source terminal path	Part of L_s
	Parasitic inductance of interconnection between freewheeling diode and output capacitor	Part of L_{out}
	Parasitic inductance of interconnection between output capacitor and transistor source terminal (not shared)	Part of L_{out}
Parasitic elements of freewheeling diode	Parasitic inductance of the freewheeling diode	Part of L_{out}
	Parasitic capacitance of the freewheeling diode	C_D

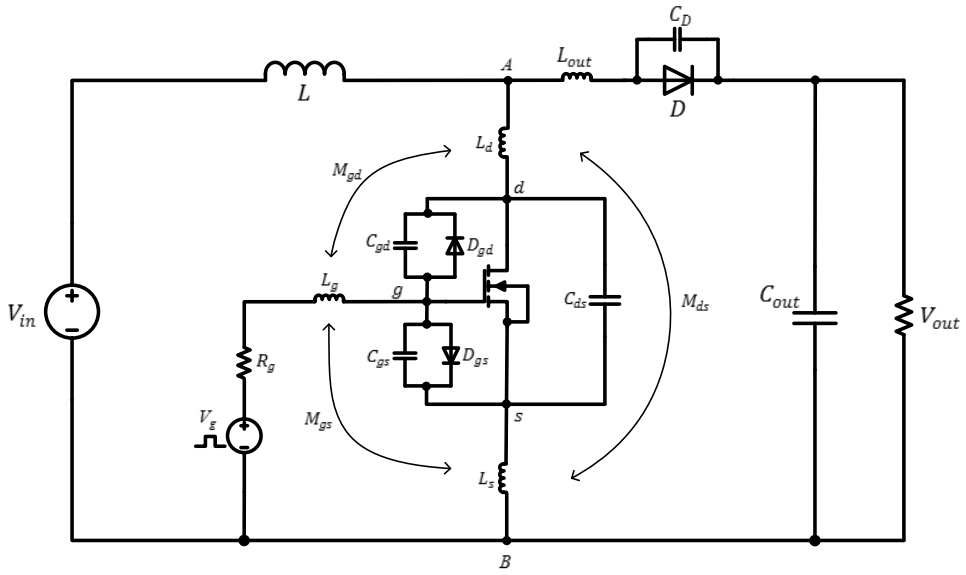


Figure 4.27 Simplified circuit of a GaN based boost converter

4.3.1.2 Analytical loss model

Switching transients of a GaN transistor is divided into different stages and sub-stages, similar to the approach of characterizing switching behaviors for Si MOSFET [4-1] [4-21]. Qualitative operation waveforms of a GaN transistor, which indicate stages and substages in switching transients and conduction state, are illustrated in Figure 4.28. Values of parasitic elements are modeled differently according to the conditions such as v_{ds} variation range (parasitic capacitance), current direction in package leads (parasitic inductance), etc. in each single stage or substage.

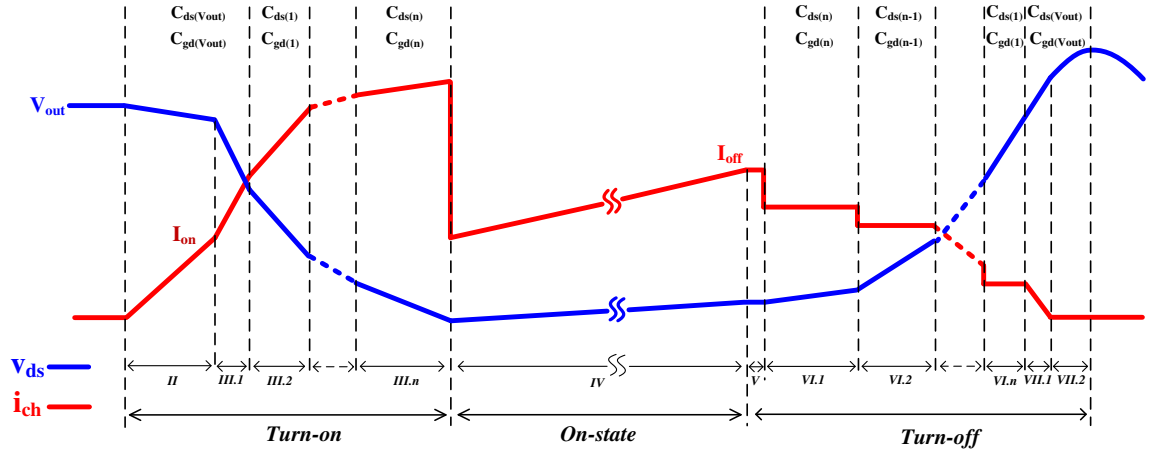


Figure 4.28 Modelled operation waveforms of a GaN transistor (Not to scale)

A. Turn-on transient

Stage I Turn-on delay

When gate voltage V_g is initiated, the resulting gate current in the gate loop starts to charge the input capacitance C_{iss} (the sum of C_{gs} and C_{gd}). As C_{gs} is usually much larger than C_{gd} when voltage across the transistor v_{ds} is high, it is assumed that only C_{gs} is charged up in this stage [4-21]. Before threshold voltage V_{th} of the transistor is reached, status of power stage doesn't change, and therefore no power loss is generated in a GaN transistor. At the end of this stage, gate-source voltage V_{gs} reaches transistor threshold voltage V_{th}.

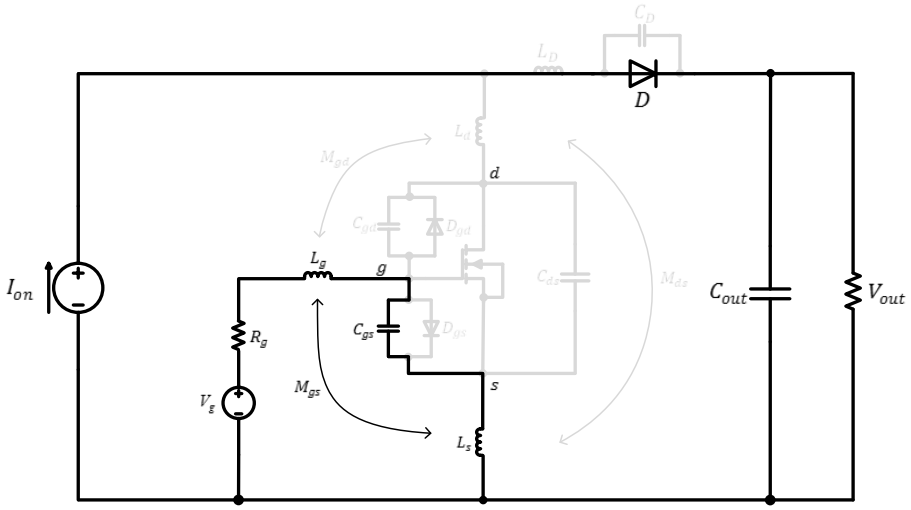


Figure 4.29 Equivalent circuit in stage of turn-on delay (I)

Stage II Channel current rise

As soon as V_{th} is reached, channel of the GaN transistor becomes conductive. Given the fact that $v_{ds} > v_{gs} - V_{th}$, transistor operates in saturation region and maximum current the channel can conduct is determined by v_{gs}, as expressed in (4.4) in which g_{fs} is the transconductance of the device. Due to time-changing current that circulates in the commutation loop, voltage drop on parasitic inductances will be induced, affecting the value of v_{ds} and losses in the transistor.

$$v_{ds-ir}(t) = V_{out} - v_{L_d}(t) - v_{L_{out}}(t) - v_{L_s}(t) \tag{4.2}$$

$$i_{ch-ir}(t) = i_{L_d}(t) - i_{sd}(t) - i_{C_{dg}}(t) \tag{4.3}$$

$$i_{ch-ir}(t) = g_{fs}[v_{gs}(t) - V_{th}] \tag{4.4}$$

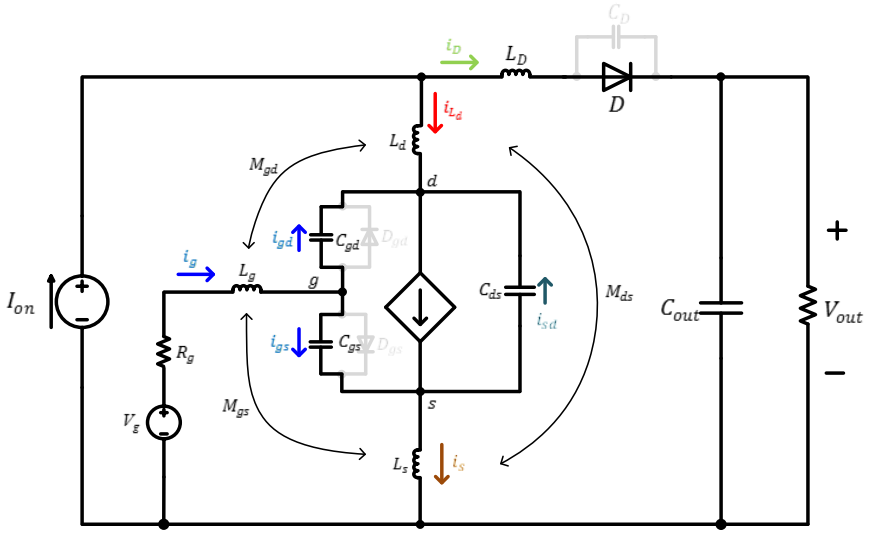


Figure 4.30 Equivalent circuit in stage of channel current rise (II)

By solving the equations of both gate loop and commutation loop for $v_{gs}(t)$ and $v_{ds}(t)$, instant values of channel current and voltage i.e. instant power loss in GaN transistor can be obtained, the expressions are quite complex though. In this paper, channel current is considered equal to drain terminal current $i_{L_d}(t)$ in this stage; the variation of v_{ds} is accounted for by adding the loss of discharging GaN transistor's output capacitance. At the end of this stage, channel of the GaN transistor takes over the whole load current I_{on} and voltage on the device is $V_{ds\,(t_{ir})}$.

Switching loss in this stage is modeled as:

$$P_{ir} = f_{sw}\int_0^{t_{ir}} v_{ds}(t)i_{Ld}(t)dt + \frac{C_{ds(V_{out})} + C_{gd(V_{out})}}{2}(V_{out}^2 - V_{ds(t_{ir})}^2)f_{sw} \tag{4.5}$$

Where t_{ir} denotes current rise time and f_{sw} is the operation frequency of the converter.

Stage III Voltage fall

After GaN transistor has taken over load current I_{on}, the freewheeling diode stops conducting and begins to block output voltage V_{out}. Voltage across the transistor starts to fall and capacitors C_{ds} and C_{gd} get discharged through transistor channel. The freewheeling diode that was forward conducting in the previous stage will shift its status to off-state during this stage. Parasitic capacitance of the diode will be charged and the corresponding current will flow through transistor channel. In commutation loop, charging process of C_D is a forced response of the discharging of transistor output capacitance, which is determined by the gate driving current. With the existence of parasitic inductances in the loop, mathematical determination on the exact charging rate of C_D is complicated. In addition, value of C_D is also dependent on instant voltage across the diode, especially under low voltage conditions. And therefore, simplifications are made to ease the

calculation. Since value of C_D is usually in magnitude of pF and values of parasitic inductance in the commutation loop should be small (in range of nH) for high frequency application, voltage drop on parasitic inductance in commutation loop, is negligible, although the charging speed (dv_D/dt) might be high (tens of Volts per nano-second). Besides, as mutual inductances are much smaller than L_{out} and given the fact that the load current is also constant as I_{on}, magnetic coupling effects between drain terminal and source/gate can be neglected in this stage i.e. $M_{gd}$and M_{ds} are be modelled as zero. Absolute value of the displacement, on the other hand, may not be negligible and should be included. Transistor loss caused by the displacement current is accounted for by:

$$P_{C_D-dis} = \frac{Q_{V_{out}} V_{out}}{2} f_{sw} \tag{4.6}$$

Where $Q_{V_{out}}$ is the charge needed to build potential across the diode up to V_{out}. Exact value of $Q_{V_{out}}$ can be obtained from device datasheet.

Since v_{ds} varies largely in this stage, nonlinearity of parasitic capacitances should be accounted for. The relationships between capacitances and v_{ds} can be approximated through curve fitting to find polynomial expressions of C_{gd} and C_{ds} as functions of v_{ds}. Although this approach could result in accurate loss calculation, as C_{gd} and C_{ds} are coupled with the time changing v_{ds}, mathematically applying the nonlinear functions will ends up with complex equations and therefore calls for simplifications [4-44]. It is reasonable to divide this stage into multiple substages according to the capacitance values in different voltage ranges and use equivalent capacitance values in each substage to calculate switching loss. Take variation of capacitance in a 200V GaN HEMT as an example, as illustrated in Figure 4.31**:** C_{gd} is almost constant when V_{ds} is between 20V and 200V, while its value changes nearly linear with V_{ds} below 20V; $C_{ds,}$ on the other hand, roughly have three different varying trends (decreasing slopes) within three voltage ranges of 0~20V, 20V~120V, and 120V~200V. Consequently, voltage-fall stage of a 200V GaN HEMT can be split into three consecutive substages and average value of capacitance in one substage can be used for loss calculation in the exact substage.

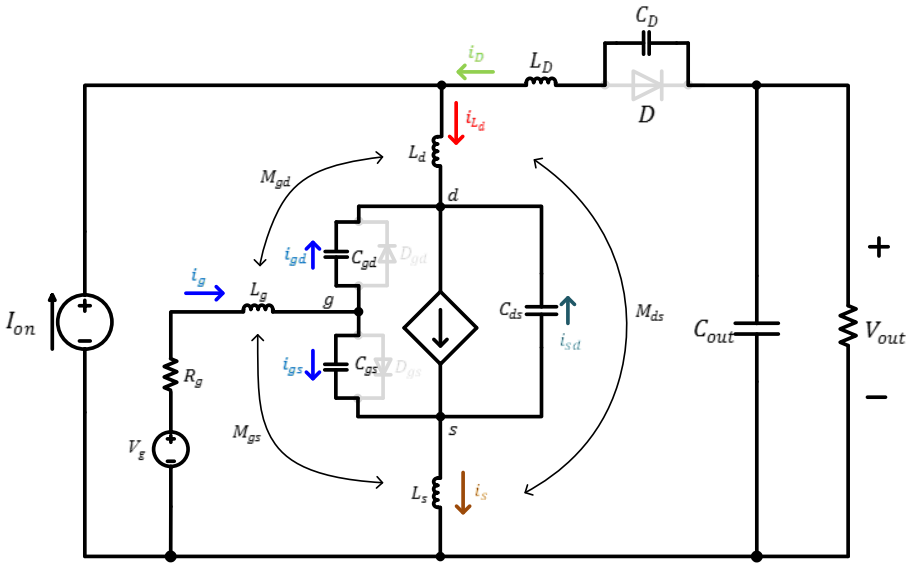


Figure 4.31 Equivalent circuit in stage of voltage fall (III)

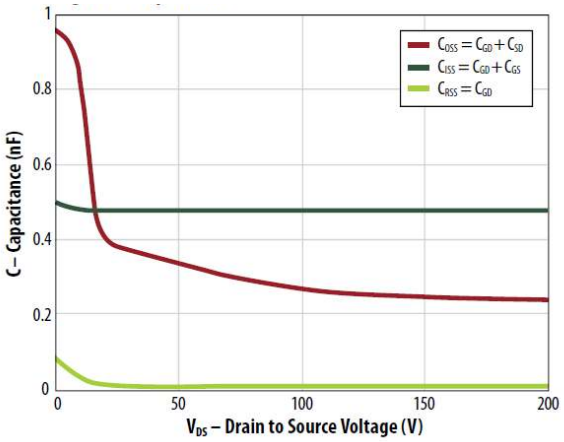


Figure 4.32 Variations of capacitance with V_{ds} in a 200V GaN HEMT [4-19]

Assuming there is a total of *n* successive substages, and initial conditions of one substage are the final status of previous substage. Rearranging equations from *Stage II* with modifications on values of channel current, mutual inductances and capacitances in each substage, expressions of channel current and drain source voltage can be obtained. Channel current in each substage, similar to expression of (4.2) in *Stage II*, is comprised of load current, discharging currents of C_{gd} and C_{ds}, and displacement current that charges C_D. The instant channel current value is determined by v_{gs} as the transistor is still working in saturation region. Expression of instant voltage can be obtained by setting v_{L_d} and $v_{L_{out}}$ as zero.

This stage ends when v_{ds} decreased to $R_{ds-on}I_{on}$, and loss in this stage can be approximated as:

$$P_{vf} = \sum_{j=1}^{n} f_{sw} \int_{0}^{t_{vf(j)}} v_{ds-vf(j)} i_{ch-vf(j)}(t)dt + \frac{Q_{V_{out}} V_{out}}{2} f_{sw} \tag{4.7}$$

Where $v_{ds-vf(j)}$, $i_{ch-vf(j)}$and $t_{vf(j)}$ stands for voltage, current and time-period in the *j-th* substage, respectively.

As will be seen in section 4.3.2, both the normally-off GaN HEMT and GaN GIT have large values of transconductance g_{fs}, and the gate-channel diodes will not conduct during switching transient until the channel currents are as high as 4~5 times the rated maximum current of the products. And therefore, the effects of gate-channel junction on turn-on loss of GaN transistors are not considered. In steady state, however, the existence of the diode is considered. After v_{ds} has dropped to $R_{ds-on}I_{on}$, v_{gs} continues to increase and, depending on the built-in voltage (V_{gsD}) of the gate-source diode D_{gs} and amplitude of the driving voltage, final value of v_{gs} (V_{gson}) and current circulating in the gate loop differs:

$$V_{gson} = \begin{cases} V_g, V_g < V_{gsD} \\ V_{gsD} + \dfrac{V_g - V_{gsD}}{R_{gon}+R_{gsD}} R_{gsD}, V_g \geq V_{gsD} \end{cases} \tag{4.8}$$

B. Turn-off transient

Stage V Turn-off delay

When the gate voltage V_g starts decreasing C_{iss} is being discharged and turn-off transient starts. As v_{ds} is low in this stage (under which condition value of C_{gd} might be comparable to that of C_{gs}) the assumption *Stage I* on handling C_{iss} is no longer valid and the combined value of C_{gd} and C_{gs} should be used to estimate the time period of this stage. Besides, without loss of generality, it is assumed that the gate-source diode D_{gs} was conducting before this stage starts. And accordingly, two different substages exist: v_{gs} will firstly drop to V_{gsD} under the influence of gate–source diode and then falls without the effects of the diode.

Substage V.1 Gate source voltage under influence of gate–source diode

In this substage, gate source voltage drops from V_{gson} to V_{gsD} by the time t_{offd1}.

$$i_{gs}(t) = C_{iss} \frac{dv_{gs}(t)}{dt} + \frac{V_g - V_{gsD}}{R_{gsD}} \tag{4.9}$$

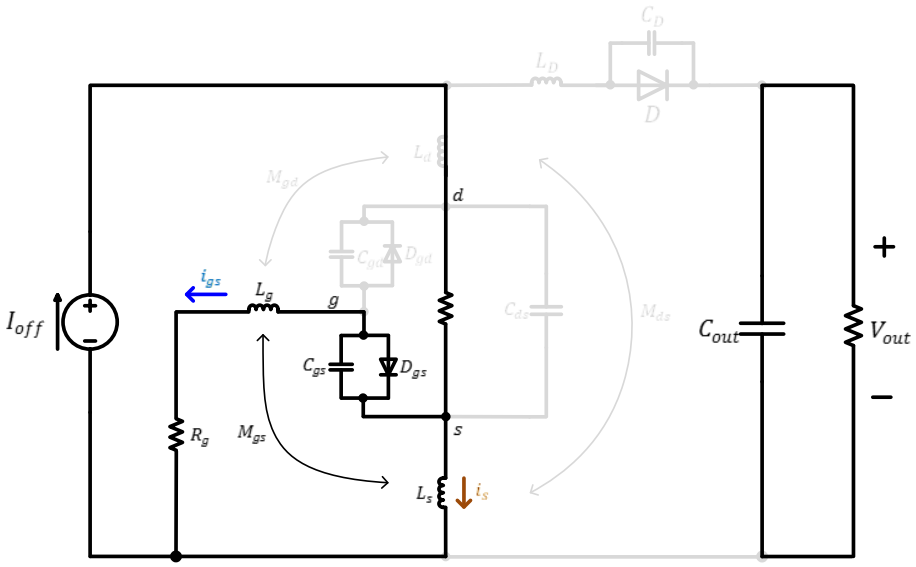


Figure 4.33 Equivalent circuit in turn-off delay stage (V.1)

Substage V.2 Gate source voltage without influence of gate–source diode

After the gate–source diode stops conducting, v_{gs} drops from V_{gsD} to turn-off plateau voltage V_{gs-vr}. The time this stage takes is denoted as t_{offd2}.

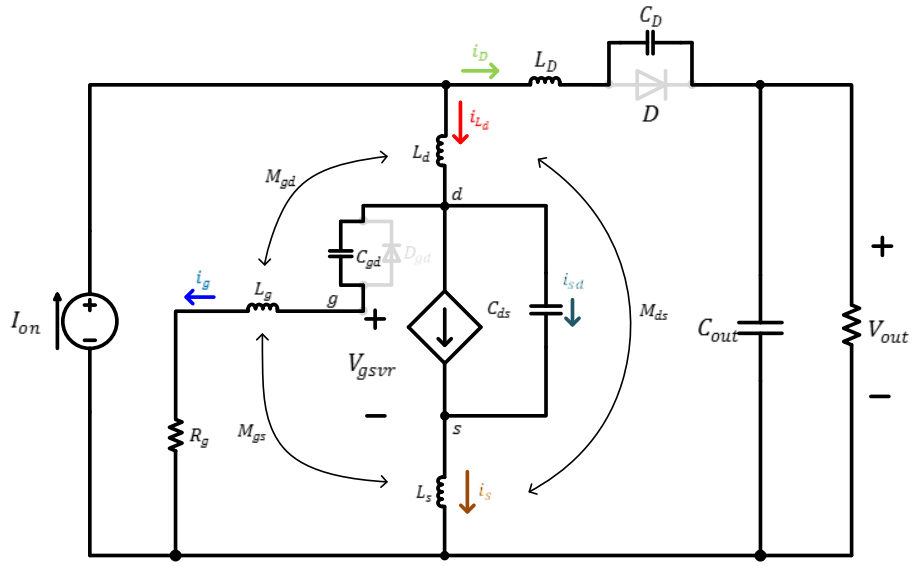


Figure 4.34 Equivalent circuit in turn-off delay stage (V.2)

It should be noted that, in the cases where D_{gs} was not conducting when *stage V* starts, turn-off delay begins with *substage V.2* with v_{gs} drops from V_g (instead of V_{gsD}) to turn-off plateau voltage V_{gs-vr}, and t_{offd2} represents the corresponding time required. As channel current and drain source voltage of a GaN transistor remains the same as on-state values, this stage can be regarded as an extension of transistor on-state.

Stage VI Voltage rise

Theoretically, after the delay stage, transistor will not enter into saturation region until $v_{ds} > v_{gs} - V_{th}$. Given the fact that GaN transistors have large g_{fs}, the transition time from ohmic region to saturation region is neglected [4-21]. During voltage rise, the load current I_{off} splits into four parts: $i_{C_{gd}}$ that charges C_{gd}, which equals the gate current; $i_{C_{ds}}$ that charges C_{ds}, i_{C_D} that charges C_D and i_{ch} that flows through transistor channel. It is assumed that v_{gs} stays constant at V_{gs-vr} in this stage:

$$I_{off} = I_{ch} + I_{C_{dg}} + I_{C_{ds}} + I_{C_D} \tag{4.10}$$

$$I_{C_{dg}} = C_{gd(R_{ds-on}I_{on})} \frac{dv_{dg}(t)}{dt} = \frac{V_{gs-vr}}{R_{goff}} \tag{4.11}$$

$$V_{gs-vr} = \begin{cases} \frac{I_{ch}}{g_{fs}} + V_{gs-th}, & I_{ch} > 0 \\ \frac{I_{off} C_{dg} R_{goff}}{C_{oss}}, & I_{ch} \leq 0 \end{cases} \tag{4.12}$$

V_{gs-vr} is determined in this thesis by applying values of C_{gd} and C_{ds} when drain source voltage is $R_{ds-on}I_{on}$.

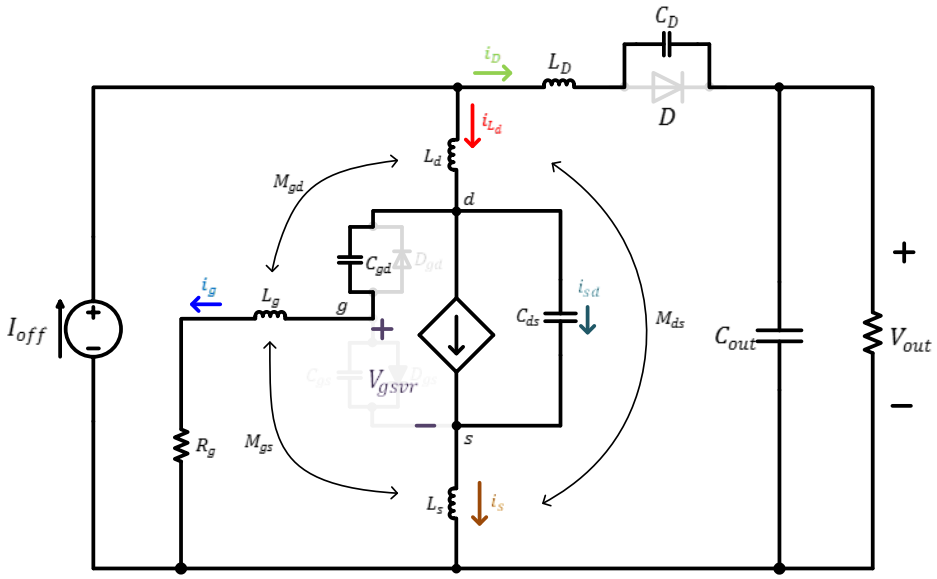


Figure 4.35 Equivalent circuit in stage of voltage rise (VI)

As discussed in *Stage III*, values of parasitic capacitors in GaN transistors show dissimilar characteristics in different ranges of v_{ds}. For the purpose of simplifying mathematical calculations, this stage is separated into *n* substages as well (mirroring the corresponding substages in *Stage III*) and initial conditions of one substage is the final status of previous

substage. Assuming that throughout all the substages, gate-source voltage stays constant as V_{gs-vr}, variations of voltage and current in the *k-th* substage are expressed as:

$$v_{ds-vr(k)}(t) = \frac{V_{gs-vr}}{R_{goff}C_{gd(k)}}t \tag{4.13}$$

$$I_{ch-vr(k)} = \begin{cases} I_{off} - \frac{V_{gs-vr}}{R_{goff}}\left(1 + \frac{C_{ds(k)} + C_{D(k)}}{C_{gd(k)}}\right), & I_{off} > \frac{V_{gs-vr}}{R_{goff}}\left(1 + \frac{C_{ds(k)} + C_{D(k)}}{C_{gd(k)}}\right) \\ 0, & I_{off} \leq \frac{V_{gs-vr}}{R_{goff}}\left(1 + \frac{C_{ds(k)} + C_{D(k)}}{C_{gd(k)}}\right) \end{cases} \tag{4.14}$$

Where $C_{gd(k)}$, $C_{ds(k)}$ and $C_{D(k)}$denote the equivalent value of C_{gd},$C_{ds}$and C_D in the *k-th* substage, respectively. The time needed in the substage is represented by $t_{vr(k)}$.

At the end of this stage, voltage of the freewheeling diode is charged up to forward build-in voltage (from -V_{out}) and loss generated in GaN transistor during this stage is modeled as:

$$P_{vr} = \sum_{k=1}^{n} f_{sw} \int_0^{t_{vr(k)}} v_{ds-vr(k)} i_{ch-vr(k)}(t)dt \tag{4.15}$$

Stage VII Drain current fall

As soon as diode starts conducting, inductor current I_{off} commutes from transistor to diode. If there is still current in transistor channel, substage VII.I starts and when this substage finishes, VII.II is initiated; otherwise substage VII.II begins directly.

Substage VII.I Channel current fall

It is assumed in this thesis that channel current falls first, and parasitic capacitor charging current are the same as in the *substage VI.n* ($I_{C_{ds}}$). And thus, drain-source voltage v_{ds-if1} increases linearly and expression of channel current i_{ch-if} can be found by applying basic circuit law in commutation loop as:

$$i_{ch-if}(t) = I_{ch-vr(n)} - \frac{I_{C_{ds}}}{2C_{ds(V_{out}t)}(L_D + L_d + L_s)}t^2 \tag{4.16}$$

This substage ends when channel current decreases to zero, and loss occurred in GaN transistor can be calculated as:

$$P_{if} = f_{sw} \int_0^{t_{if-ch}} v_{ds-if}(t) i_{ch-if}(t)dt \tag{4.17}$$

Where t_{if-ch} is the channel current fall time.

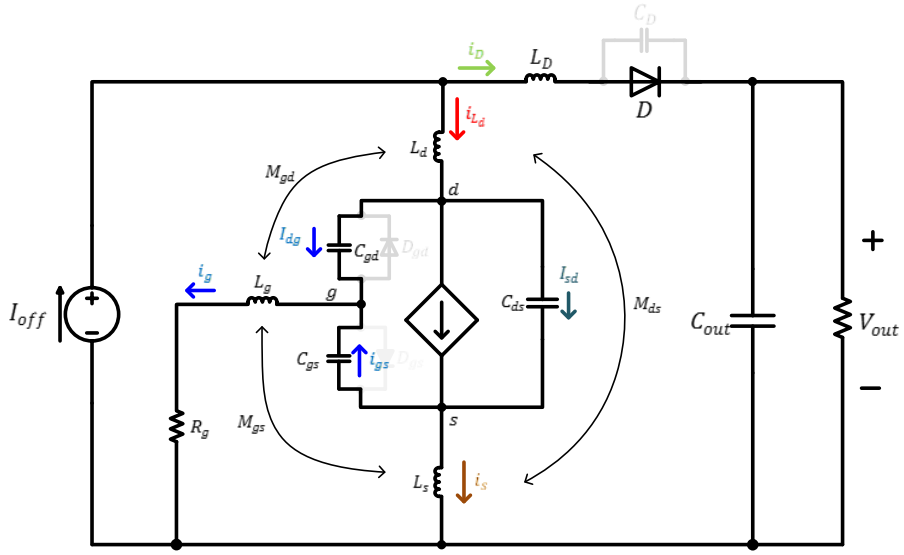


Figure 4.36 Equivalent circuit in substage of channel current fall (VII.1)

Substage VII.II Drain current fall

During this substage, drain current falls resonantly down to zero. Output capacitance of the transistor oscillates with parasitic inductances in the commutation loop, and voltage on the transistor resonates to its maximum value when drain current is zero. No power loss is generated in GaN transistor in this substage.

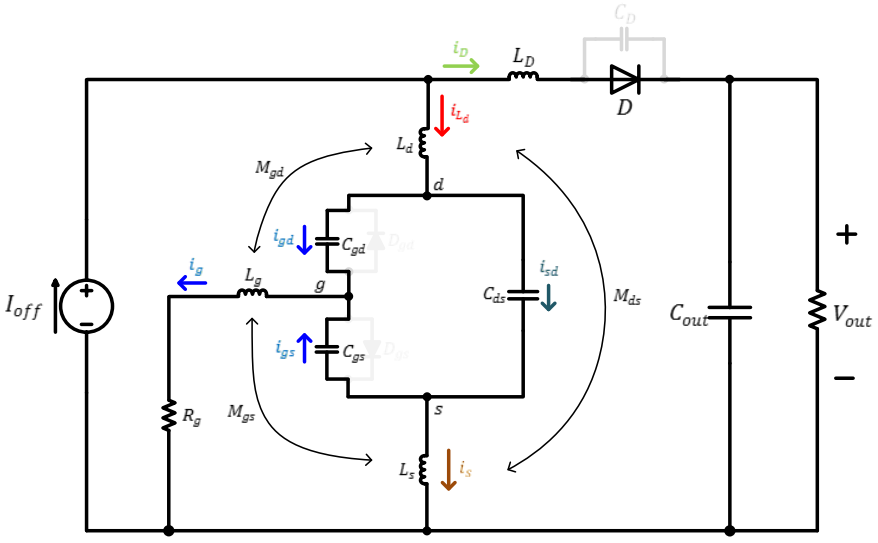


Figure 4.37 Equivalent circuit in substage of drain current fall (VII.2)

C. Conduction loss

Apart from the switching loss, there is also conduction loss, which is generated when GaN transistor is fully on including on and turn-off delay stages.

$$P_{cond} = I_{rms-on}^2 R_{ds-on} \tag{4.18}$$

In case of conducting in reverse direction, reverse conduction loss can be estimated as

$$P_{cond-rev} = f_{sw} \int_0^{t_{rev}} v_{ds-rev}(t) i_{Ld-rev}(t) dt \tag{4.19}$$

Where v_{ds-rev} and i_{Ld-rev} are voltage on and current though the transistor, respectively, when it is conducting in reverse direction. And t_{rev} is the duration of reverse conduction process.

4.3.2 Validation of the developed loss model in a boost converter

The developed model needs to be validated to find out whether it is capable of effectively predicting losses in GaN transistors so that it can be further be used for loss analysis. Loss model validation can be performed by comparing modelled loss values (calculated) with measured (actual) values and, if modelled loss values can approximate measured ones with satisfactory accuracy, the model is considered as valid. Losses can be calculated by applying electric parameters and specifications of the setups, in which the transistors are tested, to the developed loss model. Electric parameters of the components can be obtained from device datasheets, measurements, etc. while parameters of the circuit carrier can be extracted by tools such as Finite Element (FE) and Partial Element Equivalent Circuit (PEEC) simulation software. Loss measurement methods in power electronics systems, in general, can be categorized into two types: electrical and calorimetric (thermal). So far, two different kinds of electric loss measurement techniques have been used to quantify losses in GaN transistors: in [4-25], loss in a GaN HEMT was measured through waveforms of voltage across the device and current flowing through it in a DPT and in [4-44], loss values of a GaN HEMT was obtained by the measurements on efficiency and power of a buck converter and subtracting losses in the rest components in the converter. The former approach is very sensitive to phase discrepancy between the measured current and voltage, especially at high frequencies. The causes of phase discrepancy, such as poor frequency response characteristics of current/voltage sensing devices, mismatch between probes, delays in oscilloscope channels, are inevitable in the measurements [4-45]. Besides, as indicated in the model, measured current and voltage are not necessarily the actual values in the transistor. And therefore, accuracy of the approach is not always pleasing. The latter approach, on the other hand, requires precise estimation of loss in the rest parts of the converter e.g. diode, inductor, etc. Moreover, in a well-designed GaN converter, where efficiency is high, subtraction of two nearly equal numbers would introduce considerable error [overview loss measurement in PE]. As a result, accurateness of the results from this approach may not always be sufficient. Calorimetric methods can be used to determine power because power loss in a device dissipates as heat and heat results in a temperature rise of the device. In power electronics, calorimetric method has already been used to measure power loss of electric and magnetic components

using either simple or complex setups, but have not been applied for quantify loss in GaN transistors [4-45] [4-46]. Results from calorimetric measurements are trustworthy once the relationship between loss and associated temperature in a device are well calibrated and the effects of the environment on temperature of the device are properly accounted for.

In this thesis, the developed loss model is validated in a 200V normally-off GaN HEMT and a 600V GaN GIT, separately, in two boost converter setups. Losses in GaN transistors are measured thermally. In a boost converter setup, losses in boost inductor, freewheeling diode and gate driver could influence the temperate of the transistor. The effects of boost inductor and freewheeling diode on transistor temperature may be excluded by proper layout i.e. placing the two parts physically away from the transistor, although values of connection parasitic inductance will be increased. On the other hand, effect of driver on transistor temperature can be omitted if loss in the driver is negligible small. As a result, transistor temperature increase is caused only by losses in the device. A lookup table that calibrates relationship between loss and temperature increase in GaN transistors can be made by injecting different values of DC current into the devices when it is kept in on-state i.e. generating known power loss and observing corresponding temperature increase. Variation of on-state resistance with temperature should be accounted for to improve accuracy of the lookup table. With the help of the lookup table, values of losses in GaN transistors when they are tested in converter setups can be obtained. In calculations of transistor losses, transistor electric properties such as gate threshold voltage, transconductance, etc. and values of parasitic elements e.g. parasitic capacitances, resistance are obtained from datasheets of the products, while parasitic inductances of device packages and circuit interconnections are extracted using calculation tool of PEEC [4-47]. Detailed information on validation of the loss model can be found in Appendix B. Results from the validation are shown in Figure 4.38 and Figure 4.39. It should be noted that the measured loss value in GaN HEMT at 150W was extrapolated as the lookup table (in Figure A.2) for GaN HEMT is limited to a maximum temperature increase of 25.5^{o}C while at 150W the GaN HEMT has a temperature increase of ~ 50^{o}C. Loss in GaN HEMT at 150W was quantified using the same thermal resistance as in the maximum temperature point in the lookup table.

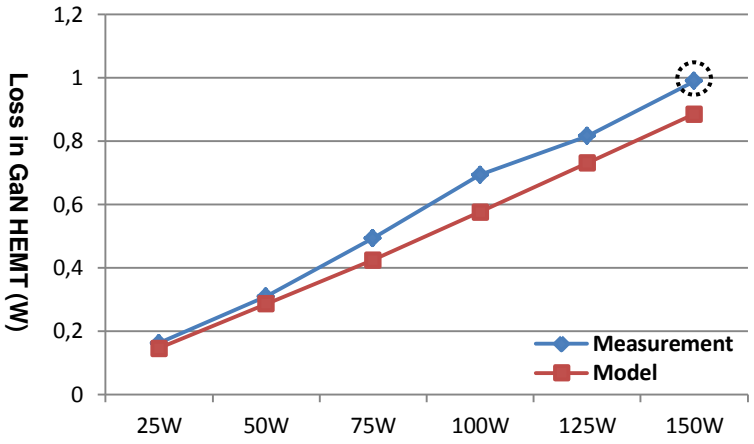


Figure 4.38 Modeled and measured loss in a normally-off GaN HEMT in CCM

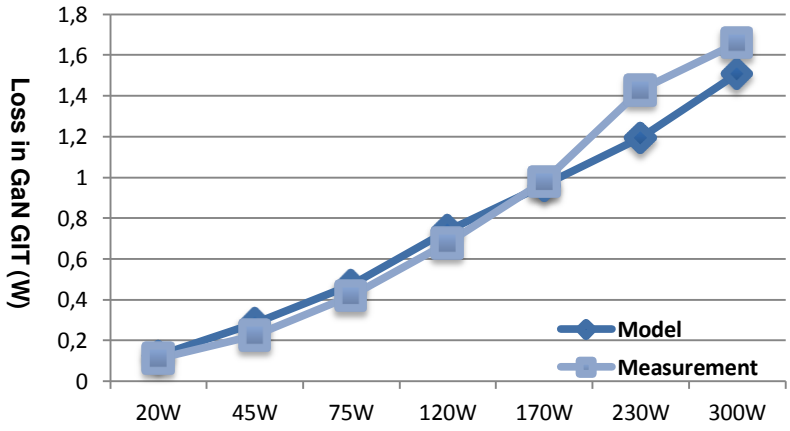


Figure 4.39 Modeled and measured loss in GaN GIT in CCM

The developed model predicts losses in GaN HEMT and GaN GIT with satisfactory accuracy, whilst modelled loss values deviate from measured values in different patterns with the two kinds of transistors. With GaN HEMT, the modeled loss values deviate more from the measured results as power increases (and at the same time, output voltage, as shown in Table A.1 in Appendix B). Throughout all the testing points (specified in Table A.1), ratio of C_{ds}/C_{gd} is so large that, with zero gate driving voltage i.e. gate current is determined only by plateau voltage and gate loop resistance, no channel current exists during turn-off. (In fact, no channel current will present in the 200V GaN HEMT until the current reaches 32A with driving voltage as zero during turn-off). In turn-on loss, as is analyzed in 5.3, discharging loss of output capacitance (combination of C_{ds} and C_{gd}, with value of C_{ds} more than 20 times that of C_{gd}) dominates. And therefore, accuracy of the model depends, to large extent, on how good the nonlinear output capacitance (in particular, C_{ds}) is modeled. In low voltage ranges, averaged values of capacitance (which is used to model nonlinearity of the capacitors) can estimate losses in GaN HEMT well while, when voltage ranges become wider, the two-point-averaged value of the capacitance show more deviations from the real values and so does the modeled loss. With GaN GIT, the modelled loss in test points up to

120W (output voltage up to 250V and turn-off current up to 1.1A, as shown in Table A.3 in Appendix B) are smaller than the measured values while in test points with higher power (and output voltage), the trend is reversed. As discussed in Appendix B, values of C_{gd}, C_{ds} and the ratio of C_{ds}/C_{gd} in GIT are almost constant when V_{ds} is greater than 255 V and below 255 V, both capacitances values vary with V_{ds} , with C_{ds}/C_{gd} varies dramatically. In this thesis, capacitances are modeled using average values in two separate regions (above and below 255V). This approach could result in relatively better approximation of loss below 255V because: a). under low turn-off current conditions, hardly any current would flow in transistor channel as the ratios of C_{ds}/C_{gd} in both regions are sufficiently large (~7 in in low voltage range and up to 70 in high voltage range) with driving voltage as zero, and therefore turn-off loss is negligible; b). as is explained in 5.3, discharging loss of output capacitance dominates in turn-on loss of GIT and reasonable accuracy can be obtained when values of the capacitances, especially C_{ds}, are well modelled. Given the fact that two discrete capacitance values are used in the two voltage regions, a sudden decrease in capacitance value will lead to underestimation of loss. Besides, as capacitance values of GaN HEMT are about 3 times larger than that of GaN GIT and variation of capacitance are more dramatic in GaN HEMT than GIT, when the same capacitance modeling approach (averaged values) are used, smaller turn-on loss estimation error would be induced in modeling of GaN GIT.

During turn-off, on the other hand, ratio of C_{ds}/C_{gd} and gate current play significant roles in generating turn-off loss, especially when gate current is small, as indicated in (4.14). In GaN GIT, the ratio of C_{ds}/C_{gd} is as low as. When turn-off current is high, however, there will be channel current in region of 0~255V V_{ds}, and the value of channel current depends on the ratio of C_{ds}/C_{gd}, which varies greatly, and value of gate current. With a gate current determined by transistor plateau voltage (zero driving voltage during turn-off) and gate resistance R_g, the usage of averaged capacitance values in the developed model underestimates turn-off loss in GIT at high currents. Better approach on modeling C_{ds}/C_{gd} during low voltage can improve accuracy of the modeling of turn-off loss and also total switching loss of GaN GIT.

4.3.3 Discussion

Apart from satisfactory accuracy in predicting losses in GaN transistors, the developed loss model also has benefits in aspects of:

- Device and circuit parasitics are well accounted for. Loss modeling of normally-off GaN HEMT has also been carried out in [4-4] and [4-48], both analytically. In [4-48], loss modeling of GaN HEMT in high current, low voltage switching conditions (in application of POL) was presented. The model did not include effects of device output capacitance, which is crucial for loss in higher voltage, low current applications of GaN HEMT as demonstrated in [4-4], although nonlinearity of the capacitance was characterized. The

proposed modeling approach of GaN HEMT in [4-4], on the other hand, did not take circuit and package parasitic inductances into consideration, and therefore may not be capable of providing sufficient guidelines on design and optimization of a GaN HEMT based system. The developed loss model in this thesis have taken almost all circuit and package parasitic elements into account and therefore has the capacity of uncovering critical parasitics in either the device or the circuit it operates in. In particular, for GaN GIT, of which loss modeling has not been performed so far, presence of gate-channel diode and effects of magnetic coupling between package leads are enclosed in the model so that more insights into the transistor can be obtained to reveal optimal application conditions.

- Calculation of transistor loss and identification of influences of different factors on transistor loss are made simple. Simplifications and assumptions made in the process of loss modeling may be one of the causes of the deviations between the modelled and measured results, but they lead to reduced complexity and therefore calculations are made easy. Moreover, with less complex expressions of voltage and current in stages and substages, factors that affect loss can be identified easily.
- The model can also be applied to GaN device in other topologies. As discussed in chapter 1, electromagnetic environment has profound influence on characteristics and losses of GaN transistors, especially the normally-off GaN HEMT, and therefore, characterization on switching behaviors and loss modeling of GaN transistors in one circuit may only be valid in the specific topology. Although developed in a boost converter, the analytical loss model in this thesis is, as indicated in the modelling process, valid in any diode-clamped, inductive load switching circuits. And therefore, the model can be applied in circuits such as Buck, Buck-Boost, etc.

The developed loss model, on the other hand, also has limitations that originate from issues such as assumptions made, loss-affecting parameters neglected, inaccurate modeling of electric parameters, etc.

- As can be seen in switching stages and substages, in particular in voltage fall of turn-on and voltage rise of turn-off, proper modeling of output capacitance and miller capacitance of a transistor is of great importance as the miller capacitance influences, to great extent, voltage slewing rate of the devices and the ratio between the two capacitances affects the values of channel currents, especially during turn-off. Averaged values are used in this thesis to approximate nonlinearity of transistor capacitances, which results in reasonable accuracy of the modelled loss values. More accurate modeling of the non-linear capacitances of GaN devices, especially in low voltage ranges, are needed to achieve better modeling results.

- Modeling approach of on-state resistance can only be applied to certain applications. In this thesis, characteristic of temperature-dependent on-state resistance is dealt with by using averaged values. This approach would lead to underestimated loss when the actual temperature of the device is high and overestimated loss when device temperature is low. Besides, the values are taken from device datasheets, which are tested under specific conditions, and whether the values can be directly used in the testing points of GaN devices needs to be checked. The modeling approach is adopted in this thesis because on-state resistances of the devices are low (even with high temperatures) and they are to be used in low current conditions i.e. on-state loss is low. In applications where on-state loss is comparable to switching loss or even dominating in total loss, better modeling method of on-state resistance is needed.
- In spite of the fact that effect of charging current of diode parasitic capacitance on transistor turn-on loss is taken care of by considering the amount of charge required and neglecting voltage drop caused by the time-varying charging current, more insight into the charging process are demanded in case of high parasitic inductance in the commutation loop as the charging-current induced voltage across the inductance may not be negligibly small given fast switching (high dv/dt) nature of GaN devices. Voltage drop on parasitic inductances would affect instant values of drain-source voltage and loss during voltage fall in turn-on.
- As was made clear that capacitance of the boost inductor is not included in the model and in the validation, multiple single layer inductors are connected in series to minimize the parasitic capacitance. In applications where parasitic capacitance of the inductor is not negligible compared with the values of the transistor, it should be included. This capacitance needs displacement currents to be charged during transistor turn-on and discharged during turn-off. And accordingly, the currents will affect switching loss of the transistor, as is observed in [4-49], and need to be accounted for. The capacitance, together with some parasitic inductance, is in parallel with output capacitance of the transistor. The same approach of modeling diode capacitance, discussed above, can be used to model the effect of capacitance of the inductor.
- The including of parasitic capacitance of the freewheeling diode by using the value of total charge required to block output voltage approximate the influence of the capacitance in a relatively simple way. As discussed in 4.3.1.1, SiC diode is used in both loss modeling and validation to exclude reverse recovery effect. SiC diodes, however, has nonlinear capacitance that needs to be charged during transistor turn-on and discharged during transistor turn-off. The capacitance in a SiC diode usually show nonlinear properties which could result in a capacitance several times higher when voltage across

the diode is low than that when voltage is high and absolute capacitance values may even be comparable to that of a GaN transistor in low voltage range. For instance, in a 600V, 4A SiC diodes from Cree (C3D02060E), capacitance showed nonlinear characteristic (higher value) when voltage across the diode is low (0~150V) and nearly linear property (lower value) when voltage is high (150V~600V), maximum capacitance is more than 4 times the low value. Besides, the maximum capacitance is as high as ~45 pF, which is comparable to output capacitance of a 600V GaN GIT (70pF). During transistor turn-on, diode is charged up from low voltage to high voltage: when voltage across diode is low (larger capacitance, required charge Q_1), voltage on transistor is high and when diode voltage is high (lower capacitance, required charge Q_2), voltage on transistor is low. In other words, Q_1 will flow through transistor channel when V_{ds} is high while Q_2 flows through transistor channel when V_{ds} is low. The approach taken in this thesis has decent accuracy in condition that Q_1 and Q_2 are comparable, or even close, to each other. When Q_1 and Q_2 are not comparable to each other, better modeling method is needed.

- Exclusion of electric characteristics such as nonlinearity of transconductance of the transistor, parasitic resistance of the PCB, etc. would also contribute to inaccuracy of the loss model, the contributions are hardly noticeable though. Take the nonlinear transconductance as an example: similar to that of Si MOSFET, transconductance of a GaN transistor is non-linear, especially when gate-source voltage is low. The assumption that transconductance is constant over an entire switching transient holds in condition that the transistors are tested (and to be used later) in current levels where the transconductance can be treated as constant. With normally-off GaN HEMT, transconductance is almost constant when current is in range of 0.5A~6A and with GaN GIT, transconductance is nearly constant from 0.5A up to 40A. And therefore, constant values are used for loss modeling and calculation. In case of operating GaN transistors in current ranges where transconductance show obvious nonlinearity, the assumption may not tenable. Modeling of a nonlinear transconductance can be accurately done through approach of curve fitting or roughly approximated by dividing the transconductance curve into different sections, within which the value can be regarded as constant, and using the equivalent value in each section.
- The developed loss model also has limitations in measure of frequency range in which it is effective. In developing circuit model of GaN transistors in 4.2 and equivalent circuit of the GaN based boost converter in 4.3, effectiveness of modeling of devices and interconnections are all subjected to frequencies. For instance, as already mentioned in 4.2.2, depending on operation frequency, the output capacitor can be modelled in different ways. Circuit model in Figure 4.24 was adopted provided that switching

transients of GaN transistors are longer than the time period of the capacitor's first self-resonant frequency. Similarly, in modeling of the parasitic capacitances of a GaN transistor, lumped capacitors are used, which may not be accurate at frequencies where parasitic inductances of current paths in the structures (where parasitic capacitance originate from) start to influence performance of the transistor. In this thesis, where GaN transistors are to be used in MHz range, the modeling approaches adopted are considered sufficient.

4.4 Qualitative analysis of losses in GaN transistors

Given the fact that the developed model worked well in estimating losses in GaN transistors, qualitative analysis on influences of the parameters included in the model can be performed by examining the mechanisms in different stages/substages of the model. The influences of device parasitic elements, circuit parasitic elements and properties of other components in the circuit are summarized as follows:

- *In a GaN transistor,* loss is greatly affect by parasitic capacitances C_{gs}, C_{gd} and C_{ds}. During turn-on, larger C_{gs} would require longer charging time during turn-on (when the same driving scheme is used) and, as voltage across C_{gs} controls maximum current that can flow through transistor channel, channel current rising durations is prolonged. Besides, a smaller slew rate of channel current would cause less voltage drop on parasitic inductances in the commutation loop i.e. voltage on transistor will not be reduced much. And thus, turn-on loss is increased. Meanwhile, both C_{gd} and C_{ds} will get discharged through transistor channel, and the larger their values are, the more discharging loss will be generated. During turn-off transistor channel current is determined by the ratio of C_{ds}/C_{gd} (with the same gate current) in stage of voltage rise and current fall and channel current, as well as turn-off loss, could be zero with sufficiently C_{ds}/C_{gd} large ratio regardless of the length of switching duration and variation of drain-source voltage. When there's channel current during turn-off, loss is affected by the values of C_{gd} (determines voltage rise time when gate current is fixed), the ratio of C_{ds}/C_{gd} (determines amount of channel current when gate current is fixed) and loop inductance (affects variation of drain-source voltage). Furthermore, larger C_{gs} will lead to longer turn-off delay time, which will hardly have any influence on conduction loss in a closed loop converter (as the longer delay time will be compensated by the control) but will cause higher conduction loss in the transistor in an open loop converter.
- *In a GaN transistor,* parasitic inductances influence transistor loss in different extent. Source inductance (part of L_s) would reduce value of V_{gs} with the flowing of an increasing current during turn-on and increase V_{gs} with the flowing of an decreasing current during turn-off, and thus the inductance slows down both switching transients and increases switching loss. Gate

inductance (part of L_g) and common source inductance also hinder the variation of gate current from charging discharging C_{gs} during turn-on and therefore extend the duration and enlarge turn-on loss. Turn-off delay period, which is part of the transistor on-time, will also be prolonged. Drain inductance (part of L_d) reduces transistor drain-source voltage during current rise in turn-on and causes overvoltage (together with transistor source inductance) during channel current fall in turn-off, and therefore decreases turn-on loss but will increase turn-off loss. Besides, magnetic coupling effects between different terminals of a GaN transistor increases or reduces effective values of L_g, L_s and L_d and therefore also have their influences on transistor loss.

- *Circuit parasitic inductances* of interconnections connecting drain, source and gate of a GaN transistor has the same effect on transistor loss. Lumped parasitic inductance in commutation loop, L_{out}, has the same effect on switching loss as that of L_d.
- *Gate driver* in a GaN based boost converter provides sourcing and sinking currents during switching transients to GaN transistors and therefore has direct influence on transistor loss. Larger sourcing current in turn-on and sinking current in turn-off would result in small switching loss. In fact, as indicated by (4.14), the product of gate current and ratio between output capacitance and gate-drain capacitance determines channel current, and thus switching loss, during turn-off.
- *Parasitic capacitance of the diode* as already discussed in 4.2.2, requires displacement currents to get charged in order to block output voltage and discharged before conducting, would increase of transistor channel current during transistor turn-on and decrease channel current during turn-off and therefore affects turn-on and turn-off loss accordingly.

It should be noted that, modeling of reverse conduction characteristics of GaN transistors have not been verified since the devices are tested only in CCM in this chapter. In next chapter, GaN transistors are tested in other operation modes where reverse conductions are activated, modeling of conduction loss in reverse direction will be validated.

4.5 Summary

In this chapter, loss modeling of GaN transistors is developed. Circuit models of normally-off GaN HEMT and GIT are firstly proposed through the approach of using a combination of existing discrete electric components to reflect physical structure of the die (which results in operation mechanisms and electrical characteristics of the device) and package technology adopted for the device (which contributes to parasitic elements). A general equivalent circuit model that is suitable for both transistors is then obtained. Furthermore, an equivalent circuit of a GaN transistor based boost converter, which is to be used in PFC, is presented, in which circuit

models of components in the boost converter such as boost inductor, freewheeling diode and output capacitors and parasitic elements arise from circuit carriers e.g. PCB traces, pads, vias, etc. are included. With the equivalent circuit, voltage and current expressions in switching transients and conduction period of the transistor are derived to model losses in the transistors. The developed loss model was validated in a normally-off GaN HEMT and a GaN GIT in two CCM boost converters, respectively. And, since the model predicts losses in GaN transistors with satisfactory accuracy, losses in GaN transistors are qualitatively analyzed.

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Chapter 5. High frequency operation of GaN devices in boost converters in BCM-VS

5.1 Introduction

In this thesis, exploration of possible potentials of GaN devices focuses on high frequency operation capabilities of GaN transistors. And accordingly, identification on suitable topologies and operation modes for application of GaN transistors are loss-minimization oriented so that operation frequency of GaN based converters can be pushed up. As discussed in 1.2, optimal usage of GaN devices may not be achieved if they are simply used in existing power converters that are mostly designed to suit Si devices. To fully exploit potentials and benefits of GaN technology, optimal utilization of GaN transistors in high frequency applications should be investigated.

Since it was confirmed in chapter 3 that boost converter, which is the most widely used PFC topology with Si devices, will remain as a preferred choice for implementing PFC with the advent of GaN technology, losses in GaN transistors are firstly analysed using a boost converter as a platform. Through loss analysis, suitable operation conditions of GaN transistors for high frequency applications i.e. desirable switching conditions are to be revealed, with the knowledge of which, approaches to facilitate GaN devices with the such switching conditions will be investigated. Challenges and design trade-offs when applying GaN transistors in the approaches are then dealt with to achieve optimal usage of the transistors at high operation frequency. Moreover, frequency boundaries of the approaches are explored to guide design and implementation.

5.2 Loss analysis of GaN transistors in boost converters

In theory, GaN devices would have greatly improved FOM than Si counterparts and thus have the potentials of boosting performances of existing power electronics systems and enabling new applications. In reality, however, capabilities of GaN transistors in terms of switching speed, maximum operation temperature, etc. are limited by issues such as die design and fabrication approach, device packaging technology, the way they are used in circuits, etc. And therefore, it is necessary to investigate application conditions of GaN transistors where potentials of the transistors can be exploited. The investigation should uncover switching and conduction conditions that can best accommodate parasitic elements in GaN transistors and circuits (inductance, capacitance and resistance) so that losses in the transistors can be minimized. In this thesis, the investigation focuses on two different kind of single-die, normally-off GaN transistors, namely GaN HEMT and GaN GIT, which were well introduced in chapter 4.

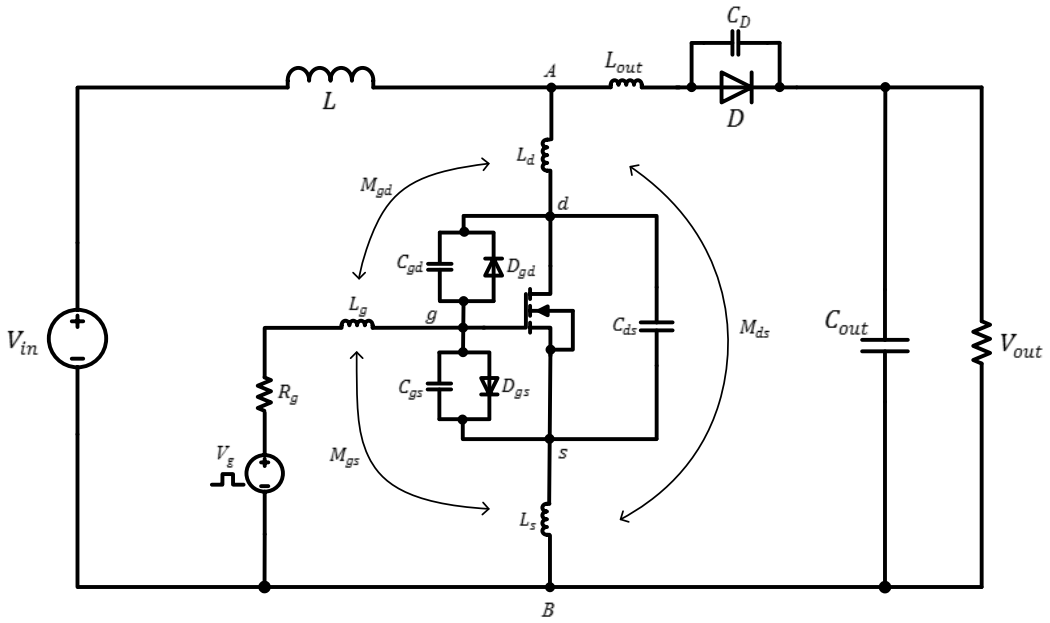


Figure 5.1 Equivalent circuit of a GaN based boost converter

5.2.1 Loss characteristics of GaN transistors in boost converters in CCM

Effects of parasitic elements on loss in transistors are subjected to switching (e.g. hard switching or soft switching) and conduction conditions (e.g. conduction in forward or reverse direction) of the transistors. To start with, losses in GaN transistors are analysed in boost converters in CCM employing the developed loss model in chapter 4. In CCM, the transistors are hard-switched in both turn-on and turn-off processes. Besides, transistors will conduct in forward direction when they are in on-state while conduction in reverse direction will not occur.

5.2.1.1 Loss distribution of GaN transistors in CCM

Losses in GaN HEMT and GaN GIT is assessed firstly at 100 kHz in CCM in two boost converters, respectively. The frequency chosen is based on practical concerns so that loss in the transistors are high enough to be measurable and the devices would not be overheated when no extra thermal management actions e.g. implementation of heatsinks, enforcement of fan, etc. were taken.

Losses breakdown of the normally-off GaN HEMT is performed with parameters of the transistor and circuit summarized in Table A.1 and specifications of the test points listed in Table 5-1. As can be seen from Figure 5.2, in the test points: turn-on loss dominates in GaN HEMT, turn-off losses are zero and conduction losses are low. The discharging of the large output capacitance of the transistor causes high turn-on losses and the low conduction losses are due to the transistor's low on-state resistance. With zero gate driving voltage, where gate current is determined only by plateau voltage and gate loop resistance, thanks to the large C_{ds}/C_{gd} ratio (up to 24), no channel

current exist in transistor throughout all the test points. In fact, according to (4.14), with the freewheeling diode in the boost converter chosen as the one specified in Table A.1 and driving voltage as zero during turn-off, channel current will not present in GaN HEMT until turn-off current reaches ~32A.

Table 5-1. Specifications of test points in GaN HEMT based boost converter

P_{out}(W)	v_{out}(V)	I_{on}(A)	I_{off}(A)
25	61.5	1.06	1.40
50	87.0	1.52	1.96
75	106.0	1.88	2.36
100	122.5	2.16	2.72
125	137.0	2.4	3.12
150	150.0	2.64	3.36

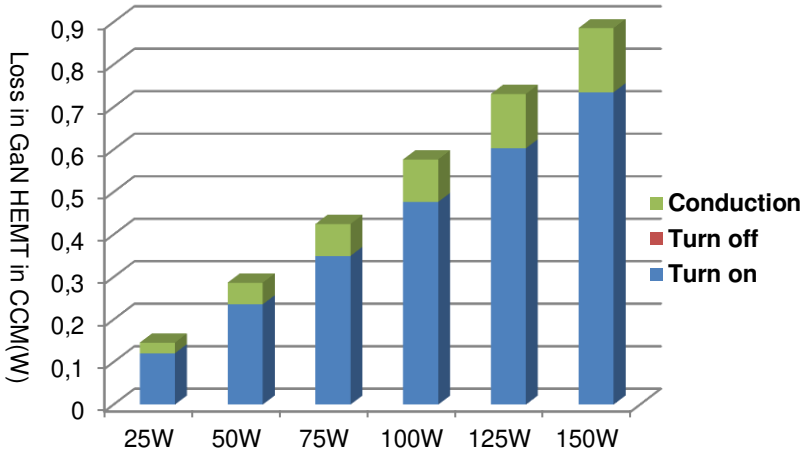


Figure 5.2 Loss breakdown of a normally-off GaN HEMT in CCM

Loss distribution of the GaN GIT, as illustrated in Figure 5.3, is also investigated employing the developed loss model in previous chapter. Turn-on loss, resulting from the discharging of the large output capacitance of the transistor and the long discharging time duration because of the large miller capacitance in low voltage range, dominates. As was already mentioned in 4.3.2, the ratio of C_{ds}/C_{gd} in GIT is large (up to 70) in high voltage range (>255V), and small (down to 4.9) in low voltage ranges (<255V). And according to (4.14), when driving voltage is zero, channel current will present when turn-off current is beyond 2.2A. In the test points, where maximum turn-off current is 1.65A, turn-off currents, and accordingly turn-off losses, are zero. Conduction losses, thanks to the low on-state resistance, are small.

Table 5-2. Specifications of test points in GaN GIT based boost converter

P_{out}(W)	v_{out}(V)	I_{on}(A)	I_{off}(A)
20	100	0.35	0.44
45	150	0.51	0.65
75	200	0.70	0.88
120	250	0.87	1.09
170	300	1.04	1.31
230	350	1.20	1.52
300	400	1.35	1.65

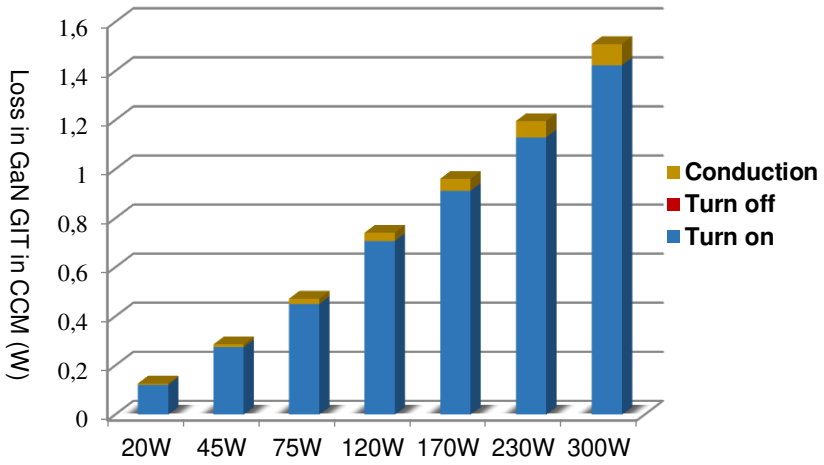


Figure 5.3 Loss breakdown of high voltage GaN GIT in CCM

To summarize, with both GaN HEMT and GaN GIT:

- Turn-on loss dominates in both transistors in CCM due to the large output capacitance that will get discharged though transistor channel;
- Turn-off loss will not be present in the transistors when turn-off current is low because of the high C_{ds}/C_{gd} ratio that eliminates channel current; when turn-off current is high enough, turn-off loss will be generated;
- Conduction loss, resulting from low on-state resistance of the transistors, is low

5.2.1.2 Effects of parasitic inductance on loss in GaN transistors in CCM

The loss distributions of both GaN HEMT and GaN GIT exhibits the influences of parasitic capacitance and resistance in a clearer way than that of the parasitic inductance from both package and circuit as, for the latter, only the net effect of different parasitic inductances (as shown in Figure 5.1) is included. A thorough study of the effects of parasitic inductances, from the

viewpoint of loss, is needed to gain more insights e.g. is all parasitic inductances bad or there are ones that helps, which parts are more critical, etc. to guide design of package and layout.

Influences of circuit and package inductances on switching loss of GaN HEMT is demonstrated at the test point of 150W (output voltage is 150V and on/off currents are 2.64A/3.36A) and as illustrated in Figure 5.4, L_s has the largest influence on turn-on loss in CCM as it behaves as a negative feedback between gate loop and switching loop and thus slows down switching transients. L_{out} and L_d reduce turn-on loss by lowering the value of V_{ds} during turn-on transient. The presence of L_g increases turn-on loss in that it prolongs rise time of channel current. As no current flows in transistor channel during turn off with such a low switching current (far below 32A), parasitic inductances has no effect on turn off loss. It worth be pointed out that, the LGA packaged GaN HEMT used in this thesis has very low parasitic inductances (gate 0.07nH, drain 0.07nH and source 0.08nH) and the results in Figure 5.3 works more as a reflection on effects of circuit parasitic inductances as they are quite large (gate 1.48nH, drain 3.37nH and source 2.66nH) compared with the package counterparts.

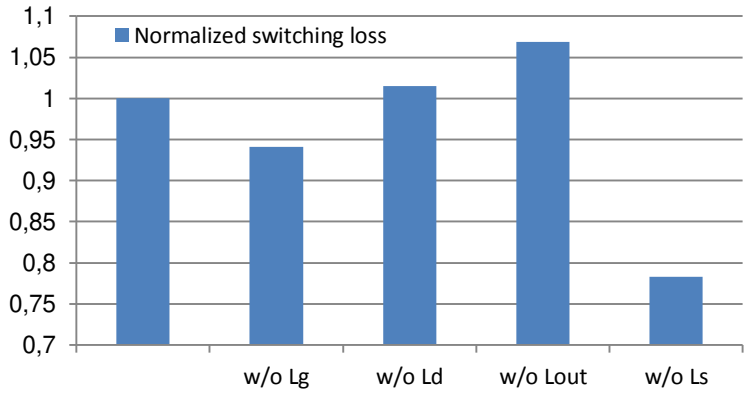


Figure 5.4 Effects of parasitic inductance on turn-on loss in GaN HEMT (150W)

Effects of circuit and package parasitic inductances on switching losses of GaN GIT are assessed at 300W and the results are shown in Figure 5.5. As switching current is low (less than 2.2A), no channel current will be present i.e. turn-off loss is not influenced by parasitic inductances in the 300W test point. Similar to the influences of parasitic inductances on losses in GaN HEMT: L_s has the largest influence on switching loss in CCM; L_g increases turn-on loss as it slows down the speed of channel current increase; L_{out} and L_d lower turn-on loss by means of reducing the value of voltage across the transistor in turn-on transient. Unlike GaN HEMT, leaded packaged GaN GIT also introduces magnetic coupling effects between leads, which affects effective parasitic inductances differently during turn-on and turn-off as current directions differ. Given current directions in GIT leads during turn-on, effective inductances in common source is reduced by coupling effect in gate-source (M_{gs}) and drain-source (M_{ds}), and therefore helps to reduce turn-on loss. Mutual inductance between gate and source also reduces effective gate inductance and

decreases turn-on loss thereof. Magnetic coupling effect between gate and drain (M_{gd}) will increase effective inductance in both L_g and L_d. In other words, existence of M_{gd} would cause drain-source voltage to drop while prohibit the increase of channel current, and the net effect of M_{gd} is almost zero. As is clearly shown in Figure 5.5, apart from the common source inductance, the rest parasitic inductances have limited effect on switching loss of GaN GIT, especially the mutual inductances. The influence of circuit parasitic inductances (PCB inductances in the designed setup) on turn-on loss in GIT were also explored and, as indicated by Figure 5.5, the contribution is limited (less than 5%).

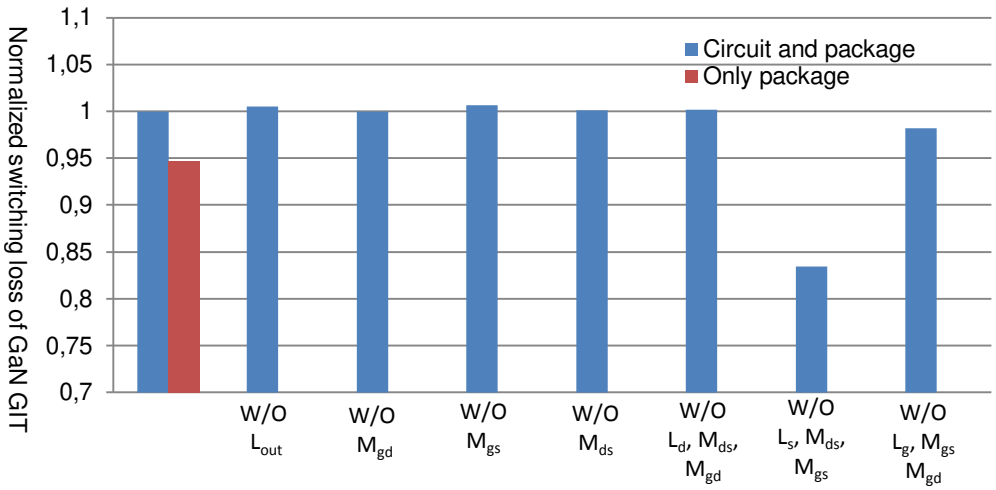


Fig.5.5 Effects of parasitic inductance on switching loss in GaN GIT (300W)

To conclude, with GaN HEMT and GaN GIT: parasitic inductances have no effect on turn-off loss when switching currents are low, whereas they have different effects on turn-on loss in CCM, with the effective (net effect of both self- and mutual-inductance) common source inductance the most critical one. Effective drain side inductance and partial inductance of the commutation loop (L_{out}) is beneficial for loss reduction at turn-on while the effective gate inductance increases switching loss.

5.2.2 Desirable switching conditions of GaN transistors for high frequency applications

Results from loss analysis of both normally-off GaN HEMT and GaN GIT in CCM in boost converters indicate that, in both transistors, switching loss overwhelms conduction loss when used in low-current, high-voltage conditions in hundreds of kHz and proper switching conditions are required to reduce switching loss so that application of the transistors with further increased frequency can be achieved to maximum possible gain brought about by the new technology. The two different kinds of GaN transistors showed similar characteristics of switching loss in CCM: turn-on loss, resulting mainly from discharging of the large output capacitances dominates; circuit

and package parasitic inductances, especially the common source inductance, affect turn-on loss but not turn-off loss when turn-off current is so low that channel current during turn-off transient will not be present. Apart from the shared properties, difference also exists between switching loss characteristics of the two types of transistors: GaN HEMT, because of its large C_{ds}/C_{gd} ratio, will not have channel current i.e. turn-off loss until switching current is very high (e.g. with a 200V GaN HEMT, up to 70A), and therefore GaN HEMT is considered to be exempt from turn-off loss; GaN GIT, due to the large C_{gd} (influences voltage-rise duration) and small C_{ds}/C_{gd} ratio (affects amount of channel current), turn-off loss will be present even at low switching current level (e.g. above in a 600V GaN GIT), and thus, turn-off loss reduction may also needed for GaN GIT. In spite of the difference regarding turn-off loss of the two specific GaN devices, switching conditions for proper usage of transistors can be generalized as: turn-on with low voltage to alleviate the effects of output capacitance and low current to mitigate the effects of parasitic inductances; turn-off with low channel current.

Consequentially, proper switching conditions of GaN transistors can be summarized in Figure 5.6, simultaneous satisfactions of which would result in minimized switching loss in the transistors in high frequency applications. In other words, advantage of GaN technology for high frequency applications can be taken of when low voltage, low current turn-on and low channel current turn-off (in case of GaN GIT) are fulfilled at the same time. And therefore, it is necessary to investigate applications that could facilitate such conditions simultaneously.

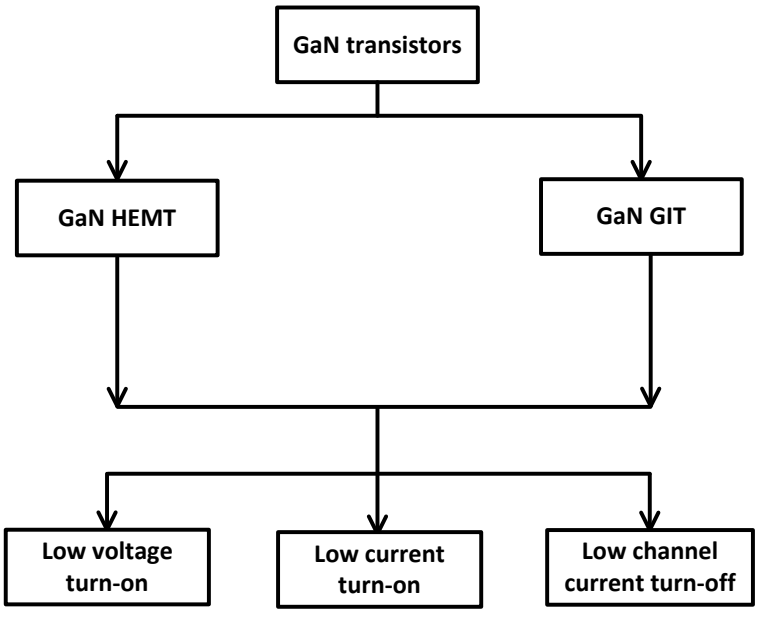


Figure 5.6 Desirable switching conditions of GaN transistors for high frequency operation

5.3 Application of GaN transistors in high frequency boost converters in BCM-VS

In a power converter, switching and conduction environment of transistor(s) is mainly determined by the operation mode of the converter, although adoption of auxiliary circuitry i.e. passive and active snubbers could change typical switching condition of a transistor in one operation mode. Several different operation modes were developed in power converters and, as was discussed in 3.3.1, each of the PFC topologies can work in these operation modes. Given the fact that boost converter, among other existing topologies, will remain as a preferred choice for actualizing PFC, for the goal of maximizing benefits out of GaN technology in high frequency PFC application, operation modes in a boost converter is to be examined to find out whether one of the existing modes can provide proper operation conditions for GaN transistors or none of the modes is suitable and investigations on approaches e.g. snubbers for changing switching conditions that could lead to the demanded conditions is needed.

5.3.1 Operation modes in a boost converter

Traditionally, a boost converter, according to inductor current shape, has two operating modes – Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM), which are well described in most handbooks [5-1][5-2]. When operated in CCM, inductor current is continuous and never drops to zero and, ideally, inductor current is discontinuous in DCM as it drops down to zero during transistor off-time and, after an idle period during which voltage across the transistor is subject to the input, a new switching cycle starts. To improve efficiency, a boost converter is also operated in so called Boundary Conduction Mode (BCM, boundary between CCM and DCM), in which a new switching period is initiated when the inductor current returns to zero.

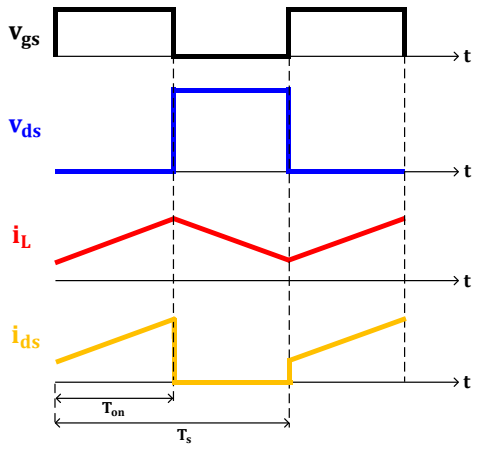


Figure 5.7 Representative waveforms of CCM

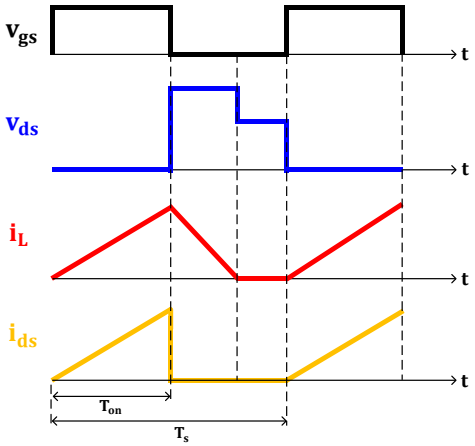


Figure 5.8 Representative waveforms of DCM (theoretical)

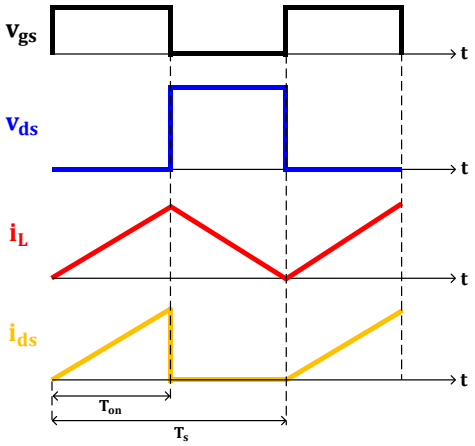


Figure 5.9 Representative waveforms of BCM

In addition, if the transistor is not switched on immediately after the demagnetization of boost inductor in BCM, resonance between parasitic capacitance of transistor and boost inductor will occur. Voltage across the transistor starts to drop resonantly, transferring the energy stored in the output capacitance of the transistor to the inductor. This mode of operation is called BCM with valley switching (BCM-VS) and is commonly used in PFC boost converters [5-3]-[5-5]. As a matter of fact, two different situations exist in BCM-VS in boost converter, depending on the ratio between the converter's input voltage and output voltage, as shown in Figure 5.10 and Figure 5.11. When $V_{out} \leq 2V_{in}$, voltage across the transistor falls resonantly and the minimum value is reached after half of a resonant period, at which point transistor current returns zero. When $V_{out} > 2V_{in}$, voltage on the transistor will drop below zero and the transistor will conduct in reverse direction through the device channel. Drain current will then increase linearly back to zero, at which point a new switching cycle starts.

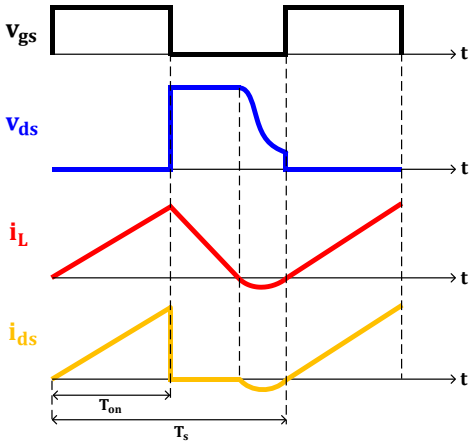


Figure 5.10 Representative waveforms of BCM-VS when $V_{out} \leq 2V_{in}$

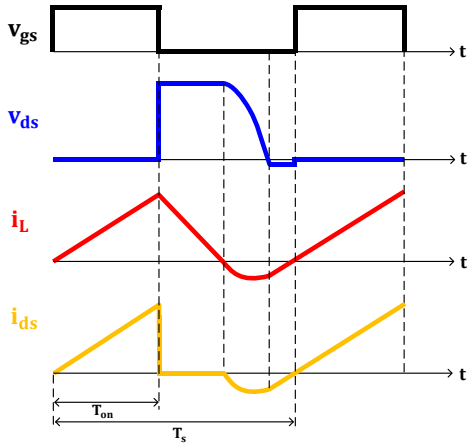


Figure 5.11 Representative waveforms of BCM-VS when $V_{out} > 2V_{in}$

Accordingly, different switching and conduction conditions of transistors are facilitated in different operation modes of a boost converter:

- Turn-on. In CCM, transistor is turned on with a voltage of V_{out} and certain inductor current and, in BCM, ZCS turn-on is enabled with the same switching voltage. ZCS is maintained in both situations of BCM-VS, switching voltage, however, differs: when $V_{out} \leq 2V_{in}$, transistor turn-on process happens at the first valley point of the oscillating voltage with a value of $(2V_{in}-V_{out})$, which is lower than V_{out}; when $V_{out} > 2V_{in}$, transistor will be switched on with the voltage across it being the voltage drop in reverse conduction (V_{Rev}), which is determined by both gate-source voltage and gate-drain voltage and is usually in range of few volts.
- Turn-off. With the same input current, transistor is subjected to different turn-off current levels when operation mode changes: in CCM, where inductor current ripple is the smallest, lowest peak current will present; in BCM, peak current is high as 2 times the

input current; in BCM-VS, highest turn-off current (higher than $2I_{in}$) will be induced to compensate the negative current brought about by the mode.

- Conduction. RMS currents of transistors that directly links to conduction loss is also influenced by operation mode of a boost converter when the input and output conditions are fixed, although the influence may not be so critical. For instance, with the same input current and voltage conversion ratio, RMS current in BCM is 1.15 times that of the counterpart in CCM with a ripple of 20% of the input. In BCM-VS, RMS current is higher than that of BCM with the same input current and frequency because of the existence of the ringing time and, as will be discussed in 5.6, the difference got enlarged with increase of frequency. Conduction of transistor in reverse direction (from source to drain) happens only when $V_{out} > 2V_{in}$ in BCM-VS.

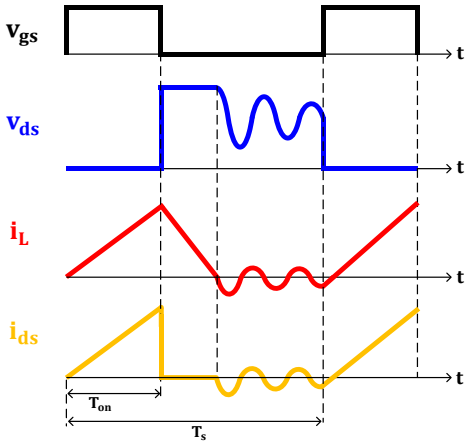
Table 5-3 Transistor switching and conduction conditions in different operation modes

		Turn-on		Turn-off	Conduction	
		Voltage	Current	Current	RMS current	Reverse conduction
CCM		High	Low	Low	Low	No
BCM		High	Zero	Higher	Higher	No
BCM-VS	when $V_{out} \leq 2V_{in}$	Low*	Zero	Highest	Highest	No
	when $V_{out} > 2V_{in}$	Zero				Yes

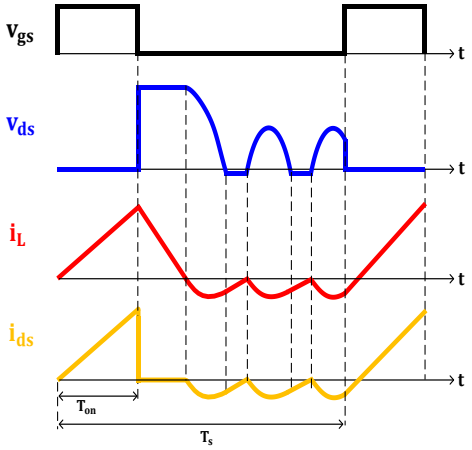
* In the special case of $V_{out}= 2V_{in}$, turn-on voltage is zero

It should be noted that, in DCM, due to the same oscillation as in BCM-VS, voltage across the transistor and inductor current varies in a damped sinusoidal manner instead of maintaining at V_{in} and zero, respectively, as illustrated in Figure 5.12. Depending on the need of a specific application, turn-on of transistors in DCM may or may not occur at one of the valley point of voltage where current is zero in case of $V_{out} \leq 2V_{in}$ whereas, when $V_{out} > 2V_{in}$, both ZCS and ZVS can be achieved. On one hand, BCM-VS can be regarded as one special case of DCM where turn-on is initiated the first time the inductor current returns to zero after the diode stops conducting, which is also the first valley point of the switching voltage when $V_{out} > 2V_{in}$. On the other hand, DCM can also be viewed as exceptional cases of BCM-VS where duration of switching cycle is prolonged and switching voltage and current are shifted. Compared to BCM-VS, with the same input and output parameters, ringing time in DCM is prolonged, during which time energy circulates in the circuit and does not contribute to power transfer, leading to high current peak and less efficient power delivery. In particular, in PFC application, DCM only occurs in very low/light load as a supplementary mode of BCM-VS where switching frequency would be very high to lower the effective operation frequency [5-5]. And thus, in this thesis, DCM is considered

as one special case of BCMV-VS and switching and conduction conditions of transistors in DCM is not discussed separately.



(a)



(b)

Figure 5.12 Representative waveforms of DCM (practical)

(a). when $V_{out} \leq 2V_{in}$; (b). when $V_{out} > 2V_{in}$

To sum up, when GaN transistors are used in a boost converter, different switching and conduction conditions are enabled by operating the converter in different modes: in CCM, the turn-on process is hard switching; in BCM, zero current (ZCS) turn-on can be achieved, the effect of turn-on current on turn-on loss is eliminated; in BCM-VS, zero current turn-on can be maintained while the voltage across the switch is at a low level (or even zero).

The switching conditions enabled by both situations of BCM-VS, therefore, makes the mode ideal for high frequency usage of GaN HEMT not only because discharging of the large output capacitance at high voltage is exempted but also due to the fact that parasitic inductance has no effect on turn-on loss in the transistor. The mode of BCM-VS is also suitable for high frequency

application of GaN GIT when turn-off current is low as, similar to that with GaN HEMT, turn-on loss can be greatly reduced with low-voltage and ZCS turn-on and turn-off loss would not be generated. When current at turn-off is high, however, turn-off loss in GaN GIT may become dominating with the increase of switching frequency and attention needs to be paid to investigate approaches suitable for channel current reduction or even elimination.

5.3.2 Application of GaN transistors in BCM-VS

To prove and demonstrate the analysis that BCM-VS provides ideal switching conditions for GaN HEMT and, when peak current low, GaN GIT and that, turn-off loss reduction in GaN GIT is needed for high frequency application of the transistor when turn-off current is high, the two types of transistors are operated in both situations of BCM-VS at increased frequency. For the purpose of illustrating the potential of low switching loss in GaN transistors at high frequency brought by BCM-VS, assessments of losses in GaN transistors in CCM and BCM are also added as comparing groups.

GaN HEMT in BCM-VS mode is exemplified by operating the 200V GaN HEMT based boost converter used for loss model validation in Appendix A.1 (with corresponding parameters of the setup listed in Table A.2) in different working modes at 1MHz with an output voltage of 100V and a maximum power of 150W. Both calculation and measurement results of losses in GaN HEMT in BCM-VS are shown and the measured loss corresponds well with the calculation results, as shown in Table 5-4. Limited by thermal management of the transistor, experimental measurements of losses in GaN HEMT in CCM and BCM at high frequency were not performed and only calculated results are presented. Loss breakdown of GaN HEMT in different modes, employing the developed loss model, indicate that switching losses in GaN HEMT can be greatly reduced in both situations of BCM-VS even at high frequencies as illustrated in Figure 5.13. The operation mode of BCM-VS in a boost converter indeed provides ideal switching conditions for high frequency application of GaN HEMT.

It should be pointed out that the high voltage stress are caused by the needed large commutation loop to keep other components away from the transistor in the setup so that temperature rise of the device during the testing are caused only by the loss in the device itself and thus loss quantification can be done through thermal measurement. Detailed explanation on the loss quantification mechanism are given in Appendix A.

Table 5-4 Specifications for assessing losses in GaN HEMT at high frequency

Mode	V_{in}(V)	V_{on}(V)	I_{on}(A)	I_{off}(A)	Calculated loss(W)	Measured loss(W)
CCM	30	100	2.25	2.75	4.04	/
BCM	30	100	0	5	3.10	/
BCM-VS I ($V_{out} < 2V_{in}$)	60	20	0	5	0.22	0.20
BCM-VS II ($V_{out} > 2V_{in}$)	30	2.2	0	5.4	0.15	0.12

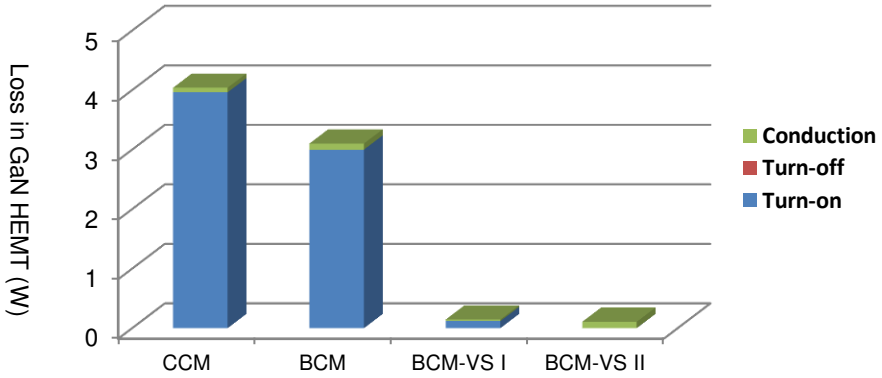


Figure 5.13 Loss breakdown of GaN HEMT in different modes at high frequency

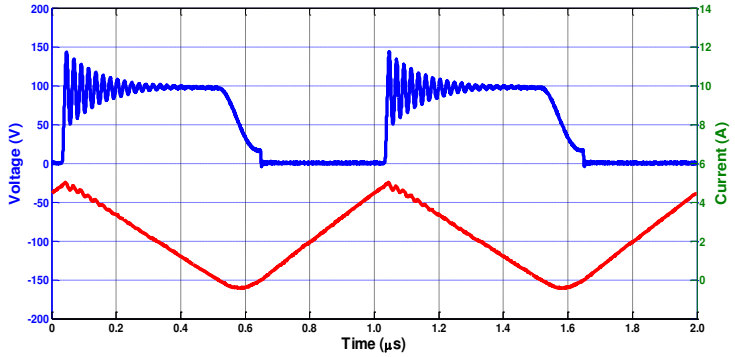


Figure 5.14 Measured waveforms of boost converter with GaN HEMT in BCM-VS ($V_{out} \leq 2V_{in}$)

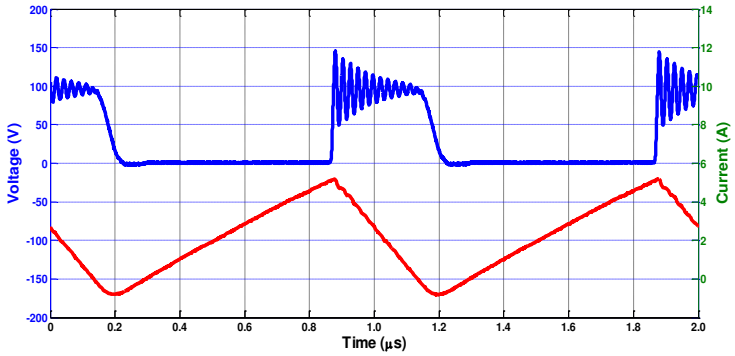


Figure 5.15 Measured waveforms of boost converter with GaN HEMT in BCM-VS ($V_{out} > 2V_{in}$)

GaN GIT in BCM-VS is demonstrated by running in the 600V GaN GIT based boost converter setup described in Appendix A.2 in different operation modes at 1MHz with an output voltage of 400V and a maximum power of 300W. Electrical specifications of the test point and corresponding loss are shown in Table 5-5. As indicated by the loss breakdown of GaN GIT in BCM-VS in Figure 5.16, turn-on loss in both transistors are greatly reduced while turn-off loss starts to become dominating with increase of turn-off current. And therefore, with low switching current, BCM-VS is ideal for GaN GIT whereas with high switching current, BCM-VS is beneficial in reducing turn-on loss whereas turn-off loss reduction is needed for high frequency application of the transistor.

Table 5-5. Specifications for testing GaN GIT in different operation modes

Mode	V_{in}(V)	V_{on}(V)	I_{on}(A)	I_{off}(A)	Calculated loss(W)	Measured loss(W)
CCM	200	400	1.35	1.65	12.35	11.9
BCM	200	400	0	3	10.98	11.0
BCM-VS (V_{ou}=2V_{in})	200	0	0	3	2.92	3.0
BCM-VS I (V_{out} < 2V_{in})	260	120	0	3.2	4.66	4.5
BCM-VS II (V_{out} > 2V_{in})	120	1.3	0	6.6	10.87	9.8

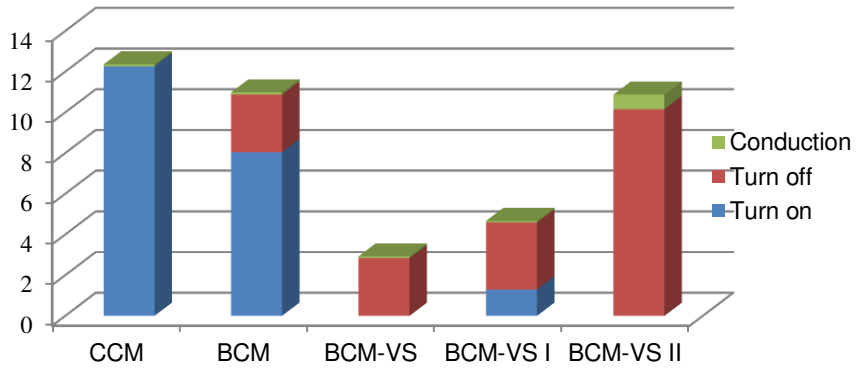


Figure 5.16 Loss breakdown of GaN GIT in different operation modes at high frequency

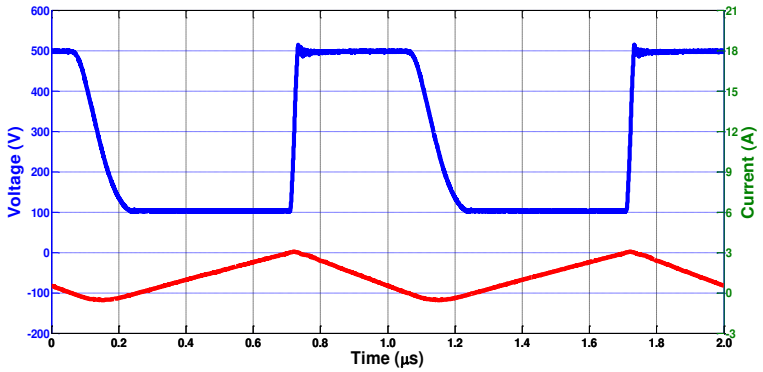


Figure 5.17 Measured waveforms of boost converter with GaN GIT in BCM-VS (V_{out}= 2V_{in})

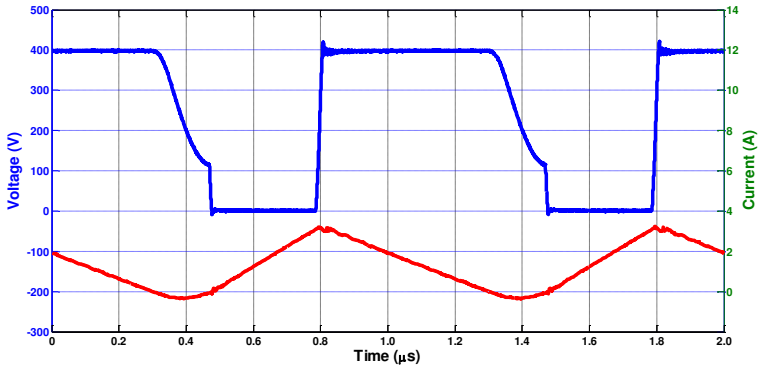


Figure 5.18 Measured waveforms of boost converter with GaN GIT in BCM-VS ($V_{out} \leq 2V_{in}$)

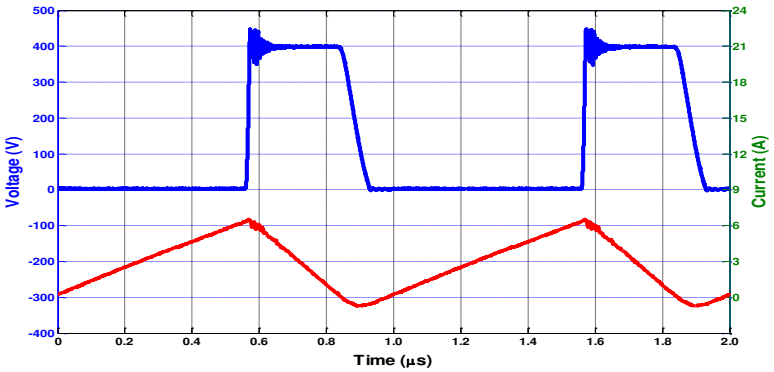


Figure 5.19 Measured waveforms of boost converter with GaN GIT in BCM-VS ($V_{out} > 2V_{in}$)

The applications of GaN transistors in BCM-VS have proved that this operation mode naturally provides ideal switching conditions for GaN HEMT and GaN GIT (with low turn-off current) for high frequency applications. When used in high turn-off current conditions, channel current reduction i.e. turn-off loss reduction is needed for high frequency usage of GaN GIT. Besides, it is worth pointing out that GaN transistors conduct current in reverse direction (from source to drain)

in BCM-VS when output voltage is larger than two times the input voltage and therefore, conduction loss in this mode consists of both forward conduction (current flow from drain to source when transistor is on) loss and reverse conduction loss (when transistor is off). Reverse conduction loss are calculated with equations (4.1) and (4.19). The good match between measured and modelled loss in BCM-VS in condition of $V_{out} > 2V_{in}$ with both GaN HEMT and GaN GIT indicates that the modelling of reverse conduction loss approximates reality with satisfactory accuracy.

5.4 Optimal utilization of GaN transistors in high frequency boost converters in BCM-VS

With the identification that BCM-VS in boost converter, by nature, provides proper switching conditions for high frequency application of GaN HEMT and, when turn-off current is low, GaN GIT as switching losses in the transistors can be greatly reduced, a thorough investigation on limitations as well as design trade-offs when applying GaN transistors in BCM-VS is needed so that optimal utilization of the transistors can be achieved and, consequentially, benefits of the new technology can be fully exploited in high frequency applications.

In this section, attention will be exclusively paid to solve the problems that applying GaN transistors in both situations of BCM-VS brings to achieve, with proper functioning of the transistors, loss minimization. Although, when it comes to turn-off, none of the widely used operation modes would enable soft switching conditions, value of turn-off current do vary when operation mode of the boost converter differs with the same input current and, as explained in 5.3.1, adoption of BCM-VS would introduce highest turn-off current. The high current at turn-off not only possibly lead to high turn-off loss but also causes other problems such as high overvoltage across transistor, more energy dissipation, which need to be taken care of for successful usage of the transistor in practice. Besides, conduction of GaN transistors in reverse direction is triggered in BCM-VS when $V_{out} > 2V_{in}$, the consequence of which needs to be investigated to come up with suitable methods for total loss minimization.

5.4.1 Trade-off between switching loss minimization and overvoltage suppression

During and after turn off, oscillation occurs between parasitic inductance of the commutation loop and parasitic capacitance of a GaN transistor. The oscillation leads to overvoltage on GaN transistors and dissipation of the oscillatory energy in circuit, which may hinder successful usage of the transistors, as illustrated in (5.1) where C_{ext} denotes external capacitance added. For instance, when the 200V GaN HEMT were tested in BCMV-VS at 1MHz with an output voltage of 100V and a peak current of 5.4A, switching loss as low as less than 0.1W while overvoltage is as high as 50V. Switching loss, as explained in 5.3.2, will remain at such a low level with further

increase of peak current up to 32A, however, to keep the transistor from exceeding maximum rated voltage, the peak current has to be limited down to 10.8A in the same setup. Reduction of both transistor overvoltage and circuit oscillatory energy dissipation, as suggested by (5.1), can be accomplished through minimization of circuit parasitic inductances during design or paralleling external capacitors to GaN transistors in a fixed setup.

$$v_{ds} = I_{off}\sqrt{\frac{L_d + L_s + L_{out}}{C_{oss} + C_{ext}}}\sin\left(\frac{t}{\sqrt{(L_d + L_s + L_{out})(C_{oss} + C_{ext})}}\right) + V_{out} \tag{5.1}$$

Higher turn-off current in BCM-VS, in theory, will also cause higher turn-off loss under the same driving conditions. However, given the large C_{ds}/C_{gd} ratio of GaN HEMT that eliminate channel current until turn-off current is beyond 32A, turn-off loss of GaN HEMT can be regarded as immune from the effect of higher turn-off current. With GaN GIT, because of the low C_{ds}/C_{gd} ratio in low voltage range, depending on the absolute value of the higher turn-off current, turn-off loss of GaN GIT may or may not be affected. When GaN GIT based boost converter is operated in high current applications (input current is higher than 1.1A, such that turn-off current in BCM-VS is larger than 2.2A), turn-off loss will be generated and should be reduced to achieve high frequency application of the converter, as indicated by the loss distribution in both situations in BCM-VS in Figure 5.16. Turn-off loss reduction i.e. turn-off channel current reduction, as can be extracted from equations (4.13) and (4.14), can be achieved by enforcing negative V_{gs} during turn-off or paralleling external capacitors to GaN GIT. The former practice requires an additional negative power supply, which is not preferable in real applications while the latter is more cost-effective and easy to implement.

Paralleling external capacitors to GaN transistors, in this thesis, is adopted to combat the issues of high turn-off loss (in GaN GIT), high overvoltage and oscillatory energy dissipation introduced by the high turn-off current of BCM-VS. Addition of external capacitance to GaN transistors in BCM-VS, however, will increase turn-on loss linearly, as capacitive turn-on loss is determined by:

$$P_{on} = \frac{(C_{oss} + C_{ext})V_{on}^2 f_{sw}}{2} \tag{5.2}$$

Where V_{on} denotes the voltage across GaN transistor when it is switched on. In fact, the increase of turn-on loss is more severe in the situation $V_{out} \leq 2V_{in}$, especially when the value of turn-on voltage is high, than when $V_{out} > 2V_{in}$ where transistors will be switched on with voltage drops across the devices when they conduct in reverse direction. Accordingly, trade-offs on the selection of proper external capacitor value exists between increased switching loss and reduced voltage stress:

- With GaN HEMT and, when turn-off current is low, GaN GIT, in which turn-off loss will not present, a trade-off between reduced voltage stress and increased turn-on loss needs to be considered for the selection of the external capacitance needed;
- With GaN GIT in high turn-off current conditions, where both turn-on loss and turn-off loss is generated, paralleling external capacitor to the transistor would increase turn-on loss while reduce turn-off loss and, at the same time, ease voltage stress on GIT. Value of the capacitor should be determined by considering the trade-off between total switching loss minimization and overvoltage reduction.

Example of GaN HEMT

Take the two cases, BCM-VS I and BCM-VS II, using the 200V GaN HEMT at 1MHz with an output voltage of 100V as examples: an overvoltage of about 46V was imposed on GaN HEMT in the example with $V_{out} \leq 2V_{in}$ while the overstress was even as high as 50V in the case when $V_{out} > 2V_{in}$, caused by the switching currents of 5A and 5.4A at turn-off, respectively. Paralleling external capacitors could reduce the voltage stress down to less than 120V when capacitor values are up to 1.5nF in both cases, as illustrated in Figure 5.18. The addition of capacitance to GaN HEMT would cause negligible increase in turn-on loss i.e. total switching loss in the transistor when $V_{out} > 2V_{in}$. In BCM-VS under the condition of $V_{out} \leq 2V_{in}$, on the other hand, increase in overall switching loss is noticeable by the same action, though the absolute value of the loss is still quite low. It should be pointed out, as will be explained in 5.6.1, conduction loss in GaN HEMT increases with the introduction of external capacitors to the transistor in both cases, the increment, however, can be neglected in these two specific examples.

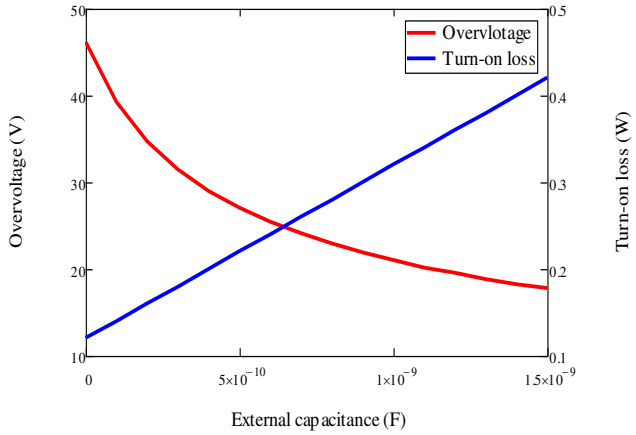


Figure 5.20 Effects of external capacitance on overvoltage and turn-on loss in BCM-VS when $V_{out} \leq 2V_{in}$

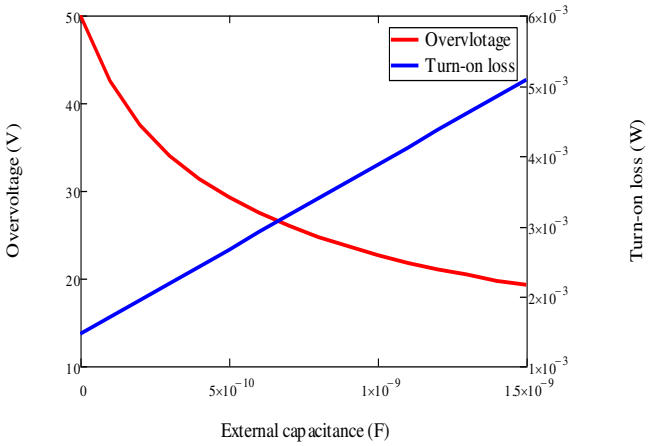


Figure 5.21 Effects of external capacitance on overvoltage and turn-on loss in BCM-VS when Vout > 2Vin

Experiments were carried out to verify the analysis and the results corresponds well with the predictions: in the example with $V_{out} \leq 2V_{in}$, overvoltage drops to about 28 V while switching losses in GaN HEMT is almost doubled (increased from 0.12W to 0.22W) when a capacitor with a value of 470pF is added to the transistor; in the example in which $V_{out} > 2V_{in}$, when three 470pF capacitors are paralleled to GaN HEMT, the overvoltage drops to 20V while switching loss remains unchanged. And therefore, for optimal usage of GaN HEMT in BCMV-VS, the trade-off between reduction of voltage stress and minimization of switching loss should be considered to determine the needed capacitance, especially in the situation when $V_{out} \leq 2V_{in}$.

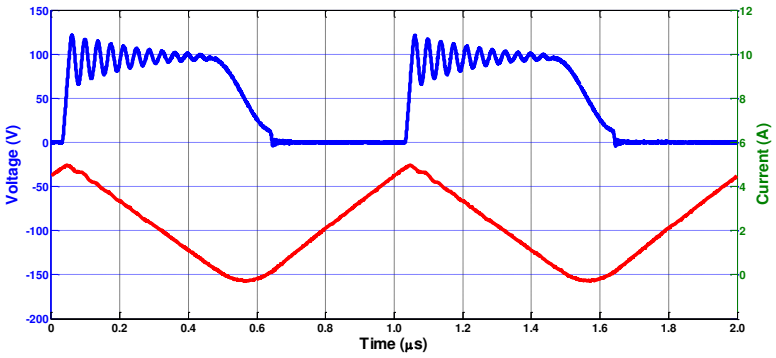


Figure 5.22 GaN HEMT in BCM-VS with external capacitance ($V_{out} \leq 2V_{in}$)

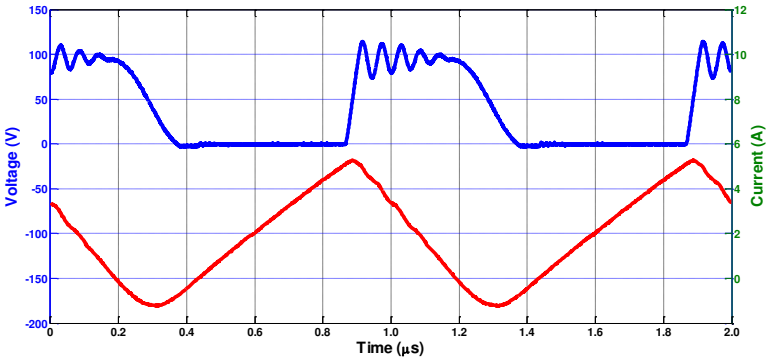


Figure 5.23 GaN HEMT in BCM-VS with external capacitance (V_{out}> $2V_{in}$)

Example of GaN GIT

With the 600V GaN GIT in BCM-VS at 1MHz with an output voltage of 400V: in BCM-VS I and BCM-VS II, values of overvoltage are up to ~27V and 56V, with currents of 3.2A and 6.6A, respectively. The overvoltage, although not so critical, can be eased by paralleling external capacitors to the transistor and, more importantly, when the proper values are added, losses in the transistor can be minimized. Addition of capacitance to GaN GIT would enlarge turn-on loss linearly in BCM-VS I but reduce turn-off loss and, in this specific example, minimal loss occurs when turn-off loss ceases to be present. As shown in Figure 5.24, loss in GaN GIT in BCM-VS I can be minimized to 2.5W when an external capacitor with a value of 125pF is paralleled to drain-source of the transistor. At the same time, overvoltage across GaN GIT is reduced from 27V to 16V. In the case of GaN GIT in BCM-VS II, where turn-on loss hardly present, enlarging the ratio between output capacitance and miller capacitance by adding external capacitors would help to decrease turn-off loss and, as can be expected, loss minimization can be obtained when turn-off no longer exist. In the BCM-VS II example, loss minimization is achieved (down to 0.74W) when additional capacitance of 420pF is added to drain-source and the overvoltage is reduced to 21V. It should be noted that, as will be further elaborated in 5.6.1, RMS currents through GaN will be augmented in both cases due to the addition of the capacitors. The augment, however, is negligibly small in the two examples.

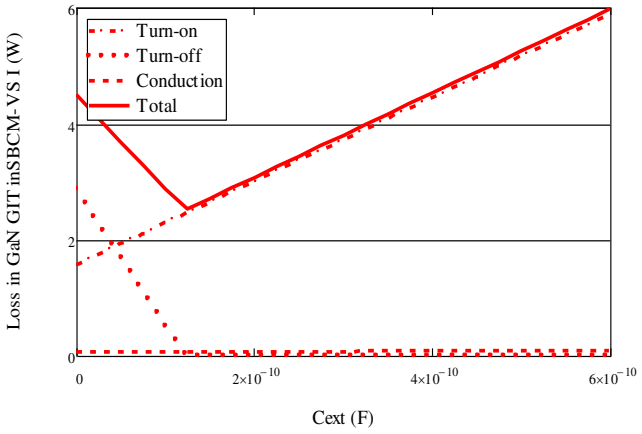


Figure 5.24 Effects of external capacitance on loss in GaN GIT in BCM-VS when $V_{out} \leq 2V_{in}$

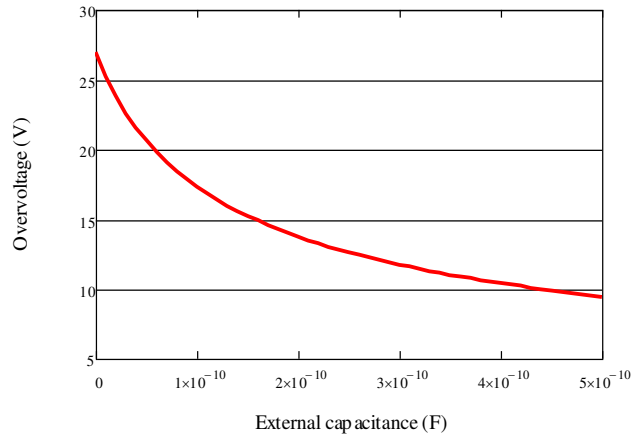


Figure 5.25 Effects of external capacitance on overvoltage across GaN GIT in BCM-VS when $V_{out} \leq 2V_{in}$

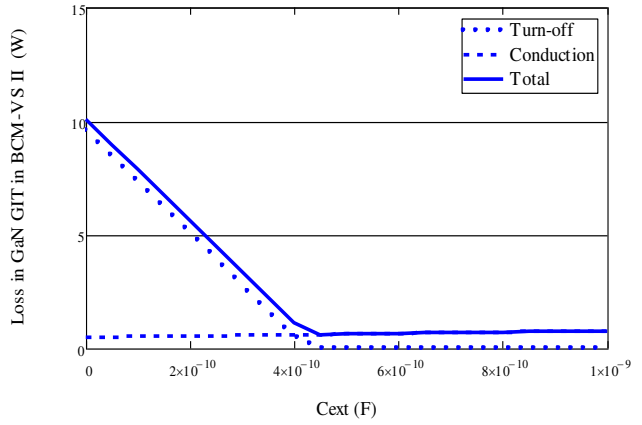


Figure 5.26 Effects of external capacitance on loss in GaN GIT in BCM-VS when $V_{out} > 2V_{in}$

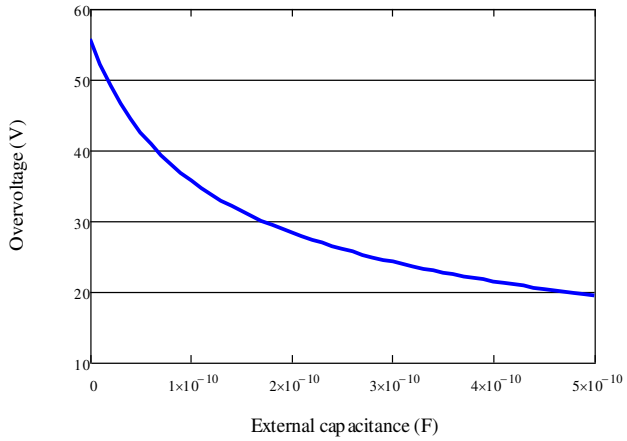


Figure 5.27 Effects of external capacitance on overvoltage across GaN GIT in BCM-VS when Vout>2Vin

Experimental measurements were conducted to prove and demonstrate the analysis. In the example of BCM-VS I, switching loss was quantified as ~2.4 W and overvoltage is measured as 15V when a capacitor with the value of 150pF was paralleled to GaN GIT, the results of which corresponds well with the prediction. On the other hand, when a capacitance of 470pF was added to GaN GIT in BCM-VS II, loss was measured as 0.7W and overvoltage dropped from ~56V to 20V, which also agrees with the analysis.

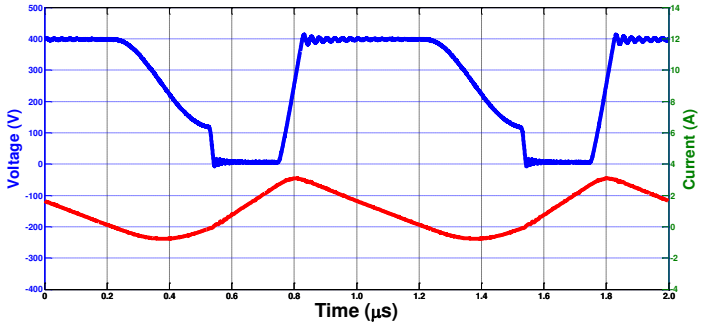


Figure 5.28 GaN GIT in BCM-VS with external capacitance ($V_{out} \leq 2V_{in}$)

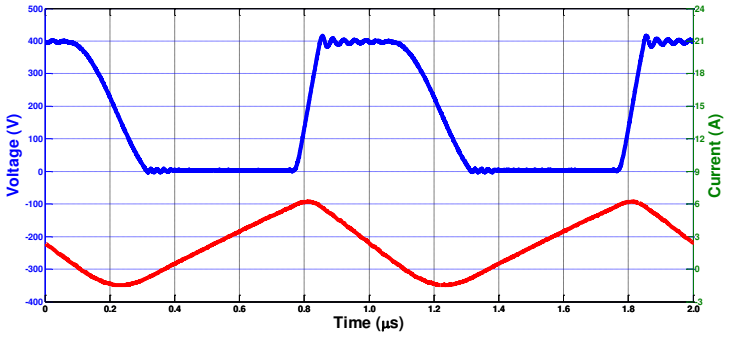


Figure 5.29 GaN GIT in BCM-VS with external capacitance ($V_{out} > 2V_{in}$)

5.4.2 Reverse conduction loss reduction

In BCM-VS, conduction of the transistors in reverse direction is necessary when $V_{out} > 2V_{in}$ to achieve ZCS and, consequentially, reverse conduction loss will be generated. As was analysed in 4.2.1, due to the nearly symmetric structures of both GaN HEMT and GaN GIT, reverse conduction of either type of GaN transistor is made possible by a positive V_{gd} to form the conductive channel. And accordingly, a potential difference of no less than threshold voltage of the transistor (1.7V for GaN HEMT and 1.3V for GaN GIT) is required between source and drain, which is high compared to voltage drop of body diode in a Si MOSFET (below 0.7V), and therefore the reverse conduction time should be minimized. In fact, a breakdown of conduction loss in GaN transistors in BCM-VS when $V_{out} > 2V_{in}$, which consists of both on-state conduction loss and reverse conduction loss, also reflect the necessity of shorten or even elimination of reverse conduction time when it is possible. As shown in Figure 5.30, of the conduction in GaN transistors in examples of BCM-VS with reverse conduction in previous section, reverse conduction loss contributions to 52.4% and 16.4% of total conduction loss in GaN HEMT and GaN GIT, respectively. It is worth pointing out that, as indicated by 4.1, presence of a negative V_{gs} will make the voltage drop across the transistor higher to conduct the same current. The action of enforcing a negative switch-off voltage to speed up the turn-off transient and reduce turn-off channel current in BCM, which is not adopted in this thesis, involves a complex trade-off between turn-off loss reduction and reverse conduction loss reduction.

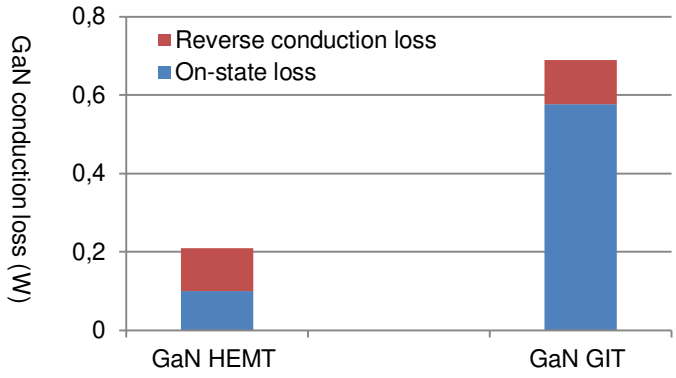


Figure 5.30 Loss breakdown of conduction loss in GaN transistors in BCM-VS $V_{out} > 2V_{in}$

Reduction or even elimination of reverse condition time, and also reverse conduction loss, can be achieved by switching on the transistor before inductor current returns to zero in BCM-VS in situation of $V_{out} > 2V_{in}$. In fact, when the converter is working with fixed input and output conditions as well as constant frequency, early turn-on in BCM-VS when $V_{out} > 2V_{in}$ would, apart from affects reverse conduction time, also influences switching and on-state conduction conditions of the transistor: a). lowering peak current and, consequentially, decreases turn-off loss (if there is any) and eases voltage stress of the transistor; b). shift turn-on condition from

ZCS with V_{Rev} to certain current with V_{Rev} and thus causing more turn-on loss; c) after the transistor is switched-on, the negative current will firstly flow through transistor channel while linearly increases to zero, whether on-state loss will increase depends on the specific timing of turn-on which affects the value of RMS current in the end. So, determination of turn-on timing is a complex trade-off between reverse conduction loss, turn-on loss and on-state RMS loss to achieve loss minimization. In practice, however, as the reverse conduction voltage drop is usually negligible in comparison to the input voltage, reverse conduction time needed in case of pursuing ZCS (t_{Rev}) is almost the same as the time needed for channel current to increase linearly from certain negative value to zero when early turn-on is initiated ($t_{on\text{-}neg}$).

$$t_{Rev} = \frac{L_B I_{neg}}{V_{in} + V_{Rev}} \tag{5.3}$$

$$t_{on-neg} = \frac{L_B I_{neg}}{V_{in}} \tag{5.4}$$

And therefore:

- Turn-off loss is not affected. With proper control when switching cycle is fixed, the on-time of charging inductor current from zero to the peak value will hardly be changed, and so does the peak current and, in the end, turn-off loss and voltage stress of the transistor.
- Total conduction loss (sum of reverse conduction and on-state RMS loss) will be reduced. When switched with a current of I_{neg} and a voltage of V_{Rev}, the ratio between reduced reverse conduction loss and increased on-state RMS loss is determined by $\frac{2I_{neg}R_{ds-on}}{3V_{Rev}}$, which means that, thanks to the low on-state resistance of GaN transistors, gain can be obtained in total conduction by switching on prior to zero current point until value of the reverse conducting current goes extremely high (102A in case of GaN HEMT and 26.4A for GaN GIT).
- Turn-on loss can be eliminated with proper timing prior to the ZCS point. With high operation frequency, time needed for drain-source voltage to drop from zero to $-V_{Rev}$ (the beginning instance of reverse conduction) would be negligible and turn-on at ZVS would have the same gain as turn-on at the very beginning of reverse conduction in terms of conduction loss and turn-off loss but with further benefits of turn-on loss elimination.

It is therefore safe to conclude that, although it seems that reduction of reverse conduction loss would affect turn-off and on-state RMS loss, given the nature of GaN devices, especially the low on-state resistance and the negligible voltage drop in reverse conduction (in comparison to input voltage, the voltage drop is still quite high in comparison to that of a body diode in a Si MOSFET), the elimination of the reverse conduction will influence turn-off loss but decrease total conduction

loss. In particular, turn-on of the transistors in BCM-VS when $V_{out} > 2V_{in}$ with zero voltage (ZVS) would maximize the benefits brought about by not switching on at ZCS as turn-on loss is eliminated, especially at high frequency. ZVS BCM-VS, accordingly, is more suitable for GaN device in high frequency applications when $V_{out} > 2V_{in}$. To distinguish the two different switching conditions in BCM-VS, the zero current turn-on with valley voltage of $(2V_{in}-V_{out})$ in case of $V_{out} \leq 2V_{in}$, is termed as ZCS BCM-VS. It worth be pointed out that, in case of $V_{out} > 2V_{in}$ in a boost converter, zero switching loss can be achieved by running the converter in the mode of BCM-VS as ZVS at turn-on is facilitated and ZCCS at turn-off is made possible (naturally when turn-off current is lower than 2.2A and with the help of external capacitance when turn-off current is higher than 2.2A). And thus, BCM-VS under this condition is an ideal mode for usage of GaN as the advantages of GaN transistors, fast switching speed and low on-state resistance, can be fully taken of.

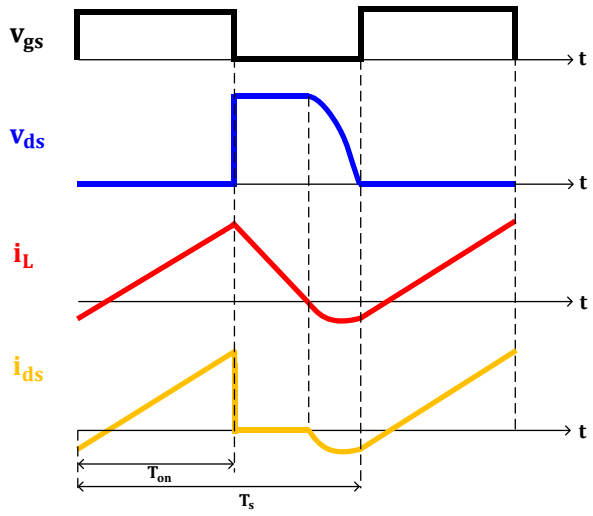


Figure 5.31 Modified BCM-VS with ZVS turn-on when (ZVS BCM-VS) $V_{out} > 2V_{in}$

Turn-on of GaN HEMT in ZVS BCM-VS was carried out in the BCM-VS example from previous section, in which the GaN HEMT is tested at 1MHz and switched on at ZCS after a reverse conduction from -0.6A to zero with duration of about 250ns and a voltage drop about 2.2V. By switching on at ZVS without changing input, output and switching frequency, peak current stays as unaffected, loss in GaN HEMT, which consists of only conduction loss, is reduced from 0.2W to 0.1W.

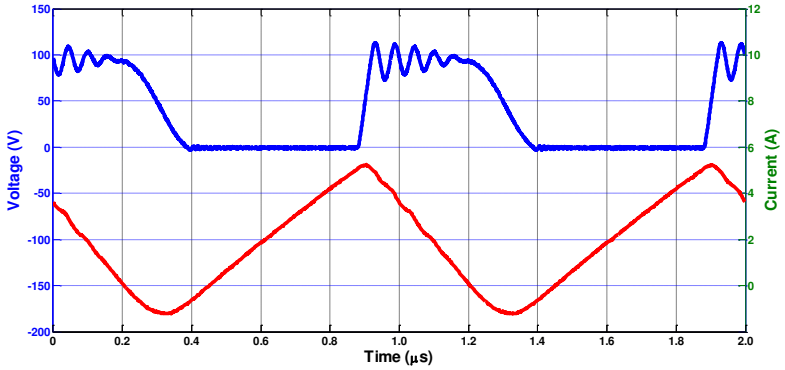


Figure 5.32 Waveform of GaN HEMT in BCM-VS with ZVS turn-on

Turn-on of GaN GIT in ZVS BCM-VS was illustrated by shifting the turn-on point previous to the point where inductor current returns zero from negative in the BCM-VS II example in Table 5-5. The earlier turn-on is helpful in reducing reverse conduction loss from 0.11W to zero while switching and on-state conduction loss remains almost unchanged. Loss in GaN GIT in BCM-VS II therefore is reduced from 0.7W to 0.6W. And therefore, ZVS BCM-VS is also beneficial for further loss reduction with GaN GIT.

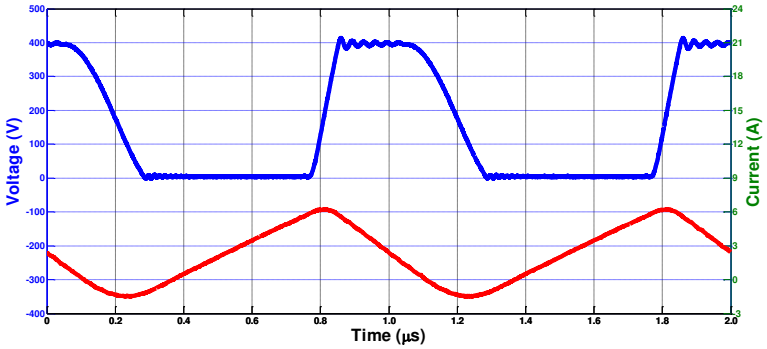


Figure 5.33 Waveform of GaN GIT in BCM-VS with ZVS turn-on

With the design trade-offs in both ZCS BCM-VS and ZVS BCM-VS taken into consideration, BCM-VS, instead of only providing ideal switching conditions for GaN HEMT and, in some cases, GaN GIT, can be regarded as an ideal application for GaN devices from overall loss minimization point of view. The need of low voltage, low current turn-on of GaN transistors are perfectly satisfied by the mode of BCM-VS which facilitates low voltage, ZCS turn-on when $V_{out} \leq 2V_{in}$ and the ZVS turn-on when $V_{out} > 2V_{in}$. Besides, when turn-off current is high enough, channel current reduction can be achieved by proper actions e.g. paralleling external capacitors (especially in ZVS BCM-VS), which is hardly possible in any other mode. At the same time, the addition of external capacitance also helps to mitigate voltage stress of the transistors. And therefore, with additional actions, optimal utilization of GaN transistors can be achieved in the mode of BCM-VS.

5.5 Boundaries and limitations of using GaN devices in BCM-VS for high frequency operation

So far, the exploration of potentials of GaN devices (high frequency operation capacity in this thesis) in existing power electronic systems (boost converter as a case study in this work) were performed by focusing exclusively on how to best accommodate GaN transistors (minimizing loss in the transistors as the major concern) so that benefits of the devices can be fully exploited (in this case study, frequency can be pushed up as high as possible with loss in the transistors kept low). And it was found that, optimal utilization of GaN transistors for high frequency operation can be realized in the mode of BCM-VS in a boost converter as all the desired switching conditions can be fulfilled. Although BCM-VS has been successfully used in PFC boost converters to achieve loss reduction of transistors, the usage are limited to relatively low frequency (below 400kHz in general). Before adopting the mode with GaN devices applied at further increased frequency, a thorough understanding on boundaries and limitations of high frequency operation of a BCM-VS boost converter is needed to guide proper design and implementation of a GaN based high frequency boost converter. In this section, the effect of pushing of frequency on performance of a BCM-VS boost converter will be analysed. The examination of the effects will be performed firstly on main components in a boost converter, namely transistor, inductor and freewheeling diode, respectively and then on the overall performance of the whole converter.

It should be noted that, the analysis on loss mechanisms in GaN transistors and identification of BCM-VS as an optimal mode for the transistors in previous sections were limited to high voltage, low current conditions as the focus of this thesis is to explore potential of GaN devices in converters of which the input is connected to the mains. It has been demonstrated that GaN transistors have large output capacitance, high C_{ds}/C_{gd} ratio at high voltage and low on-state resistance and by applying the transistors in BCM-VS, the parasitics, are effectively utilized as discharging of the large output capacitance at high voltage can be avoided at the expense of increased turn-off current and RMS current in the transistors. Exploration of boundaries and limitations on performance of the GaN based boost converter, therefore, is also confined to that in high voltage, low current operation conditions of BCM-VS.

5.5.1 Influence of high frequency operation of BCM-VS on GaN transistor

The mode of BCM-VS, in essence, utilizes a quasi-resonant stage to shift switching and conduction conditions of components in the boost converter and inevitably introduces a ringing time that is determined by the boost inductance and parasitic capacitance of the transistor (parasitic capacitor of the freewheeling diode is effectively paralleled to the transistor). With increase of frequency, the ratio (δ_r) between ringing time and a switching cycle increases, as indicated by (5.5) where $V_{in,}$ I_{in}, V_{out} denotes the input and output conditions (input voltage, current

and output voltage, respectively) while f_s,and C_t stands for the operation frequency and total output capacitance of the transistor (sum of C_{oss} of a GaN transistor and external capacitance C_{ext}), respectively, leading to changes of switching and/or conduction conditions of components in a boost converter.

$$\delta_r = \begin{cases} \dfrac{acos(\frac{V_{in}}{V_{in}-V_o})}{acos\left(\frac{V_{in}}{V_{in}-V_o}\right)+\sqrt{\frac{2I_{in}V_o}{V_{in}(V_o-V_{in})f_sC_t}+\frac{2V_o^2}{V_{in}(V_o-V_{in})}}}, & V_{out} > 2V_{in} \\ \dfrac{\pi}{\pi+\sqrt{\frac{2I_{in}V_o}{V_{in}(V_o-V_{in})f_sC_t}+\frac{4V_o}{V_{in}}}}, & V_{out} \le 2V_{in} \end{cases} \tag{5.5}$$

When input and output conditions are invariable, pushing up operation frequency of CCM (when ripple current is fixed) and BCM will not change switching (voltages and currents at turn-on and turn-off) and conduction conditions (on-state RMS current) of transistors (in CCM turn-on current could be influenced by the reverse recovery current of freewheeling diode, the effect is not considered in this part as the problem can be mitigated by proper design e.g. employing SiC diodes). In BCM-VS, however, increase of operation frequency would result in enlarged peak current and RMS current in the transistor, as expressed in (5.6) and (5.7). And therefore, turn-off energy will increase and, when the peak current is high enough, so does the turn-off loss. The increase in loss-related turn-off energy and on-state RMS current, together with the constant turn-on energy, limit the maximum applicable frequency and current of the transistor.

$$I_p = \begin{cases} \dfrac{2(I_{in}+V_of_sC_t)}{1-\delta_r}, & V_{out} > 2V_{in} \\ \dfrac{2[I_{in}+2(V_o-V_{in})f_sC_t]}{1-\delta_r}, & V_{out} \le 2V_{in} \end{cases} \tag{5.6}$$

$$I_{RMS-GaN} = \begin{cases} 2(I_{in}+V_of_sC_t)\sqrt{\dfrac{V_o-V_{in}}{V_o(1-\delta_r)}}, & V_{out} > 2V_{in} \\ 2[I_{in}+2(V_o-V_{in})f_sC_t]\sqrt{\dfrac{V_o-V_{in}}{V_o(1-\delta_r)}}, & V_{out} \le 2V_{in} \end{cases} \tag{5.7}$$

Furthermore, with frequency being pushed up, the action of adding external capacitance to GaN transistors in BCM-VS to achieve turn-off loss reduction (if there is any) also has boundaries beyond which the practice is no longer beneficial. In 5.4.1, the approach of minimizing switching loss of GaN transistors by paralleling proper external capacitors was carried out assuming invariable switching and conduction conditions of the transistors. The action of adding capacitance to a GaN transistor, in fact, would effectively increase the proportional of ringing time

in a constant switching cycle as indicated by (5.3) and thus also enhances peak current and on-state RMS current in GaN transistors. With pushing operation frequency further up, the net effect of higher frequency and higher capacitance needed to achieve turn-off loss reduction would, from loss point of view, limits the frequency span in which adding external capacitance helps. To be more specific:

- In ZCS BCM-VS, boundary of operation frequency exists on whether it is still necessary to introduce external capacitors as the turn-off loss reduction by larger capacitance added at higher frequency would be well compensated by the increase of turn-on loss and on-state loss.
- In ZVS BCM-VS, where all switching loss is shifted to on-state loss to take advantage of the low on-state resistance of the GaN transistors, frequency limitation is caused by the increasing RMS current which is the result of both increased frequency and larger capacitance added.

Using the two examples of GaN GIT in a 300W BCM-VS boost converter in specified in Table 5-6 as case studies, with frequency be pushed up from 100kHz to 10MHz, ratio of the ringing time gets enlarged in a switching cycle by 5.61 times in ZCS BCM-VS and 6.83 times in ZVS BCM-VS, as suggested by Figure 5.34, leading to increases in turn-off currents (2.07times in ZCS BCM-VS and 1.68 times in ZVS BCM-VS) and RMS currents (1.67 times in ZCS BCM-VS and 1.57 times in ZVS BCM-VS) in both situations. And consequentially, when GIT is subjected to natural convection, maximum operation frequency of ZCS BCM-VS and ZVS BCM-VS is limited to 444.5kHz and 155.7kHz, respectively.

Table 5-6 Specifications for exploration of frequency limits

of GaN GIT based boost converter

Mode		V_{in}(V)	V_{on}(V)	I_{on}(A)	I_{off}(A)
CCM		200	400	1.35	1.65
BCM		200	400	0	3
BCM-VS	ZCS	260	120	0	3.2
	ZVS	120	1.3	0	6.6

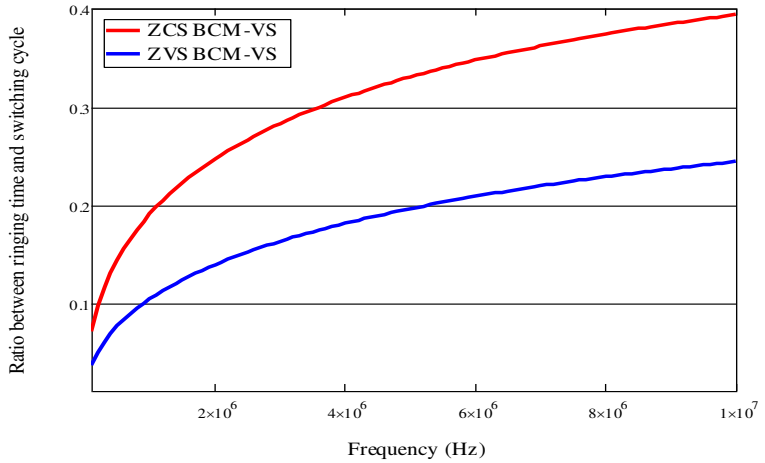


Figure 5.34 Increase of ringing time proportion with increment of frequency

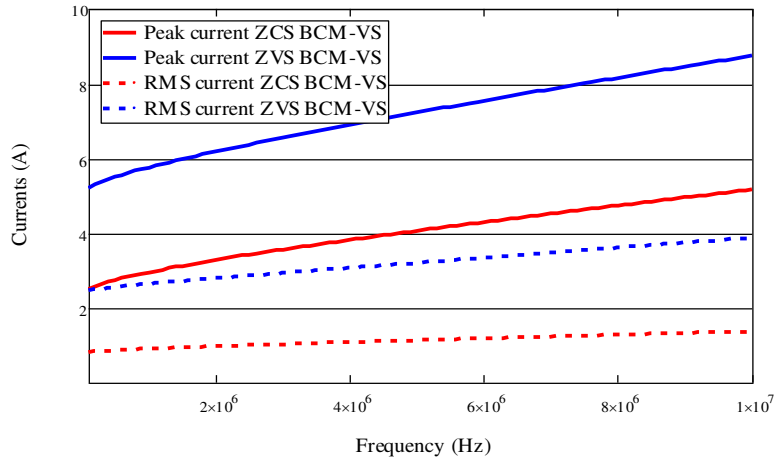


Figure 5.35 Increase of currents in GaN with pushing-up of frequency

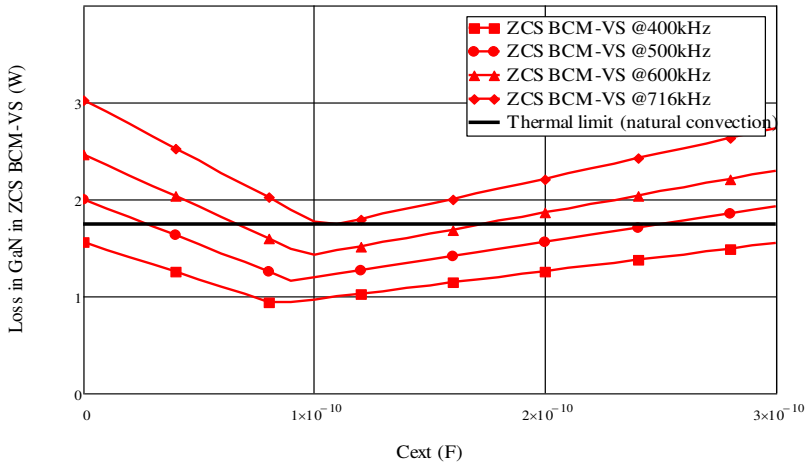


Figure 5.36 Influence of external capacitance on loss in GaN in ZCS BCM-VS

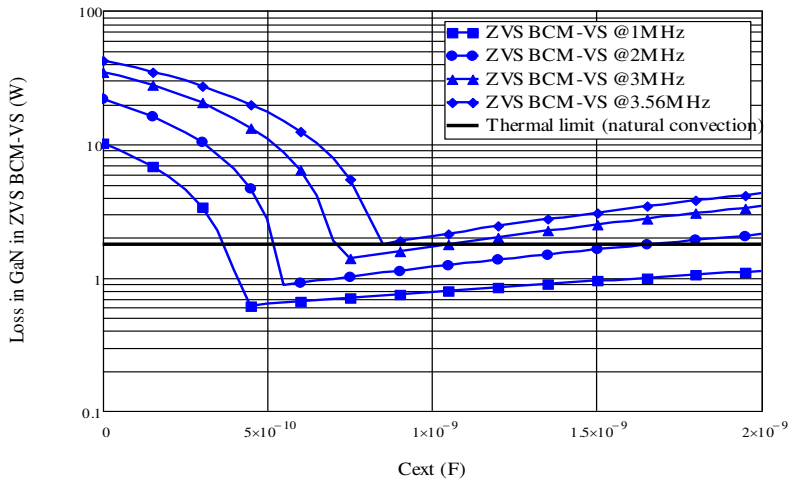


Figure 5.37 Influence of external capacitance on loss in GaN in ZVS BCM-VS

Paralleling external capacitors to GaN GIT in the ZCS BCM-VS example at elevated frequencies, as shown in Figure 5.31, increases the maximum achievable frequency to 741kHz when GIT is confined to natural convection and, in case of the ZVS BCM-VS example, the frequency is pushed up to 3.63MHz. Thermal management actions help to extend possible frequency span and, because of the increase of currents in BCM-VS, the extension ratio is less than that in other modes. For instance, using the specified modes in Table 5-6 as case studies, maximum achievable operation frequency of GaN GIT under natural convection (only $R_{J\text{-}A}$ of the GIT) and with thermal managements ($R_{J\text{-}C}$ of GIT, thermal interface material and a heatsink) were explored and presented in Table 5-7. Limits of thermal managements of GaN GIT in this work is considered using the measured results in [5-6]: with a bright aluminum plate that has a fixed thickness of 1/8 inch and a square surface, which will be positioned vertically as heatsink for a power transistor, scales the size of the surface area linearly in length and width from 5 in^2 to 150 in^2. It was measured that a practical limit on thermal resistance of 1.4 °C/W exists, as shown in Figure 5.38.

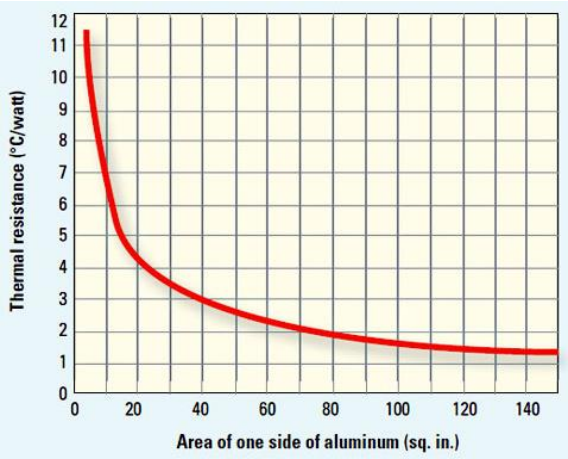


Figure 5.38 Thermal resistance of an aluminum plate with fixed thickness [5-6]

Table 5-7 Frequency limits of GaN GIT in different operation modes

Operation mode		Maximum achievable frequency		
		Natural convection	With thermal management	Increment ratio
CCM		136.1kHz	2.91MHz	21.3
BCM		155.7kHz	3.32MHz	21.3
BCM-VS	ZCS	444.5kHz	5.02MHz	11.3
	ZVS	155.7kHz	3.12MHz	20.0
BCM-VS with C_{ext}	ZCS	716 kHz	5.59MHz	7.81
	ZVS	3.56MHz	7.15MHz	2.01

- In CCM and BCM, switching energy remains constant with the increase of frequency and, as on-state loss is negligibly small in comparison to switching loss in the considered frequency range (100kHz~10MHz), increment ratio of maximum achievable frequency is as almost the same as the reduction ratio of thermal resistance from junction to ambient;
- BCM-VS generally can enable higher operation frequency than CCM and BCM, especially when paralleling external capacitors for loss minimization is an option. Addition of external capacitors is more beneficial in the mode of ZVS BCM-VS when pushing-up of frequency is the concern as the switching loss is shifted to on-state conduction loss while in ZCS BCM-VS turn-off loss reduction is accompanied by the increase of turn-on loss and on-state loss;
- In the specific examples of BCM and ZVS BCM-VS, switching energy of BCM (10.87 uJ) is in fact higher than that of ZVS BCM-VS (10.16 uJ at 100kHz), as both turn-off loss and conduction loss increases in ZVS BCM-VS, the two modes have the same maximum frequency when the device is subjected to natural convection. With the improvements in thermal performance, increment ratio of BCM exceeds that of ZVS BCM-VS as switching and conduction conditions of BCM are invariable while, in ZVS BCM-VS, the conditions change over frequency;
- With the thermal performance being improved, frequency increments in BCM-VS where are not as much as that in CCM and BCM due to the changes in switching and condition conditions and, when external capacitors added for loss minimization, the increments are even less because of the net effects of adding external capacitance and pushing-up of frequency on switching and conduction currents;
- Frequency increment ratio in the ZCS BCM-VS example is lower than that in the ZVS BCM-VS one as: a) both turn-on and turn-off loss increases in the former mode while in the latter one turn-on loss is zero; b) variation-rate of the proportion between the dead time and a switching cycle is larger in the former mode than in the latter and, as a

consequence, so does the turn-off energy and RMS currents. In BCM-VS with external capacitors, frequency increment ratio is higher in ZCS BCM-VS than in ZVS BCM-VS because in ZVS BCM-VS, where all the switching loss is transferred to conduction loss, much larger capacitance is needed than in ZCS BCM-VS (in the two specific examples, 6 times as high as in ZCS BCM-VS) and, together with the increase of frequency, variation rate of the deadtime ratio reverses: the rate is larger in ZVS BCM-VS than in ZCS BCM-VS.

- In all the ZVS BCM-VS cases switching loss were minimized to zero while conduction loss are enlarged. In other words, this mode shifts switching loss in GaN devices to conduction loss to take advantage of the low on-state resistance of GaN technology. Maximum achievable frequency of GaN in BCMV-VS is limited by on-resistance.

In extreme conditions, where the effects of thermal management are always satisfactory i.e. the junction-to-case thermal resistance of the transistor dominates in thermal path and driving requirements can always be fulfilled, paralleling external capacitor to GIT in ZCS BCM-VS is beneficial when switching frequency is below 6.25MHz and hardly any gain can be obtained at higher frequency since reduction in turn-off loss is well compensated mainly by increment in turn-on loss. Loss minimization of ZVS BCM-VS by converting turn-off loss to on-state loss also ceases to be rewarding beyond 9.4MHz.

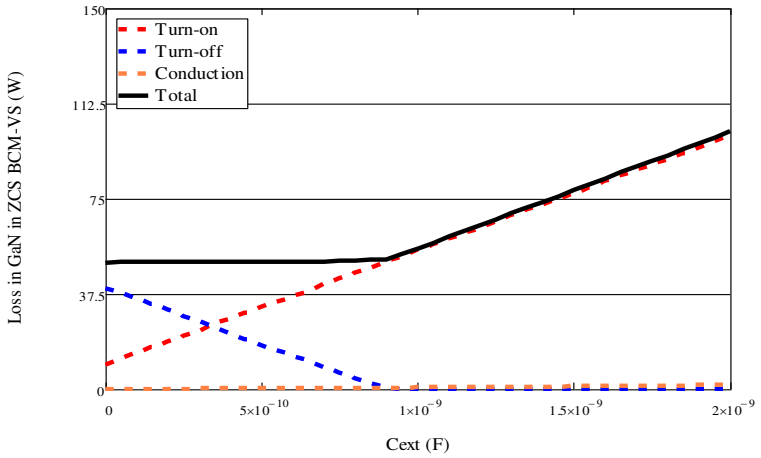


Figure 5.39 Influence of external capacitance on loss in GaN in ZCS BCM-VS at 6.25MHz

To sum up, the ringing time that is inherent with BCM-VS will shift switching and conduction conditions of a GaN transistor as frequency varies. The ratio of the ringing time over a switching cycle increases with operation frequency and, consequentially, leads to increased peak and RMS current in GaN transistors, which, together with parasitic elements of the transistors, enlarges on-state loss and loss-related turn-off energy when the peak current is high enough. Maximum applicable frequency of applying GaN transistor in the mode of BCM-VS, accordingly, is limited. Besides, the practice of adding external capacitance to reduce loss-related turn-off energy would

also effectively increase the proportion of ringing time in one switching cycle and also contribute to peak and RMS current enlargement, which leads to the demand of larger capacitance. The net effect of higher frequency and larger capacitance needed limits the maximum frequency that beyond which the action of paralleling external capacitance is no longer beneficial in terms of loss reduction.

5.5.2 Influence of high frequency operation of BCM-VS on freewheeling diode

When operation frequency of a BCM-VS boost converter with fixed input and output specifications is pushed up, conduction conditions of the freewheeling diode will also be changed. Similar to the case with the GaN transistor in BCM-VS, RMS current through the freewheeling diode increases with operation frequency of the converter to compensate the existence of the ringing time which does not contribute to power transfer. Besides, the addition of external capacitance to transistors in BCM-VS at fixed frequency effectively prolongs the dead time and thus further increases the RMS current in the freewheeling diode. And therefore, either freewheeling diodes with higher current conduction capability and limited loss at higher currents are needed at higher frequency in the mode of BCM-VS or with the same diode being applied to push up frequency of BCM-VS, maximum frequency is limited to keep the loss in the diode under control.

$$I_{RMS-diode} = I_{RMS-GaN}\sqrt{\frac{V_{in}}{V_o - V_{in}}} \tag{5.8}$$

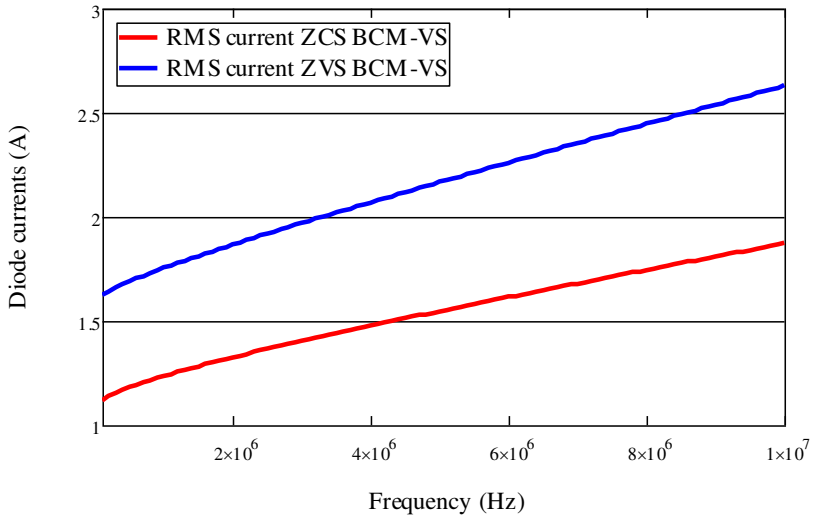


Figure 5.40 Influence of frequency on current in freewheeling diode

(pushing up the GIT based BCM-VS examples from 100kHz to 10MHz)

To conclude, pushing up operation frequency of a BCM-VS boost converter with certain input and output conditions would lead to increased currents in the freewheeling diode. And accordingly, diodes with higher current capability is demanded at higher frequency or maximum frequency is limited by the increasing loss in the freewheeling diode.

5.5.3 Influence of high frequency operation of BCM-VS on boost inductor

In CCM and BCM, switching energy that needs to be stored and released in one switching cycle decreases linearly with increase of frequency in a boost converter with specified input and output conditions. In BCM-VS, however, switching energy requirement decreases beyond linear as indirect power transfer, which is the cause of energy storage, is less demanding with the effective duty cycle reduced when switching frequency is pushed up. The less energy storage requirement, together with the increase of peak current, results in value of needed inductance decreases more than inverse proportional with increase of operation frequency, as indicated by (5.9). Moreover, the larger external capacitance needed at higher frequency would lead to further reduction of the inductance as the ringing time will be further effectively prolonged in a switching cycle.

$$L_{vs} = \begin{cases} \dfrac{1}{\{f_s[\sqrt{C_t}\,aco\,s\left(\dfrac{V_{in}}{V_{in}-V_o}\right) + \sqrt{\dfrac{2I_{in}V_o}{V_{in}(V_o-V_{in})f_s} + \dfrac{2V_o^2C_t}{V_o(V_o-V_{in})}}]\}^2}, & V_{out} > 2V_{in} \\ \dfrac{1}{\{f_s[\pi\sqrt{C_t} + \sqrt{\dfrac{2I_{in}V_o}{V_{in}(V_o-V_{in})f_s} + \dfrac{4V_oC_t}{V_{in}}}]\}^2}, & V_{out} \le 2V_{in} \end{cases} \tag{5.9}$$

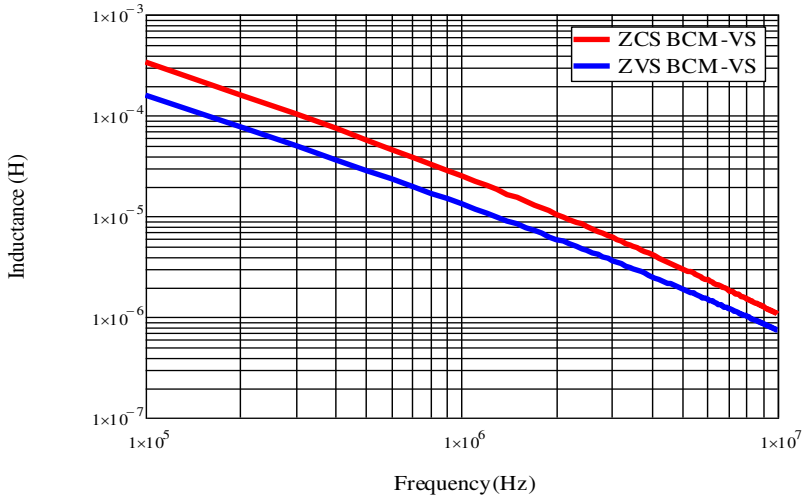


Figure 5.41 Variation of inductance needed in BCM-VS

(plotted with specifications from the GIT BCM-VS examples in Table 5-6)

The effects of high frequency operation on performance of the boost inductor e.g. temperature, size, etc., however, is less straightforward as properties of the device are usually coupled with each other. For instance, size scaling of the inductor, which is made possible by the declined

energy storage demand, interacts with loss of the inductor that is both frequency and size dependent. Besides, design and implementation of a magnetic component involves diversified technologies e.g. core materials and shapes, winding technologies, packaging method, etc. that could lead to different design trade-offs, and consequentially overall performance of the component, in different applications. And therefore, full assessment on the influence of pushing up operation frequency on performance of a boost inductor requires thorough investigations on both the interactions between different properties with variation of frequency and the implementation approaches that deals with design trade-offs under specified design considerations [5-9]- [5-11].

In this section, assessments of loss and size of a boost inductor in BCM-VS under the variation of frequency is performed qualitatively with the "modified performance factor (F_{MPF})" for an inductor with a single layer winding, which was initial developed to evaluate capabilities of magnetic materials for power conversion applications [5-12]. The F_{MPF} in (5.10), where f is the frequency under consideration and B_{pk} is the peak flux density in a magnetic core, accounts for frequency-depend skin-effect loss in the winding and characterizes performance of a magnetic core under a fixed loss density (a value of 500mW/cm^3 is usually used for magnetic components with small volume [5-13]). The F_{MPF} can be used to identify the size and loss of an inductor over frequency because: a) it maintains a constant winding loss and a specified loss density in the core, and thus, a smaller size is accompanied by lower loss at the same time (assume that size of the core dominates); b) a larger value of F_{MPF} means higher flux density is possible and, as a result, smaller size. As plotted with the datasheet information of two type of commercially available core materials suitable for >1MHz operation in Figure 5.41, an inductor with a fixed geometry but variable dimensions would achieve minimum size, and also loss, around 1MHz when 3F4 or 3F45 is used as the core material [5-14] [5-15]. Pushing up frequency of BCMV-VS beyond 1MHz would cease the gain in both loss and volume reduction of the boost inductor.

$$F_{MPF} = B_{pk} f^{\frac{3}{4}} \tag{5.10}$$

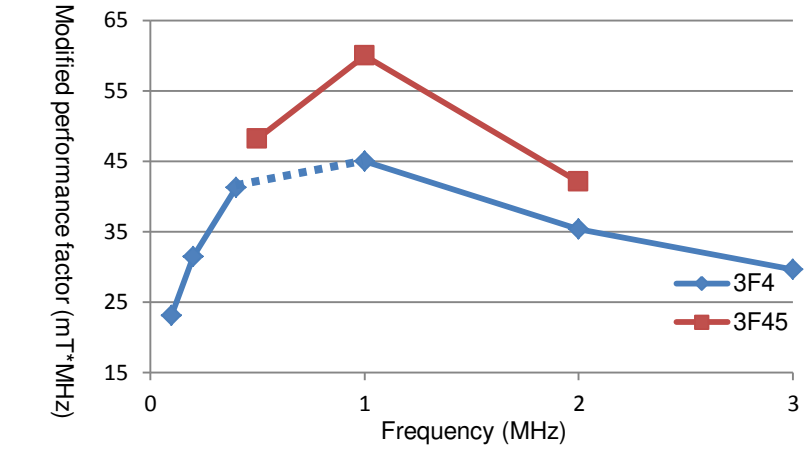


Figure 5.41 Modified performance factor of 3F4 and 3F45

It should be noted that the F_{MPF} is effective in designs where core loss is the major design constrain and thus only provides a simple way of estimating size and loss of inductors in which the two aspects of the winding is not critical in comparison with the core [5-14]. In fact, with BCM-VS, the F_{MPF} analysis does not exactly fit, as RMS currents through inductor will get enlarged with the increase of frequency. And therefore, to maintain constant winding loss, not only the skin-effect of winding conductor should be considered to account for effects of frequency on winding loss, but also the dependence of RMS current on frequency should be taken care of. The increase in RMS current is considered as having no effect on the shape of the F_{MPF} plot over frequency in Figure 5.41 as the limited increment should not change the assumption that core loss still dominates. Besides, it should also be pointed out that it was also assumed in the F_{MPF} method that the design is concerned with core loss rather than saturation [5-13] [5-14]. For more accurate estimation, comprehensive methods are needed.

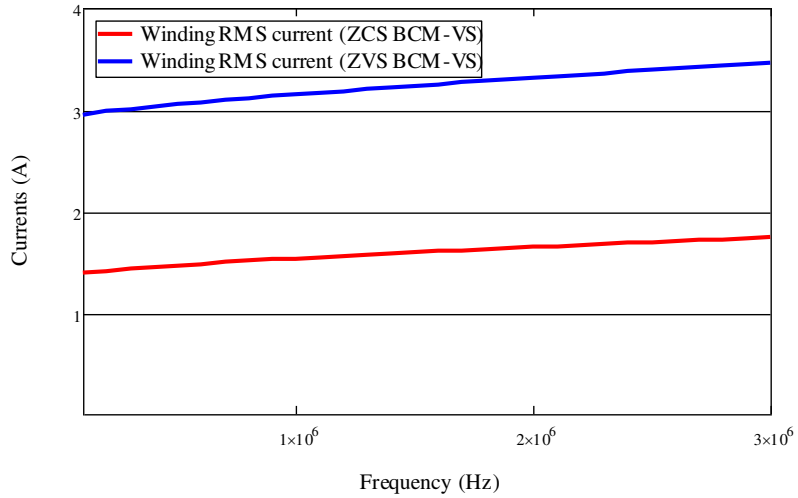


Figure 5.42 Influence of frequency on RMS current in inductor winding

(Plotted with BCM-VS examples from 100kHz to 3MHz)

5.6 Summary

In this chapter, loss in GaN transistors are analysed firstly, using a boost converter as a platform, to find out the desirable utilization conditions of the transistors in which high frequency operation of the devices is possible. It was found out that, with the two different types of GaN transistors of GaN HEMT and GaN GIT, low voltage, low current turn-on and low channel current turn-off are the desired switching conditions. Since switching and conduction environment of transistor(s) is mainly determined by the operation mode of a converter, operation modes in a boost converter is examined to find out whether one of the existing modes can naturally facilitate the desired operation conditions for GaN transistors or extra actions such as connecting snubbers to the transistors is needed for creating such conditions. It was revealed that the mode of BCM-VS that is commonly used in PFC boost converters provides exactly the needed switching conditions. The particular mode, however, also introduces high peak current and ignite reverse conduction of the transistors, which would lead to high voltage stress, high turn-off loss and high conduction loss. Optimal utilization of GaN transistors are achieved by modifying the BCM-VS mode with the actions of paralleling proper external capacitance and turn-on at ZVS when $V_{out} > 2V_{in}$. Boundaries, in terms of frequency, of the BCM-VS modes were then investigated to guide proper design of a high frequency boost converter.

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Chapter 6. Design and optimization of a GaN GIT based high frequency PFC boost converter

6.1 Introduction

Work on loss modeling and analysis of GaN transistors as well as exploration of approaches for optimal utilization of them in previous chapters have proved that the new technology does live up to the expectation of high frequency operation when they are well accommodated. Although the high frequency operation potential of GaN devices was successfully illustrated in a boost converter, demonstration of the benefits of the new technology in real applications has not been performed.

This chapter focuses on design and optimization of a GaN based high frequency application, using PFC converter as an example, to maximize the benefits out of the new technology in a real application where not just the transistor but also other components in the converter are taken into account. As it was concluded in previous chapters that boost converter will remain as the most preferred choice for implementing PFC at high frequencies and that the mode of BCM-VS in PFC boost converter is perfect for accommodating GaN transistors, a GaN based PFC boost converter with the mode of BCM-VS will be investigated. Analytical modeling of the whole converter is firstly developed, which consists of modeling of boost inductor, freewheeling diode and GaN transistor. Loss minimization of the converter is then conducted with the assistant of the model, the core of which is to select a proper external capacitor. Experimental implementation of the PFC boost converter will be introduced and results of a 3MHz PFC boost converter are analyzed.

6.2 Loss modeling of a GaN GIT based PFC boost converter

Being the most widely adopted topology for implementing PFC stage in a AC/DC converter with conventional Si technology, boost converter will remain as the preferred choice for realizing PFC at elevated operation frequency that can be enabled by the new GaN technology because, as was discussed in chapter 3, merits and demerits of DC-DC converters that are potential possible to be used as a PFC preregulator are hardly affected when frequencies of the converters are scaled up equally. A PFC boost converter could operate in several different operation modes, of which the BCM-VS mode naturally provides desirable switching conditions for GaN transistors and, in particular, with additional actions of paralleling external capacitors and facilitating ZVS turn-on when $V_{out} > 2V_{in}$, optimal usage of GaN devices can be achieved. And therefore, a boost converter with the operation mode of BCM-VS is used as the PFC converter in this work.

6.2.1 Analytical loss modeling of inductor and diode

To perform design of a high efficiency GaN based boost converter to be used as PFC, loss modeling of the whole converter is a must. In a boost converter, apart from the transistor, losses in the boost inductor and the freewheeling diode are also key components contributing to total loss in the converter. Loss in a single-layer-winding based inductor as well as conduction in a freewheeling diode are performed in this section.

6.2.1.1 Analytical loss modeling of boost inductor

In general, loss in a cored-inductor consists of two parts, core loss and winding loss, both has been modelled analytically in published work with reasonably good accuracy.

Prediction of losses in magnetic materials/cores are mainly performed through empirical methods since exact descriptions on physical procedures of magnetization e.g. time and space distribution of magnetization changes is unknown and, accordingly, practical means for loss calculation cannot be provided [6-5][6-7]. The empirical models, in general, were developed based on the basic theory of loss mechanisms in magnetic materials. Currently, there are three different types of such empirical approaches: hysteresis model, loss separation model and empirical equations.

- **Hysteresis models** express the hysteresis loops mathematically and predict losses in a magnetic core in switching cycles with the expressions. For instance, in [6-9], a differential equation was used to characterize static behaviours of ferri- and ferromagnetic materials and an iterative process was adopted to estimate parameters in the equation. In [6-10], on the other hand, a statistical approach with weight functions was used to describe static characteristics of magnetic materials. The available hysteresis models are subjected to limited practical application because: a). the models are complicated and, due to the fact that parameters that are not available from data provided by manufactures are demanded, extensive experimental efforts are needed before application of them. In differential-equation based models, 6 different parameters, including magnetic domain interaction factor, influence of thermal disordering, etc., may be needed [6-11]; b). accuracy of the models is not constantly satisfactory as, in most cases, only static behaviours are accounted for while dynamic effects are not considered [6-6]
- **Loss separation models** separates losses in a magnetic core into three parts: static hysteresis loss, dynamic eddy-current loss and excess loss. Static hysteresis loss is caused by the area of the hysteresis loop and depends on both peak flux density and frequency [6-7]. Dynamic eddy-current loss is generated by the eddy current that flows through the magnetic core and is affected by geometry of the core and resistivity of core material [6-4][6-7]. Excess loss, sometimes also referred to as anomalous eddy-current

loss, is, in fact, an artificial loss term that is used to describe the nonuniform change of magnetic field caused by domain-wall movements [6-6]. It has been demonstrated that the third loss component, which is least well-understood, normally is the bulk of total loss and when it is not considered, error between modelled loss and measurement results is between 200%~2000% [6-6]. Separation loss models are seldom used in practice because only the dynamic eddy-current loss can be really modelled or calculated, the other two parts have to be determined through experimental measurements. Besides, with the calculation of dynamic eddy-current loss, resistivity of the material provided by the manufactures is not always accurate, especially considering the fact that this factor may vary significantly with frequency and accuracy of the models is therefore not always sufficient [6-4].

- **Empirical equations** are formulas developed to approximate total loss in magnetic cores. These formulas are all of simple form and desires only empirical parameters that are readily available with each kind of magnetic materials. And, when used properly according to their preferred applicable conditions, satisfactory accuracy and simplicity can be achieved simultaneously [6-4].

  *Steinmetz equation (SE)***,** the power law formula of (6.1) (in which P_v is the time-average power loss per unit volume, B is the peak flux amplitude and f is the frequency of sinusoidal excitation while k, α, and β are the three empirical parameters), is the most widely known empirical model**.** It is of high accuracy for sinusoidal flux waveforms and the three empirical parameters (usually referred to as Steinmetz coefficients) are normally provided by manufactures [6-6]. As a matter of fact, the equation is valid only for sinusoidal excitations and the Steinmetz coefficients are typically extracted from plots of loss for sinusoidal excitation in datasheets. Direct application of SE for loss prediction of magnetic components in power converters is, therefore, not recommended as magnetic components are usually subjected to non-sinusoidal flux waveforms and better calculation approaches are needed. In [6-12] and [6-13], loss in a magnetic core under an arbitrary non-sinusoidal excitation was calculated by performing Fourier expansion of the excitation waveform, then applying equation (6.1) to each single Fourier component and finally summarizing the weighted loss as superposition. This approach is, by nature, not accurate as method of superposition is only applicable with linear systems and, in the power law equation of (6.1), dependence of core loss over frequency and flux density is nonlinear. Extension of applicable range of SE to non-sinusoidal excitation conditions with accuracy and simplicity being maintained is desirable.

$$P_v = kf^{\alpha}B^{\beta} \tag{6.1}$$

Modified Steinmetz equation (MSE) is developed based on SE with the objective to estimate core losses with non-sinusoidal excitations. Enlightened by the physical understanding that core loss is directly related with re-magnetization rate i.e. time-variation of magnetic flux density, an equivalent frequency component that characterizes this re-magnetization rate is included so that calculation of core loss can be performed in time domain for arbitrary shapes of inductions. The MSE, as shown in (6-2) and (6-3) in which T_s is the switching cycle and f_r is the repetition frequency ($f_r=1/T_s$) has been proven capable of providing better fit to measurement results of triangular-excitation induced loss than SE and is also convenient to implement as no additional parameters are needed compared with SE [6-3]. The method, however, showed inconsistence with the basic SE model when used for predicting loss for sinusoidal flux waveforms [6-7]. Besides, it also showed difficulty in treating waveforms with multiple peaks [6-7]. And therefore, a more general equation is called for to overcome the anomalies.

$$P_v = k f_{eq}^{\alpha} B^{\beta} f_r \tag{6.2}$$

$$f_{eq}^{\alpha} = \frac{2}{\Delta B^2 \pi^2} \int_0^{T_s} \left(\frac{dB}{dt}\right)^2 dt \tag{6.3}$$

Generalized Steinmetz equation (GSE) is a model that is not only fully consistent with the SE for sinusoidal waveforms but also have the capacity of predicting loss for non-sinusoidal waveforms. The GSE was developed on the basis of hypothesis that core loss is a function of flux density B and its derivative dB/dt, which simplifies the actual physical phenomenon that loss is related the shape, instantaneous value and derivative of the excitation waveform [6-5]. The GSE could lead to better accuracy than MSE, particularly for waveforms with small fundamental-frequency amplitude and only requires Steinmetz coefficients.

$$P_v = \frac{1}{T_s} \int_0^{T_s} k_i \left|\frac{dB}{dt}\right|^{\alpha} (B)^{\beta-\alpha} dt \tag{6.4}$$

$$k_i = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} |cos\theta|^{\alpha} |sin\theta|^{\beta-\alpha} d\theta} \tag{6.5}$$

Improved generalized Steinmetz equation (IGSE) is an advanced version of GSE in that applicable range of the GSE model can be extended to waveforms with minor loops. In the model, power loss dependence on instantaneous flux (B) was replaced by peak-to-peak flux density (ΔB). The IGSE, in which the k_i is calculated by the same formula as GSE in (6-5), showed better accuracy than GSE and have been successfully been applied to predict loss in flux waveforms that contains minor loops. This model is considered as the best method so far for loss prediction in magnetic cores by many as it

has the widest applicable range and, at the same time, high accuracy and simplicity can be achieved simultaneously [6-4] [6-8]. In this work, the IGSE model is adopted for calculating core loss in the boost inductor due to the merits of the model.

$$P_v = \frac{1}{T_s}\int_0^{T_s} k_i \left|\frac{dB}{dt}\right|^{\alpha} (\Delta B)^{\beta-\alpha} dt \tag{6.6}$$

Loss modelling of windings at high frequency has been well-performed as theory on loss mechanisms has been well-established. In general, for a single-layer winding, the simple model in (6-7) can be used for calculating winding loss P_W when a current with a RMS value of I_{wrms} flows through the winding [6-16]. The effective resistance R_{weff} of a regular copper-wire or a foil winding can be calculated through the basic DC resistance and the Dowell factor that accounts for skin and proximity effects as well as property of winding turns, which was introduced in [6-17].

$$P_w = I_{wrms}^2 R_{weff} \tag{6.7}$$

Loss in an inductor can therefore be calculated combing the model of core loss and winding loss. In fact, with the excitation imposed to a piece-wise-linear waveform that have no minor loop like the case with a boost inductor, the IGSE equation of (6-4) can be further formulated as (6-8). Besides, through numerical integration in (6-5), a simpler quantification formula for estimating k_i can be obtained [6-6]. The total loss of a boost inductor, of which the core has a volume of V_c, can therefore be calculated using equations (6.7) ~ (6.10).

$$P_v = \frac{k_i(\Delta B)^{\beta-\alpha}}{T_s}\sum_j \left|\frac{V_j}{NA_c}\right|^{\alpha} (\Delta t_j) == \frac{k_i(\Delta B)^{\beta-\alpha}}{T_s}\left[\left(\frac{V_{in}}{NA_c}\right)^{\alpha} T_{on} + \left(\frac{V_{out}-V_{in}}{NA_c}\right)^{\alpha} T_{off}\right] \tag{6.8}$$

$$k_i = \frac{k}{2^{\beta+1}\pi^{\alpha-1}(0.2761 + \frac{1.7061}{\alpha+1.354})} \tag{6.9}$$

$$P_L = P_v V_c + P_w \tag{6.10}$$

It worth to point out that, with the IGSE model used for predicting core loss, there are limitations in terms of its effectiveness. Firstly, the best-fit Steinmetz coefficients vary with frequency and one set of coefficients only work for the specific frequency. Given the fact that limited sets of coefficients can be obtained in datasheets, choosing the appropriate coefficients can be problematic when a core is excited at a frequency that is not specified in datasheets and accuracy of the prediction has to be sacrificed. Secondly, the effect of DC bias on core loss is not included. It was made clear that core loss increases substantially with dc magnetic flux but this effect is difficult to be included in loss models as no general theory that could explain the phenomenon and permits the inclusion of the effect exists [6-14] [6-28]. So far, the DC effects can only be performed by building of so-called Steinmetz Pre-magnetization Graphs (SPG) based on

extensive measurements. The graphs record variations of Steinmetz parameters of one type of core material over different DC pre-magnetization conditions and can be used as a lookup table for calculating core loss when it is subjected to a flux waveform that has a DC bias [6-14].

6.2.1.2 Analytical loss modeling of diode conduction loss

Conduction loss in a diode will be generated when the diode is conducting in forward direction due to the voltage drop (V_F) across the device. A well-established approach of modelling the conducting behaviour is to treat the diode as a DC voltage source connected in series with a resistor. The DC voltage source (V_{F0}) stands for the on-state, zero-current voltage drop of the diode and the resistor (R_D). The voltage drop across a diode and associated conduction loss can therefore be expressed as:

$$V_F = V_{F0} + R_D i_D(t) \tag{6.11}$$

$$P_{conD} = V_{F0} I_{Fav} + R_D I_{Frms}^2 \tag{6.12}$$

In which i_D is instantaneous diode current, P_{conD} is the average conduction loss over a switching cycle, I_{Fav} and I_{Frms} is the average diode current and RMS diode current, respectively. It should be noted that both V_{F0} and R_D are temperature dependent and, whatever diode technology is utilized, thermal coefficient of the threshold voltage is negative while the coefficient is positive with resistance [6-17]. Thermal coefficient of the overall voltage drop V_F, therefore, depending on current level and specific diode technology can be either positive or negative. The influence of temperature is usually not considered in converter design stage as temperature of the diode is, apart from loss, subjected to the surrounding environment in an actual converter and, even when temperature of the diode can be accurately predicted, the data of thermal coefficients is not always available from datasheet. The conduction loss model in (6-12) is used in this work.

The selected loss models of an inductor and a diode, together with the developed loss model of GaN transistors in chapter 4, form the analytical loss model of a GaN based boost converter. And for a BCM-VS boost converter with specified input and output requirements, as the two examples of ZCS BCM-VS and ZVS BCM-VS boost converters discussed in 5.6 and quantified in equations (5.6) ~ (5.8), the currents through all the components (transistor, inductor and diode) are functions of switching frequency (f_s) and additional output capacitance (C_{ext}).

6.2.2 Loss modeling of a GaN based PFC boost converter in BCM-VS

In a PFC converter, in theory, the instantaneous input current is always proportional to voltage. With a boost converter operated in the mode of BCM-VS, such synchronization is usually achieved thorough the so-called constant on-time control, under the scheme of which on-times of the transistor in different switching cycles are the same throughout the half-line input period [6-1]. As indicated in the relationship between instantaneous voltage ($V_{in}(t)$) and current ($I_{in}(t)$) in BCM-

VS boost converter in (6-13), current naturally follows voltage when on-time (T_{on}) is fixed. Off-time, on the other hand, have to vary, causing variable frequency that is necessary for given line and load conditions. As suggested by (6-15), the lower the load, the higher the switching frequency.

$$I_{in}(t) = \frac{T_{on}}{2L_B} V_{in}(t) \tag{6.13}$$

$$T_{off}(t) = \frac{V_{in}(t)}{V_o - V_{in}(t)} \tag{6.14}$$

$$f_{sw}(t) = \frac{V_{in}^2(t)}{2L_B V_{in}} [1 - \frac{V_{in}(t)}{V_o}] \tag{6.15}$$

While losses in a simple boost converter occur in the main power components (transistor, boost inductor and freewheeling diode) at one set of input and output conditions under one specific frequency, losses in a PFC boost converter in the mode of BCM-VS, as a consequence of the constant on-time basis of the mode, is generated not only under different sets of switching and/or conduction conditions (i.e. voltage and current levels) but also at varied frequencies in different switching cycles. Besides, as was introduced in chapter 3, in a step-up type in PFC converter, an output voltage of higher than 380V is usually maintained. Loss modeling of a GaN based PFC boost converter in BCM-VS can therefore be performed with the accumulation of a finite number of loss models of a simple boost converter, which have different input and load specifications as well as frequency but with fixed on-time of transistors and a constant output voltage.

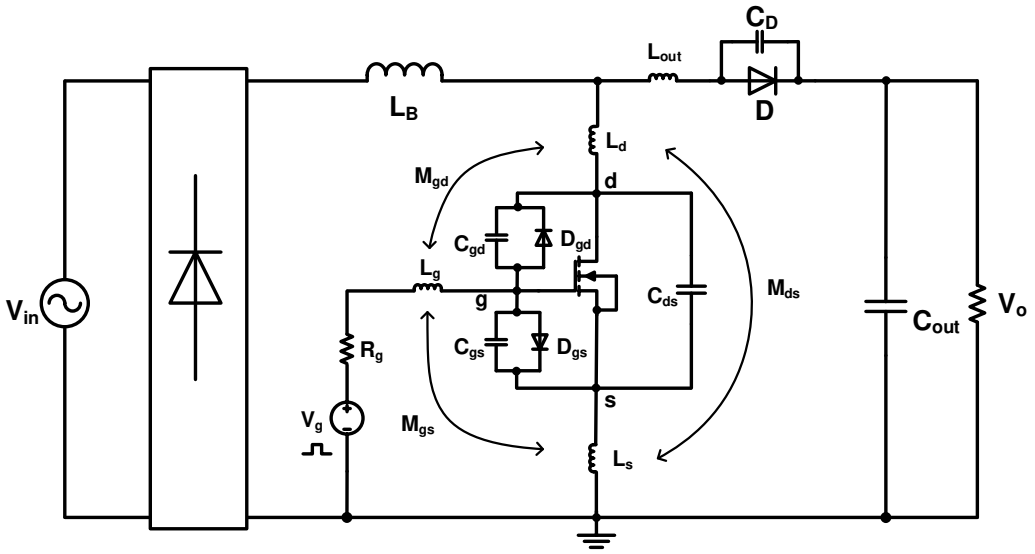


Figure 6.1 GaN based boost converter used as PFC preregulator

6.3 Design of a high frequency GaN GIT based PFC boost converter

Currently, boost converters with BCM-VS mode are commonly seen the PFC stage of low-to-medium power AC-DC power supplies like notebook adapters, LED drivers, etc., in which the maximum operation frequencies are generally limited to 500kHz due to excessive losses in Si transistors [6-1]- [6-3]. The lacking of suitable switching devices is therefore the major challenge for achieving high frequency and high efficiency at the same time [6-4]. The advent of GaN technology, as demonstrated in chapter 5, paves the way for high frequency operation of switching devices in BCMV-S at frequencies that are more than 7 times higher than Si transistors. To design and implement a high efficiency converter at frequencies greatly increased from 500kHz, however, demands more advanced technologies e.g. magnetics, controllers, etc., that are also suitable for high frequencies applications. Take high frequency magnetic materials as an example, very few ferrites that are suitable for >1MHz operations are commercialized and, with optional products like 3F4, 3F45, etc., availability of core shapes and dimensions are quite limited. In this chapter, the focus of which is to demonstrate the high frequency potentials and benefits of GaN technology in a real application, a PFC boost converter, with efficiency as the objective, is designed and built under these practical constrains.

Design guidelines of fixed-frequency CCM or DCM PFC boost converters have been extensively investigated and discussed in literature and, depending on the design objectives, optimization approaches are well-established [6-19]-[6-22]. Methodologies for design of a BCM-VS PFC boost converter, however, are limited to low frequencies and are not applicable for high frequencies as the effect of ringing-time and the presence of resonant current are neglected [6-1] [6-23]. In this work, a BCM-VS mode PFC boost converter with GaN GIT is designed with the goal to achieve high efficiency at high frequencies.

6.3.1 Design of a BCM-VS PFC boost converter

In BCM-VS, switching and/or conduction conditions of main components in a boost converter is determined mainly by the instant input and load conditions of a switching cycle while operation frequency of the switching cycle (and also, the frequency swing in a half-line cycle) can be designed by adjusting the boost inductor [6-4]. In this work, as indicated in Table 6-1, a 600W PFC boost converter with a maximum frequency of 3MHz will be designed under the considerations of demonstrating high frequency operation benefits of GaN technology and the concerns of practical implementation of the converter with currently available technologies:

- High-line input ($230V_{ac}$) is considered in the design stage as both situations of BCM-VS ($V_{out} > 2V_{in}$) and $V_{out} \leq 2V_{in}$) will be present in a half-line cycle. This is different from commonly taken practice of designing the PFC converter by considering low-line (high current) as the worst-case situation [6-1];

- A maximum frequency (f_{max}) of 3MHz was chosen as a result of the maximum operational frequency of commercialized magnetic material [6-24];
- Maximum power of the PFC boost converter (P_{max}) will be pushed up to 600W, which is a "grey area" for selecting operation mode of a PFC boost converter, to examine the possibly of overcoming the challenge with the adoption of the new semiconductor technology. Conventionally, apart from EMI problems, because of loss and electrical stress concerns, BCM-VS mode is generally used in low and medium power (P_{max}<300W) PFC boost converters while in the high-power ones (P_{max} >1kW), CCM mode is usually applied [6-1] [6-23] [6-25] [6-26].

Table 6-1 Converter Specification

Parameter	Symbol	Specification
Input Voltage	V_{in}	230V_{ac}, 50Hz
Output Voltage	V_o	400V
Maximum instant output power	P_{max}	600W
Maximum switching frequency	f_{max}	3MHz

Due to the fact that state-of-art BCM-VS controllers are all confined to an applicable frequency of 500kHz, operating of the GaN based PFC boost converter that is designed for MHz range through the entire half-line cycle is not possible. In this work, 6 working points, as illustrated in Table 6-2, that covers both situations of BCM-VS are selected. The approach is considered as an effective alternative for investigating high frequency PFC converter with GaN technology applied in that, implementing of closed-loop control, in essence, is selection of finite number of working points. And as long as all the possible working conditions of the converter are accounted for, the same pattern should present and so does the conclusions. Given the fact that both $V_{out}>2V_{in}$ and $V_{out} \leq 2V_{in}$ conditions are represented by 3 different working points, the approach taken therefore is a simplified version of closed-loop controlled BCM-VS PFC boost converter.

Determination of on-time and boost inductance

At a working point, may it either be the testing point selected in this work or a sampling point in a close-loop controlled half-line cycle, two basic relationships exists when the ringing time and resonant current are considered: duration of a switching cycle consists of on-time, off-time (T_{off}) and ringing time (T_r) as expressed in (6-16)~(6-18); input current is affected by not only the triangular-shaped inductor current (I_{tr}) but also negative current (I_n) brought about by the mode of BCM-VS as illustrated in (6-19)~(6-21). It should be noted that, when $V_{out}>2V_{in}$, negative current consists of two parts as illustrated in Figure 6.2: resonant current (I_{n1}) that occurs when voltage across GaN drops from V_{out} to zero and, after turn-on of GaN at zero voltage, linear current (I_{n2}) that flows through channel of GaN and boost inductor and back to input. In these equations, C_t

denotes total capacitance that is effectively paralleled at output of the transistor (sum of output capacitance of the device, parasitic capacitance of the freewheeling diode and external capacitance added). In low frequency PFC designs, the effects of ringing-time on switching cycle and the fact that the presence of resonant current affects power delivery are often neglected. As was discovered in chapter 5, existence of the ringing time and associated resonant current cannot be overlooked as, with the increase of operation frequency, the portion of ringing over switching cycle gets larger causing excessive loss in components and putting limits on achievable frequency of the converter.

$$\frac{1}{f_s} = T_{on} + T_{off} + T_r \tag{6.16}$$

$$T_{off} = \frac{V_{in}}{V_{out} - V_{out}} T_{on} \tag{6.17}$$

$$T_r = \begin{cases} \sqrt{L_b C_t}\ acos(\frac{V_{in}}{V_{in} - V_{out}}), & V_{out} > 2V_{in} \\ \pi\sqrt{L_b C_t}, & V_{out} \le 2V_{in} \end{cases} \tag{6.18}$$

$$I_{in} = I_{tr} - I_{n1} - I_{n2} \tag{6.19}$$

$$I_{tr} = \frac{V_{in}}{2L_b} \frac{V_{out}}{V_{out} - V_{in}} f_s T_{on}^2 \tag{6.20}$$

$$I_{n1} = \begin{cases} V_{out} f_s C_t, & V_{out} > 2V_{in} \\ 2(V_{out} - V_{in}) f_s C_t, & V_{out} \le 2V_{in} \end{cases} \tag{6.21}$$

$$I_{n2} = \begin{cases} \frac{V_o(2V_{out} - V_{in}) f_s C_t}{2V_{in}}, & V_{out} > 2V_{in} \\ 0, & V_{out} \le 2V_{in} \end{cases} \tag{6.22}$$

The unknowns in these equations are: inductance value to be decided, value of external capacitance and on-time in a switching cycle. These parameters are correlated as:

$$L_B(f_s, C_t) = \begin{cases} \frac{1}{\{f_s[\sqrt{C_t} aco\,s\left(\frac{V_{in}}{V_{in} - V_{out}}\right) + \sqrt{\frac{2I_{in}V_{out}}{V_{in}(V_{out} - V_{in}) f_s} + \frac{2V_{out}^2 C_t}{V_o(V_{out} - V_{in})}}]\}^2}, & V_{out} > 2V_{in} \\ \frac{1}{\{f_s[\pi\sqrt{C_t} + \sqrt{\frac{2I_{in}V_{out}}{V_{in}(V_{out} - V_{in}) f_s} + \frac{4V_{out}C_t}{V_{in}}}]\}^2}, & V_{out} \le 2V_{in} \end{cases} \tag{6.23}$$

$$T_{on}(f_s, C_t) = \begin{cases} \frac{V_{out} - V_{in}}{V_{out} f_s} - \frac{V_{out} - V_{in}}{V_{out}} \sqrt{L_b(f_s, C_t) C_t}\ acos(\frac{V_{in}}{V_{in} - V_{out}}), & V_{out} > 2V_{in} \\ \frac{V_{out} - V_{in}}{V_{out} f_s} - \frac{V_{out} - V_{in}}{V_{out}} \pi\sqrt{L_b(f_s, C_t) C_t}, & V_{out} \le 2V_{in} \end{cases} \tag{6.24}$$

In our design, the conventional practice of keeping on-time constant throughout the whole half-line cycle will be used to ease the design. With the design specifications considered, namely a frequency of 3MHz with 102.8V input, a current of 1.85A at 325V input, the operation frequency of the P_{max} , which is the minimum frequency in all the working points, can be found as 928kHz when external capacitor is not involved. Besides, A constant on-time of 183ns is maintained in all working points and an inductance of 14.6uH is needed.

Table 6-2 Parameters of working points without C_{ext}

P_o	V_{in}	f_{vs}	I_{in}
10%	102.8V	3.00MHz	0.00A
20%	145.3V	2.59MHz	0.21A
40%	205.6V	1,93MHz	0.84A
60%	251.7V	1.57MHz	1.17A
80%	290.7V	1.23MHz	1.47A
100%	325.3V	0.93MHz	1.85A

Loss calculation

With inductance and on-time determined, switching and conduction conditions e.g. current, switching frequency, etc. of the components at all the selected working points can be disclosed. Loss calculation of the converter can be performed once properties of the components are specified.

- *GaN transistor* is used as the switching device to enable high frequency operation of the converter. A 600V GaN GIT will be utilized since single-die, normally-off GaN HEMTs are subjected to low voltage (≤ 300V). Parameters of the device can be extracted from [6-27].
- *Inductor design* is subjected to issues that not only limits maximum frequency of the converter but also inhibits optimization of the component for lowest loss.
    - Availability of core shapes and sizes of materials suitable for high MHz operation are limited. Currently, the only market-available magnetic material suitable for beyond 1MHz operation is limited to 3F4. Core shape of this material is confined to planar EI and optional dimensions are limited (E58/11/38, E64/10/50, E22/6/16 associated I). In this work, the combination of 22mm/15.6mm/2.9mm I cores are used simply because alternative options results in either excessive loss because of the large volume or have very limited winding window. 8 core blocks are used to form a square shape with 2 blocks combined together at each side of the square. The designed core structure facilitates easy adjusting of airgap and permits greatly enlarged winding window;

- Because of the uniqueness of the decided core structure, experimental measurements were carried out to find the limitation of increasing length of airgap. In the measurements, a constant inductance of 14.6uH is maintained by scaling the square of number of terms with length of the airgap and it was found that when number of turns was increased beyond 15 turns (airgap ~1.7mm), the inductance will drop significantly. In design of inductor to be used in the PFC boost converter, this effect is considered as a limiting factor;
- Loss density of the core is confined to below 200kW/m^3. As was presented in [6-28], in a core-loss dominating inductor, maximum practical allowable power dissipation per unit volume of a core is limited and a conservative value are quantified as 200kW/m^3 to keep temperature of a magnetic core from overheating. The conservative value is used in this work;

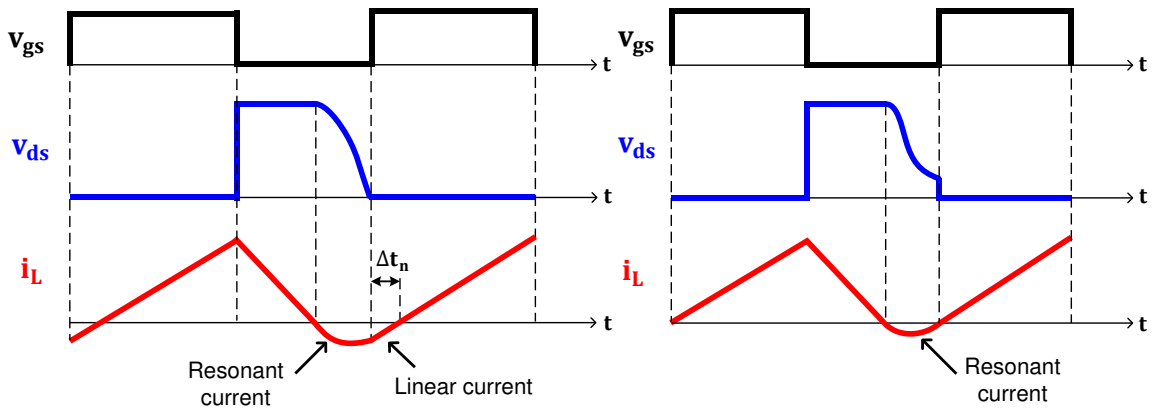
Under these practical constrains, the inductor parameters are summarized in Table 6-3. With the parameters specified and core loss parameters obtained from [6-24], core loss can be calculated.

Table 6-3 Design parameters of boost inductor

Parameter	Value	Parameter	Value
Inductance value	14.6uH	Max. no. of turns	14
Core cross section area	90.5 mm^2	Core volume	15920 mm^3

Freewheeling diode is chosen as a Si one that will generated lowest loss under the specified working conditions in Table 6-2. A freewheeling diode would generate conduction loss in the device itself and would also contribute to switching loss of the transistor. The latter effect is not considered in this part but the presence of parasitic capacitance of the diode is accounted for in predicting loss of GaN GIT. Of conduction loss in a high voltage Si diode, the forward voltage drop related part generally dominates. And thus, a market-available 600V Si diode with lowest forward voltage drop is selected, which has a forward voltage drop of 0.89V and a R_D of 0.022 Ω. Loss calculation of diode can then be carried out at each of the working points.

With switching and conduction conditions of each of the 6 working points determined and parameters of the components specified, loss in the PFC converter can be predicted. It should be noted that, in both of the two situations of BCM-VS, resonant current also contributes to inductor loss and, in case of $V_o>2V_{in}$, after ZVS turn-on is enabled to avoid transistor from conducting in reverse direction, the resulting negative current will flow through transistor channel and the boost inductor back to input, generating losses in GaN transistor and boost inductor.



a b

Figure 6.2 Loss contributing currents during idle time

a. When $V_{out}>2V_{in}$; When $V_{out} \leq 2V_{in}$

6.3.2 Optimization of a BCM-VS PFC boost converter

As was elaborated in chapter 5, the mode of BCM-VS permits loss minimization of a GaN transistor through paralleling of optimal external capacitance to the device. The addition of external capacitance will not only change switching and conduction currents in GaN, but also affects the currents in inductor and freewheeling diode as indicated in equations (6-.16)-(6.22). And thus, it is necessary to investigate loss variation of the PFC converter as a function of extra capacitance to minimize loss of the converter, which was built under practical constrains in terms of suitable controller and magnetic materials.

Considering the effect of ringing-time and resonant current, switching and conduction currents in key components can be expressed as functions of capacitance. Applying the expressions of these currents into the developed loss model of the PFC converter, in which parameters of components are specified in previous section, the effects of output capacitance on loss in the PFC converter can be found. To on-time constant in the switching cycles, which is the basis of the BCM-VS mode to make input current instantaneously proportional to input voltage and thus realizing PFC, when extra capacitance is involved, at least one of two design parameters (boost inductance and operation frequency) needs to be adapted. In this design, fixed on-time is achieved by increasing duration of a switching cycle in response to the enlargement in ringing-time and the linear negative time (Δt_n in Figure 6.2a) while boost inductance is kept intact. As illustrated in Figure 6.3, converter loss reduction is possible with the introduction of C_{ext} and, when a 85pF capacitor is utilized, a loss reduction of 13.4% is achieved and thus optimizing efficiency of the converter. It should be noted that, this gain was obtained not only because the introduction of external capacitance, but also because switching frequencies at all the working pointes are decreased.

Table 6-3 Parameters of working points with C_{ext} added

P_o	V_{in}	f_{vs}	I_{in}
10%	102.8V	2.80MHz	0.00A
20%	145.3V	2.43MHz	0.00A
40%	205.6V	1,80MHz	0.72A
60%	251.7V	1.48MHz	1.06A
80%	290.7V	1.17MHz	1.39A
100%	325.3V	0.89MHz	1.76A

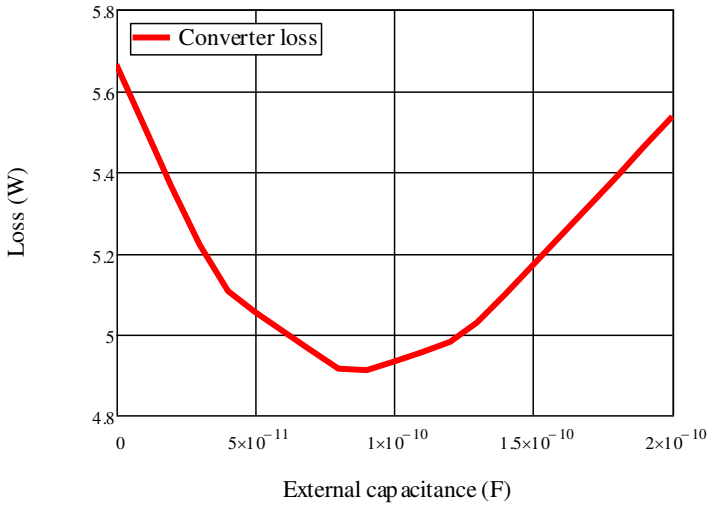


Figure 6.3 Effects of external capacitance on loss in PFC boost converter

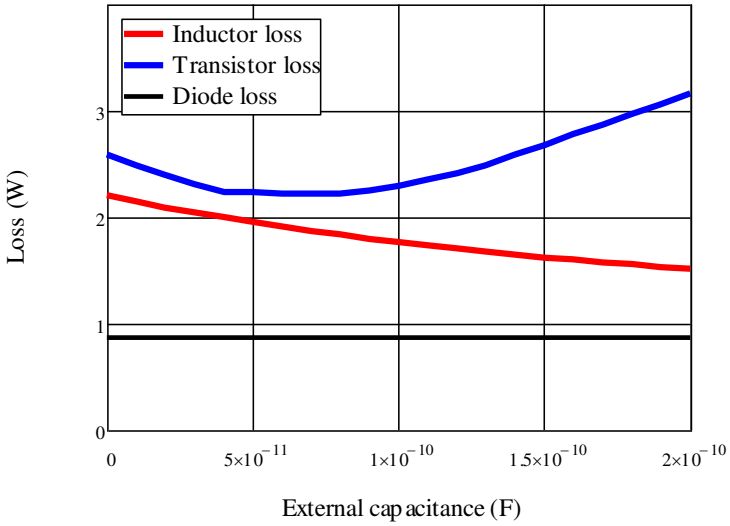


Figure 6.4 Effects of external capacitance on loss in key components

Introduction of additional capacitors for loss reduction of GaN transistor in the designed PFC boost converter, in which constant on-time is kept and switching cycles are varied as a

consequence of the added capacitance, would not only lead to loss reduction in GaN device but would also result in decreased loss in the boost inductor, mainly attribute to the lowering of switching frequencies. In the designed converter, a decrement of ~0.76W was achieved, which is, in fact, a net effect of loss variations in the components:

- In a BCM-VS PFC boost converter, because of the nature of constant-on scheme, frequency varies across a half-line cycle: high frequency operation occurs at working points with low current, and thus GaN transistor is switched-on with ZVS and switched-off with low or even zero channel current; low frequency switching happens at relatively high current level and, in this region, GaN is switched-on with ZCS and a valley voltage of $(2V_{in}-V_{out})$.

  In this specific design, ZVS turn-on is enabled at the 3MHz and 2.59MHz working points in which turn-off loss will also not be generated because, as analyzed in 5.2.1, channel current will not be present until turn-off current is beyond 2.2A due to the large ratio of C_{ds}/C_{gd} (~4.9 when voltage across the device is below 255V and up to 70 when voltage is higher than 255V). And therefore, switching loss at this two high frequency working points are zero. In fact, in the designed converter, existence of parasitic capacitance (~55pF) of the freewheeling diode, which is effectively in parallel with GaN, further increase the threshold current to ~2.6A. And therefore, when the converter operated with a input voltage of 205.6V, turn-off loss will also not exist in GaN GIT. Turn-off loss, however, will be generated in the rest 3 working points and, at the same time, turn-on loss also presents. And the higher the input voltage, the larger turn-off current and the valley voltage and, consequentially, so does the turn-on and turn-off energy. With the design approach taken in this work, on-time in all the working points is kept as independent of C_{ext}, maintaining the same peak inductor current (turn-off current). Addition of C_{ext} is beneficial for turn-off loss reductions in the working points with input voltage of 251.7V,290.7V and 325V, but would linearly enlarge turn-on loss. As a result, as illustrated in Figure 6.5, switching loss reduction can be only be achieved at testing point that is with 251.7V input and 290.7V input, respectively. In particular, when the converter operates at its maximum power (325V input), addition of extra capacitance will only induce more loss as the increment in turn-on and conduction loss overwhelm that of decrement of turn-off loss.

  With the developed loss model, loss reduction of ~0.36W can be obtained when a capacitor with a value of 85pF is paralleled to GaN GIT. The reduction, in fact, is a net effect of 0.89W increase in turn-on loss and 1.25W and 2mW decrease in turn-off loss and conduction loss, respectively. It should be pointed out that, with the designed converter that has a constant on-time and varied frequency to deal with introduction of

external capacitance, effective idle time in a switching cycle is enlarged and RMS current is lowered.

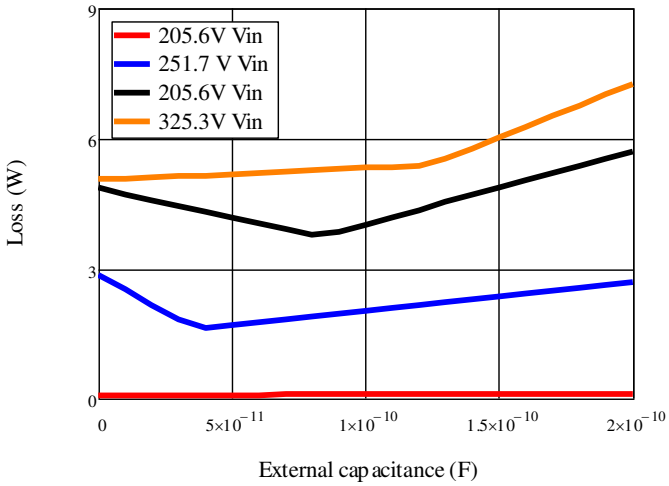


Figure 6.5 Effects of external capacitance on loss GaN GIT

(Switching loss at 102.8V and 145.3V input is zero)

- Due to the fact that, in a diode, forward voltage drop related loss dominates and the fact that in the designed PFC converter output current is independent of frequency and output capacitance, loss in the diode has negligible change with the introduction of extra capacitance. In fact, the resistance related loss drops about 2mW as a result of the reduced RMS current.

- In the mode of BCM-VS, loss in a boost inductor is generated by both positive current that flows to the transistor and output and negative current that is fed back to the input. As illustrated in Figure 6.2a, when $V_{out}>2V_{in}$, apart from the triangular-shaped current, a partial resonant current and a linear negative current will also flow through the inductor and generating loss in core and winding. Both duration of the resonance and that of the time period (Δt_n) that is needed to increase the inductor current from negative to zero, are directly related to the value of extra capacitance. Peak amplitude of the resonant current and the linear negative current, are also subjected to change of effective capacitance across GaN transistor. In case of $V_{out} \leq 2V_{in}$, amplitude and cycle of the resonant current associated with the mode will also be increased when more capacitance present. And thus, when output capacitance of the switching device is effectively enlarged, more loss will be induced by these two current, provided that switching frequency will not be decreased.

  In the designed converter, due to the maintaining of a constant-on time regardless of changes in capacitance and a predesigned inductor, peak values of positive currents, and also the resulted flux density in inductor core, will not be affected by the inclusion of

extra capacitance. Switching frequency, however, will effectively drop causing less core loss. Negative current induced loss are generated at the same frequency as the positive parts, but with increased flux density as peak value of the resonant current and the linear negative current get increased with the addition of external capacitors. Since in the designed converter core loss generated by the positive current dominates, loss in the boost inductor, is therefore decreased as winding loss, resulting from the reduced RMS current, will also drop. In the designed PFC converter, core loss drops by 0.39W while loss in winding also has a decrement of 2mW.

It should be noted that, as suggested in Figure 6.7 and Figure 6.8, negative current induced loss in ZVS BCM-VS operation points are higher than that in ZCS BCM-VS switching points because:

- In both ZCS and ZVS conditions, peak of resonant currents is determined as $(V_{out} - V_{in})\sqrt{\frac{C_t}{L_b}}$, and consequentially, in ZVS conditions, peak currents and also flux density in the inductor core are always higher than that in ZCS due to the large voltage ratio between output and input voltage as well as larger effective parasitic capacitance of the switching device. In case of a GaN GIT, output capacitance in low voltage range (<255V) can be 4 times as high as that in high voltage range. The resulting higher flux density may overwhelm the fact that in ZVS, core is subjected to less excitation as the resonant current happens in less than a half resonance cycle. Besides, idle time generally have higher ratio over a switching cycle, making negative current generated core loss higher in ZVS than in ZCS. In addition, the negative current (I_{neg}) that linearly returns to zero after turn-on of GaN GIT at ZVS will also be increased in both amplitude ($\sqrt{\frac{C_t V_{out}(2V_{out}-V_{in})}{L_b}}$) and time ($\frac{L_b I_{neg}}{V_{in}}$), resulting in more loss when capacitance is increased.

- In a PFC half line cycle, switching frequency in ZVS region is also much higher than the region where ZCS BCM-VS occur.

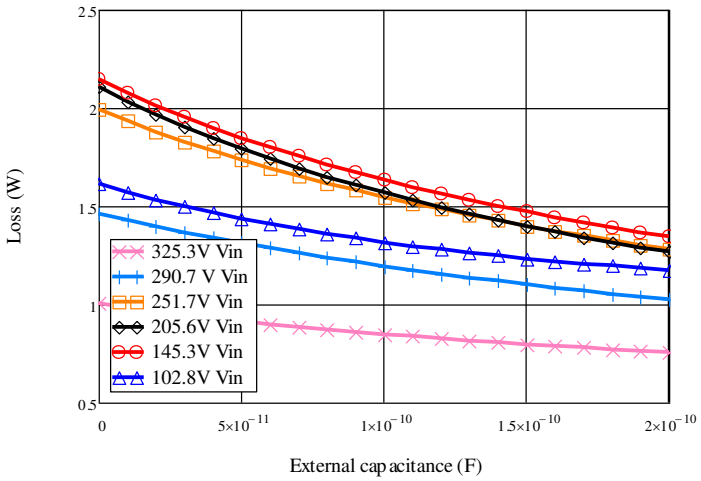


Figure 6.6 Effects of external capacitance on loss in inductor

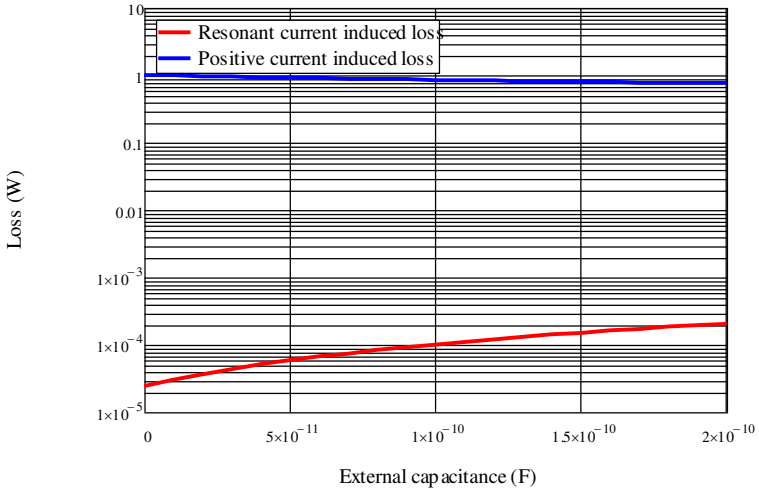


Figure 6.7 Inductor loss induced by different currents at 325.3V input

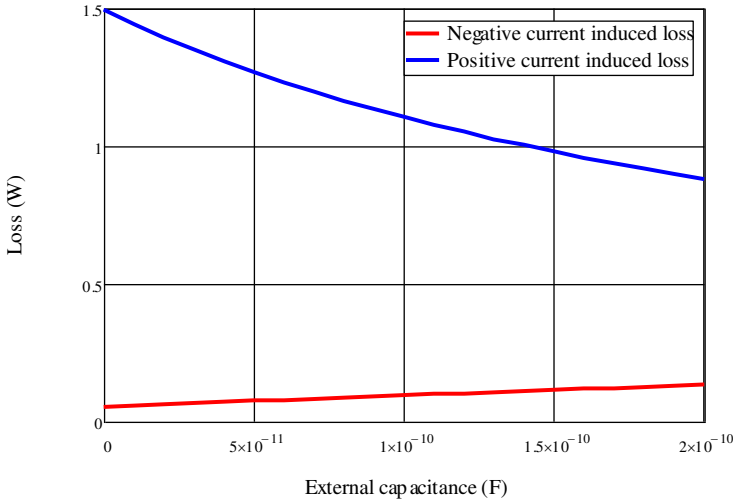


Figure 6.7 Inductor loss induced by different currents at 102.8V input

6.3.3 Summary

A PFC boost converter is essentially a boost converter operate with a finite set of parameters including switching frequency, voltage and current. When operated in the mode of BCM-VS, keeping transistor on-time as constant in the switching cycle across a half input line cycle is the basis of realizing the needed PFC. The nature of constant-on time, however, leads to varied switching frequency and, in a half-line cycle, the lower the input voltage, the higher the switching frequency. In traditional BCM-VS PFC boost converters, maximum frequencies are confined to a maximum switching frequency of 500kHz. The design methodologies of these converters are not suitable for high frequency design of a PFC boost converter that works in BCM-VS, due to the fact that the ringing-time and negative current that is brought about by the mode is not considered. As was discussed in chapter 5, at high frequencies, the effects of ringing time and associated current cannot be overlooked.

With the developed loss model for the key components in a PFC boost converter and the derivation of expressions of current and idle time in a switching cycle, loss modeling of a PFC boost converter with the ringing-time and the negative current being accounted for is achieved. Design of a PFC is then carried out with the developed model. Due to the lack of PFC controllers that can operate at MHz range, 6 discrete testing points are selected to resemble the operation of a controlled PFC. Design of the inductor is performed with practical constrains resulting from the limited availability of high frequency core materials as well as shape and dimensions. After the inclusion of properties of key components into the model, the PFC converter is optimized for highest efficiency in search of an optimal value of extra capacitance. The introduction of external capacitor, under the concept of constant-on time, will effectively decrease operation frequency of the converter and thus, loss reduction is net result of both switching loss reduction in GaN device but also loss decrease in inductor and diode. The designed PFC boost converter would achieve 13.4% loss reduction when an external capacitor with a value of 85pF is paralleled to GaN GIT.

6.4 Experimental demonstrator and results

A boost converter setup is built to demonstrate the design and analysis and, at the same time, to explore potentials of GaN technology in the application of PFC experimentally. In this section, the demonstrator is introduced, followed by analysis and discussion of the results.

6.4.1 A high frequency GaN PFC boost converter demonstrator

Following the design, a 600W boost converter, as shown in Figure 6.8, is built to approximate performance of a PFC converter with 6 discrete operating points that are specified with different voltage, current as well as switching frequency but the same on-time (183ns) and inductor (14.6uH). A 600V GaN GIT (PGA26C09DS) is utilized as the transistor and a 600V Si diode with

lowest forward voltage among market-available competitors (STTH8L06) is used as the freewheeling diode. As was introduced in 6.3.1, inductor design is subjected to practical constrains: using only 22mm/15.6mm/2.9mm I shaped cores made from 3F4, a unique square shape that consists of 8 I shaped-core blocks (2 blocks bonded together on each side) is made. The inductor winding utilizes litz wire with a specification of 130×0.071mm to avoid skin-effect without introducing excessive DC resistance. The winding has a number of turns of 14 to lower flux density in the core as much as possible while the inductance is maintained according to the experimental measurement results introduced in 6.3.1. With such a number of turns, maximum flux density in the 3F4 core is about 0.047T, which is well below the maximum allowable flux density of the material (0.35T). An external capacitor with a value of 82pF is added to achieve loss minimization.

As was analysed and proved in chapter 5, circuit parasitic inductances have limited effects on loss in GaN transistors even in hard switching conditions. In the mode of BCM-VS, as promoted in 5.3 and 5.5, the advantage of ZVS turn on (when $V_{out}>2V_{in}$) and ZCS turn-on (when $V_{out} \leq 2V_{in}$) further reduces the influence of circuit parasitic elements. Besides, turn-off loss will only be generated in the voltage rise stage when voltage is below 255V, which is also not affected by parasitic inductances. And thus, from loss reduction point of view, it is not necessary to perform minimization of parasitic inductances to its extreme values through approaches such as 3D design, resistive-switching design, etc. [6-30] [6-31]. Conventional PCB is therefore used as circuit carrier. To ease problems such as electrical stress in components, oscillatory energy that circulates in circuits, etc., attention was paid to reduce parasitic inductances on the PCB. The circuit parasitic elements are lumped with PEEC simulation and, merged with device package parasitic inductances of the GIT according to equivalent circuit of Figure 4.26 and Figure 4.27.

Table 9-4 Circuit and package parasitic inductances

Parameters	Values	Parameters	Values
L_d	3.13nH	L_s	3.08nH
L_{out}	8.20nH	L_g	2.72nH
M_{gd}	0.54nH	M_{ds}	0.54nH
M_{gs}	0.29nH		

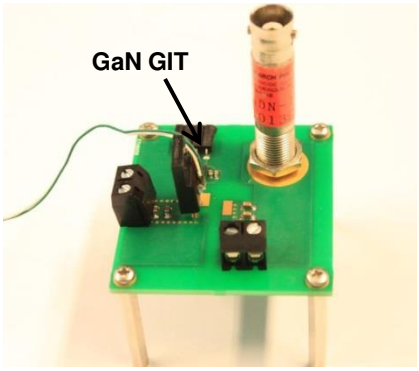


Figure 6.8 A 600W PFC boost converter prototype

6.4.2 Results

The converter setup was tested in the 6 working points as specified in Table 6-3. The measured efficiency of the converter agrees with the predictions of the developed loss model. There are, however, deviations between the measured and calculated values, which are mainly attributed to the overestimating of core loss in design stage, especially at high frequencies. Extraction of Steinmetz parameters at frequencies that are specified in datasheet of magnetic materials are easy to perform while determination of the parameters for operation frequencies at which loss data is not provided can be problematic due to the fact that, in core loss, dependence over frequency and flux density are nonlinear. In this work, Steinmetz parameters are extracted in a conservative way: a ceil function is used. For instance, in working points that have a frequency between 1MHz and 2MHz, the Steinmetz parameters at 2MHz are used. Apart from core loss, nonlinear capacitance of the GaN transistor could also contribute to the deviation. The higher the turn-on voltage, the smaller the error in estimating turn-on energy and resonance time and current, because at higher voltage levels, especially beyond 255V, output capacitance of GaN GIT can be considered as linear while, below 255V, output capacitance of the device varies dramatically.

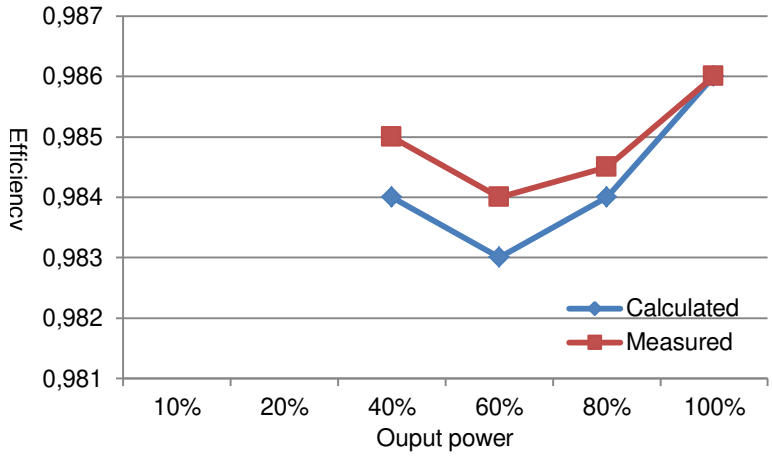


Figure 6.9 Efficiency curve of the PFC boost converter

The designed converter, in which the inductor is subjected to practical constrains and therefore not optimized, an average efficiency of 98.5% is obtained, indicating that GaN technology, when properly accommodated, have the capacity of facilitating high performance of power converters at frequencies that are beyond the reach of Si technology. It should be noted that, a turning point exists in the efficiency curve which mainly attribute to the greatly increased turn-on loss at 60% load point and 80% load, in comparison with that at 40% load as indicated in Figure 6.10.

Since the measurement results agree with the predictions with reasonable accuracy, loss breakdown of the converter is then performed employing the developed loss model to reveal loss distributions at different switching points. As illustrated in Figure 6.10, in high frequency range, loss in the boost inductor dominates and transistor loss is negligible while, at low frequencies, loss in GaN starts to dominate.

- In high frequency operation points (2.43MHz and 2.8MHz), switching loss in GaN will not be generated as the transistor is switched-on with ZVS and switched-off with zero channel current because of the large ratio between effective output capacitance and miller capacitance. On-state loss, due to the low on-state resistance of ~70mΩ, is negligible. Diode loss, in which the forward voltage drop induced loss overwhelms that of the resistance-related part, is small as output current is low. Inductor loss, as a result of high loss density of the material at high frequency, contributes to more than 89% at highest frequency and, at 2.43MHz, 87%, indicating that better magnetic materials are need at such frequency.

- In middle frequency range (1.17MHz, 1.48MH and 1.8MHz), transistor loss starts to appear, of which turn-off loss will not be present due to the aforementioned capacitance ratio. In fact, as demonstrated in Figure 6.5, the effectiveness of the added capacitance in terms of loss reduction is achieved in this frequency range, especially at 1.17MHz and 1.48MHz. Although, as already introduced in 6.3.2, turn-off at the 1.8MHz working point will not be present even without the involvement of external capacitor in this specific design. Even though turn-on loss in GaN is augmented linearly by the added capacitor, in this frequency range more gain is achieved in turn-off loss reduction. And therefore, it can be concluded, in middle frequency range, loss in GaN device is minimized. Loss in inductor increases with frequency, although peak flux density drops. Magnetic material with improved performance in this middle frequency range is necessary.

- In low frequency range (0.89MHz), transistor loss contributes to 68% of total loss as a result of the high turn-on loss, which is further worsened by the addition of extra capacitance, as illustrated in Figure 6.5. Inductor loss contributes to 14% of loss, suggesting that it is more suitable to work at a frequency range of below 1MHz.

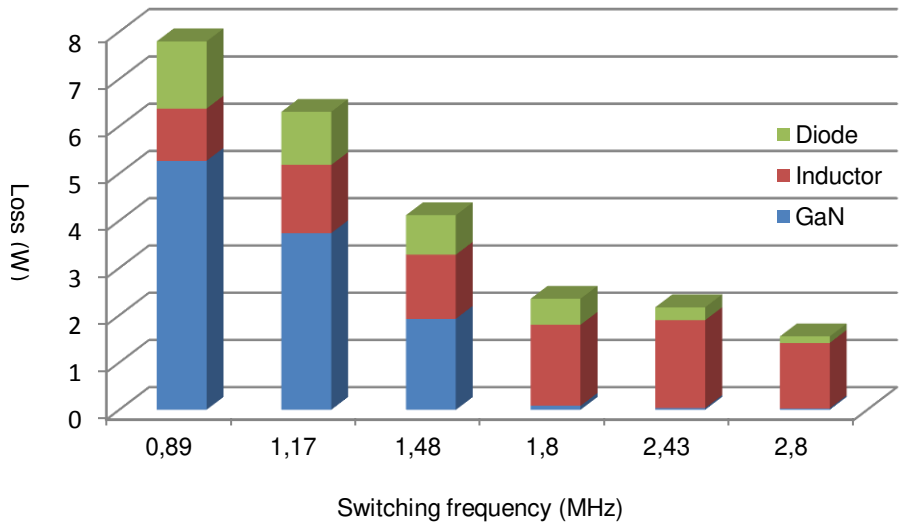


Figure 6.10 Loss distribution at different switching points

It can be concluded that:

- When properly used, GaN technology has the capacity of enabling high performance power converters at frequencies that are beyond the reach of Si technology. The designed BCM-VS PFC boost converter has a maximum operation frequency that is almost 6 times as the maximum achievable frequency of Si based ones (<500kHz) while efficiency is maintained as high as 98.5%;
- From loss point of view, PFC boost converter is an ideal application for GaN technology: across a half-line cycle, high frequency switching occurs when GaN is switched on with ZVS and switched-off with low or even zero channel current while ZCS turn-on, which is also accompanied by a voltage of ($2V_{in}$-V_{out}), and high channel current turn-off happens in low frequency region. And thus, a GaN device can be well accommodated.
- Better magnetic material suitable for operating at MHz is needed.

6.5 Summary

This chapter focuses on design and optimization of a GaN based high frequency application, using PFC converter as an example. As it was concluded in previous chapters that boost converter will remain as the most preferred choice for implementing PFC at high frequencies and that the mode of BCM-VS is perfect for accommodating GaN transistors, a GaN based PFC boost converter with the mode of BCM-VS is investigated. Analytical modeling of the whole converter is developed as a tool to perform design and optimization. Due to lack of suitable controllers, discrete points are selected in a quarter line-cycle to approximate a controlled PFC. Besides, as availability of magnetic materials capable of operating at MHz range are limited and, with the

limited options, core shapes and dimensions are subjected to few options, boost inductor is designed with practical constrains. Loss minimization of the designed converter is performed through search of optimal extra capacitance. A PFC boost converter prototype is built and tested to verify the design. The converter achieved an average efficiency of 98.5% even though the inductor is not optimized suggesting that, when properly-accommodated, GaN technology has the benefits of enabling high performance power converters at switching frequencies beyond the reach of Si technology. Moreover, PFC boost converter with the mode of BCM-VS, from the viewpoint of loss, is an ideal application for GaN technology. Both the design and the experimental results suggest that, at this stage, pushing up frequency of a converter is no longer limited by the lack of suitable switching devices. The limitations have shifted to practical issues e.g. high frequency controller, magnetic materials suitable for high frequency applications, etc.

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Chapter 7. Conclusions and recommendations

This thesis deals with exploration of high frequency operation potentials of GaN power semiconductors through device behavior modeling of GaN transistors to reveal high frequency limitations of the devices, accommodating the semiconductors accordingly with identified optimal topology and operation mode and demonstrating the high frequency capacities of the new technology in a real application.

The consistent demand on power electronics systems with improved performances cannot be fulfilled with the mature and well-established Si technology anymore. GaN power semiconductors, judging from the WBG nature of their material, have potentials of outperforming conventional Si counterparts in existing systems and facilitating new applications, and thus exploration of benefits and limitations of the technology is necessary (Chapter 1).

Performance of a GaN transistor is determined by more than just its material properties, practical issues from both the transistor itself and the electromagnetic environment it works in are critical for high frequency application of the device (Chapter 2). Comprehensive modeling of losses in GaN device with both device and circuit parasitic elements being accounted for is then performed as a tool to uncover capabilities and limitations of the transistor for operating in a range of few MHz (Chapter 4).

Because of the limitations of GaN transistors, direct adoptions of the new devices as substitutes of Si counterparts in power converters does not always bring about benefits in terms of loss reduction (Chapter 2). With in-depth knowledge on switching behaviours and loss characteristics of GaN devices obtained from loss analysis of the devices employing the developed loss model, desirable application conditions, under which high frequency operation benefits of the newly emerged technology can be maximized, is revealed (Chapter 5).

With the considered application of PFC, identification of optimal converter topology and operation mode that could facilitate the desired operation conditions simultaneously at high frequency is then conducted (Chapter 3 and Chapter 5). Furthermore, design trade-offs and limitations that arise when applying GaN devices in the identified converter topology and operation mode are addressed to achieve optimal utilization of GaN semiconductor and, in the end, to fully exploit the benefits of the new technology in the converter (Chapter 3 and Chapter 5).

Combining the knowledge on characteristics of GaN devices (Chapter 2 and Chapter 4) and the developed techniques for accommodating them at high operation frequencies (Chapter 3 and Chapter 5), a GaN based high frequency PFC converter is designed and implemented for the purpose of demonstrating high frequency operation potential of GaN technology in application of PFC (Chapter 6).

7.1 Conclusions

The key conclusions, which are drawn from work with single-die, normally-off GaN transistors in this thesis, are summarized as follows:

a). Loss limitation of high voltage, low current GaN power semiconductors for high frequency operation

Properties of GaN materials are superior to that of conventional Si making GaN power semiconductors, resulting in the promise of outperforming Si counterparts in high frequency applications. Performance of a device, however, is also greatly affected by practical issues such as die design and fabrication approach, device packaging technology, the way it is used in application, etc. And accordingly, challenges arise from both the device and its surrounding electromagnetic environment, inhibiting the GaN device from operating at high frequencies.

By means of characterizing switching and conduction behaviours of GaN transistors according to physical structures of devices and modelling of associated losses in GaN transistors analytically, full insights into the challenges are obtained. With the high voltage, low current GaN transistors:

- Turn-on loss can be more than 90% of loss in hard-switching, as a result of the large output capacitance (C_{oss}) that will get discharged though transistor channel;
- Turn-off loss will not be present in a GaN transistor when turn-off current is low thanks to the large C_{oss}/C_{gd} ratio that eliminates channel current; when turn-off current is high enough, turn-off loss will be generated;
- On-state conduction loss, resulting from low on-state resistance of the GaN transistor, is low;
- Reverse conduction loss is high due to the high voltage drop (1.3V~1.7V) demanded to initiate conducting of current in reverse direction;
- Package and circuit parasitic inductances have limited influence on loss in a GaN transistors, even in hard-switching conditions (less than 5%). Of all the parasitic inductive elements, common source inductance is the most critical one.

b). Optimal utilization of GaN technology at high frequencies

Since existing power electronics systems are designed mainly to suit Si devices, adopting of GaN transistors simply as drop-in replacements in these systems, which is the commonly used practice, may not lead to optimal usage of the new technology. In fact, direct substitution of Si devices with GaN counterparts may worsen performance of a converter in hard-switching and

even lead to failure of the device. To maximize the benefits of GaN technology in power electronics systems, optimal topologies and operation modes that could best accommodate parasitic elements of device and circuit parasitic are explored.

Exploration of topology

Investigation on the most suitable topology for implementing PFC stage in AC/DC converters was conducted by examining merits and demerits of possible topological options and performing qualitative comparisons, with GaN devices considered as switching devices and pushing-up operation as variable. It was concluded that boost converter will remain as the most preferred choice for implementing PFC with GaN devices as high frequency operation brought about by GaN technology hardly affects merits and demerits of optional topologies.

Identification of operation mode

By examining switching and conduction conditions of transistors enabled by different operation modes in a PFC boost converter, optimal operation mode was identified. It was exposed that the mode of Boundary Conduction Mode with Valley Switching (BCM-VS) could facilitate all the desirable switching conditions of GaN transistors simultaneously when turn-off switching current is low, and thus is ideal for high frequency application of the devices in low current conditions.

Optimal utilization and design trade-offs of GaN technology in BCM-VS mode

Application of a GaN transistor in a BCM-VS boost converter would initiate new limitations and design trade-offs. With proper measures being taken to deal with these challenges, both switching and condition loss in the GaN device can be minimized, leading to optimal utilization of GaN devices in a boost converter with BCM-VS mode.

- Higher voltage stress will be induced and when current is high, excessive turn-off loss will be generated. It was proposed that, adding of external capacitors to GaN devices could ease voltage stress and reduce turn-off loss. The addition of capacitors, in fact, will increase turn-on loss, especially when $V_{out} < 2V_{in}$ (ZCS BCM-VS). And thus, a trade-off on the selection of proper external capacitor value exists between switching loss and overvoltage;
- In case of $V_{out} > 2V_{in}$, reverse conduction will occur, inducing high conduction loss. It was discovered that by switching-on GaN device before current returns to zero, especially at the zero-voltage point (ZVS BCM-VS), the total conduction loss (sum of on-state RMS loss and reverse conduction loss) can be minimized.

Boundaries and limitations of the utilization approach

The introduced operation mode and associated actions to achieve optimal utilization of GaN technology are subjected to boundaries and limitations beyond which the approach ceases to be beneficial:

- The proposed BCM-VS boost converter inherently introduces a ringing-time and, with increase of frequency, the ratio between the ringing-time and a switching cycle gets enlarged, resulting in increased switching and conduction currents in components. The current increments limits the maximum achievable frequency of the converter to a range of hundreds of kHz and affects design or selection of components;
- The practice of adding external capacitance to achieve loss minimization would effectively increase the ringing-time in a switching cycle and, consequentially, currents in the converter. With the paralleling of external capacitors, maximum operation frequency of BCM-VS is limited by switching loss in ZCS BCMV-VS while, in ZVS BCM-VS, by conduction loss.

c). High frequency power converter with GaN technology applied

The BCM-VS boost converter designed for application of PFC demonstrates high frequency operation potentials of GaN technology. When applying GaN in real applications:

- PFC is a perfect application for maximizing the benefits out of GaN technology with the developed technique in this thesis because, across a half-line cycle, high frequency working region is accompanied by ZVS turn-on and low or even zero channel current turn-off while ZCS with valley voltage turn-on and high channel current turn-off happens in low frequency region;
- Pushing frequency of a power converter up is, at this stage, limited by practical issues such as design of high frequency magnetic components, implementation of high frequency controller, etc., not by the lack of suitable switching devices anymore with advent of GaN technology.

7.2 Thesis contributions

The main contributions this thesis make to the engineering science can be summarized as:

1). Development of a novel and generalized analytical loss model for single-die, normally-off GaN transistors

The developed model in this thesis is a comprehensive one in that it includes all the critical parasitic elements from both device and circuit. The model is valid for two different

types of single-die, normally-off GaN transistors and can be applied in all diode-clamped, inductive load switching circuits.

2). Introduction of desirable operation conditions for high voltage, low current GaN devices for high frequency applications

Effects of all critical parasitic elements originate from both GaN device and circuit carrier are investigated thoroughly. Desirable switching and conduction conditions of high voltage, low current GaN devices are disclosed accordingly.

3). Identification of the most preferred topology and optimal operation mode for PFC with GaN technology applied

Boost converter is proved as the most preferred topology for implementing PFC at high frequencies and BCM-VS is introduced as an ideal mode for accommodating GaN devices.

4). Introduction of design trade-offs and clarification of boundaries and limitations of the BCM-VS boost converter

New design trade-offs initiated in applying GaN in the mode of BCM-VS are introduced and approaches to deal the trade-offs are proposed. Boundary and limitations, in terms of frequency, of both the mode of BCM-VS and the proposed approaches are clarified.

7.3 Recommendations for future research

In this thesis, attention was mainly paid to investigating and demonstrating how to best accommodate GaN power semiconductors in high frequency power electronics converters. To take full advantage of the new technology at converter and system levels, the following are recommended topics for future research:

i). To investigate optimal operation frequency for maximizing efficiency of a GaN boost converter in BCM-VS

As goal of this thesis is to explore high frequency potentials of GaN technology, operation frequency of a GaN boost converter in BCM-VS is pushed as high as possible with available technologies while efficiency of the converter is kept reasonably high. Optimization of a GaN converter for highest efficiency, in which the whole power stage rather than only the switching device is considered, should be investigated.

Optimum switching frequencies, at which efficiency of a BCM-VS boost converter reaches its peak value, exist. Increase switching frequency of a BCM-VS boost converter would cause higher loss in transistor and freewheeling diode. Inductor loss, as discussed in chapter 5, decreases over frequency firstly and then the trend reverse. And therefore, from loss point of view, there may exist a cross-point between loss increase in transistor and diode and loss reduction in inductor when frequency varies. It is necessary to identify the cross-point for most efficient power conversion of a GaN converter.

ii). To investigate system-level optimization and packaging of a high power density GaN converter

To really harvest benefits of GaN technology in power electronics systems, system level optimization and packaging is needed. High frequency operation capacity of GaN devices not only results directly in loss reduction in the semiconductors, which is beneficial for size and volume reduction or even elimination of heatsinks, but also indirectly brings the possibility of size reduction of passive components. As was uncovered in chapter 5, size of heatsink and inductor scales with frequency-dependent loss in transistor and inductor, respectively. And therefore, a systematically investigation on converter loss, passive component and thermal management with variation of frequency is necessary to achieve high power density. In particular, when frequency is high enough, embedding passives into circuit carriers is possible and system-level packaging of the resulted converter e.g. technology platforms for achieving highly integrated converters, thermal management techniques for the whole converter (both and active parts), etc. is called for.

iii). To investigate design of high frequency BCM-VS controllers

Conventional BCM-VS controllers, which are designed to suit Si technology, neglects the effects of ringing-time and the resonant current, and thus is not suitable for high frequency. To assist successful usage of GaN devices in high frequency PFC applications, design of BCM-VS controllers that could operate at frequencies beyond the reach of conventional ones is a must.

Appendix A. Loss model validation

A.1 Approach

Loss model validation is conducted by comparing modelled loss values with measured ones to check whether the former can approximate the latter with satisfactory accuracy. Losses is calculated by applying electric parameters and specifications of the setups, in which the transistors are tested, to the developed loss model. Electric parameters of the components such as threshold voltage, parasitic inductances, on-state resistance, etc. are extracted from device datasheets while parameters like parasitic inductances of both device package and circuit carrier, loss-relevant parasitic capacitance caused by heatsinks and circuit carrier, etc. are obtained by PEEC (Partial Element Equivalent Circuit) calculation tool [A-1].

So far, two different kinds of electric loss measurement techniques have been used to quantify losses in GaN transistors: in [A-2], loss in a GaN HEMT was measured through waveforms of voltage across the device and current flowing through it in a Double Pulse Tester (DPT) and in [A-3], loss values of a GaN HEMT was obtained by the measurements on efficiency and power of a buck converter and subtracting losses in the rest components in the converter. The former approach is very sensitive to phase discrepancy between the measured current and voltage, especially at high frequencies. The causes of phase discrepancy, such as poor frequency response characteristics of current/voltage sensing devices, mismatch between probes, delays in oscilloscope channels, are inevitable in the measurements [A-4]. Besides, as indicated in the developed model, measured current and voltage are not necessarily the actual values in the transistor. And therefore, accuracy of the approach is not always satisfactory. The latter approach, on the other hand, requires precise estimation of loss in the rest parts of the converter e.g. diode, inductor, etc. Moreover, in a well-designed GaN converter, where efficiency is high, subtraction of two nearly equal numbers would introduce considerable error [A-4]. As a result, accurateness of the results from this approach may not always be sufficient.

Calorimetric methods can be used to determine power because power loss in a device dissipates as heat and heat results in a temperature rise of the device. In power electronics, calorimetric method have already been used to measure loss of electric and magnetic components using either simple or complex setups, but have not been applied for quantify loss in GaN transistors [A-4] [A-5]. Results from calorimetric measurements are trustworthy once the relationship between loss and associated temperature in a device are well calibrated and the effects of the environment on temperature of the device are properly accounted for. In a boost converter setup, apart from losses in transistors, losses in boost inductor, freewheeling diode and gate driver could also influence temperate of the transistor. The effects, however, can be excluded when proper

measures are taken: a) the effects of boost inductor and freewheeling diode on transistor temperature may be excluded by proper layout; b) effect of driver on transistor temperature can be omitted if loss in the driver is negligible small. As a result, transistor temperature increase is caused only by loss in the device. With the help of a calibrated relationship between loss and temperature increase in GaN transistors, loss quantification can be achieved.

A.2 Setups

Two boost converter setups are built for loss validation of GaN HEMT and GaN GIT, respectively.

GaN HEMT based boost converter, as demonstrated in Figure A.1, was built with a 200V single-die GaN HEMT (EPC2010). In this setup, 5 single-layer inductors are connected in series to provide the needed inductance and minimize parasitic capacitance at the same time. A 600V SiC Schottky diode (C3D02060E) is used as the freewheeling diode. The GaN HEMT used has an absolute maximum gate voltage (V_{gmax}) of 6V and a gate-channel diode built-in voltage of ~5V. The transistor is driven by a 0V/3V pulse train to avoid exceeding of V_{gmax} caused by oscillation in gate loop. Consequentially, gate-channel diode will not conduct and conductivity modulation will not occur, and, given the low driving voltage and the small amount of charge (less than 3nC) needed to turn the transistor fully-on, loss in driver is negligible and so does its influence on transistor temperature. By activating only the gate loop and observing temperature of the transistor, the possibility of neglecting influence of gate driver was also verified experimentally. Boost inductor and freewheeling diode were placed physically away from the transistor, at the expense of increasing values of connection parasitic inductances. The converter is designed to operate with a maximum output power of 150W. Experimental verification were performed by injecting triangular and DC currents (both beyond the maximum required corresponding values when the converter operates at 150W) into the boost inductors and freewheeling diode while keeping GaN HEMT in off-state, respectively and monitoring temperature variations of the transistor. It was confirmed that boost inductors and freewheeling diodes also have no contribution to temperature of GaN HEMT in the setup.

A lookup table on loss in GaN HEMT and consequential temperature increases was made by injecting DC currents from 1A, with an increment of 0.5A, to 7A into the device when it is kept in on-state (3V DC V_{gs}) i.e. generating known power loss and recording corresponding temperature increases. Variation of on-state resistance of GaN HEMT with temperature is also accounted for to improve accuracy of the table.

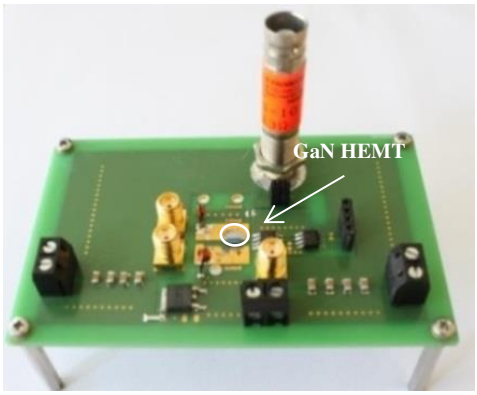

Figure A.1 GaN HEMT based boost converter

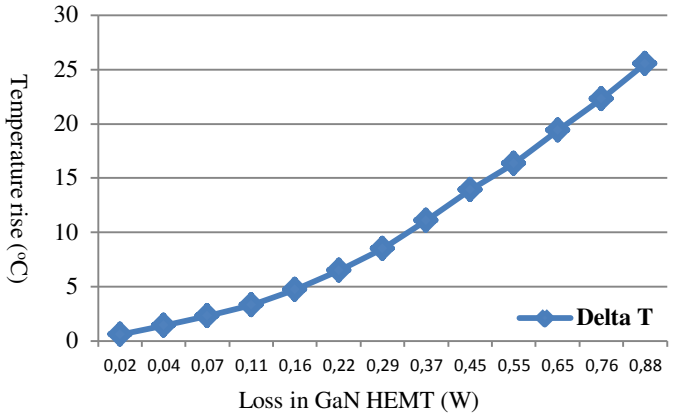

Figure A.2 Relationship between loss and temperature increase in GaN HEMT

GaN GIT based setup, as shown in Figure A.3, utilizes a 600V GaN GIT (PGA26C09DS) and, to minimize parasitic capacitance of the boost inductor, 4 single-layer inductors are connected in series to fulfill inductance requirement. Besides, a 600V, 7.5A SiC Schottky diode (C3D04060A) is utilized as the freewheeling diode. The V_{gmax} of GaN GIT is 4.5V and, to keep the gate-source voltage below maximum rating, the transistor is driven by a 0V/4V pulse train. This converter was designed to operate with a maximum power of 300W, and, similar to the approach taken for GaN HEMT based setup, experimental validation on the effects of boost inductors and freewheeling diode, which were arranged physically away from GIT, was performed and the results showed that they hardly have any effects on temperature of the transistor. On the other hand, loss in gate driver and potential effect on temperature of GIT is also neglected as the device requires only 8 nC to be fully-on. The gate-source diode in GIT, however, will conduct as build-in voltage of the device is about 3.5V and generating loss in GaN GIT itself. This effect can be taken care of by keeping the driving power on until temperature of GIT is stable (as initial state) before the main power is initiated. By keeping the GaN GIT in on-state (4V DC V_{gs}) and injecting DC current from 1A, with an increment of 0.5A, to 8A and observing the following temperature increase, a lookup table in Figure A.4 is obtained. It should be noted that, the lookup table for GaN GIT was made

when a heatsink (27/27/10) is attached to the device, which is not presented in the converter setup shown below.

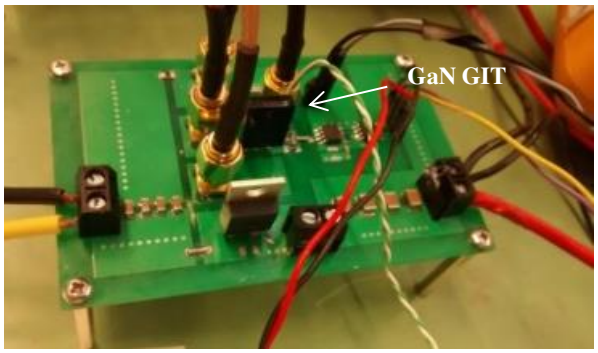

Figure A.3 Converter employing high voltage GaN GIT

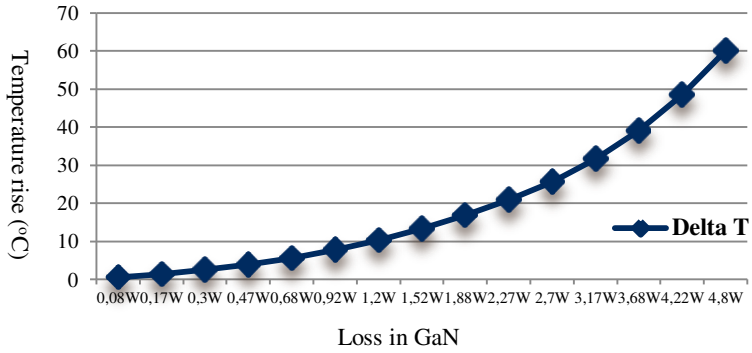

Figure A.4 Thermal lookup table of GaN GIT

A.3 Results

To verify the effectiveness of the developed loss model in GaN HEMT, the device is tested at 6 different operation points (of which the parameters are listed in Table A.1) in a boost converter in CCM (Continuous Conduction Mode) at 100kHz, and the associated losses are quantified using the lookup table in Figure A.2. Losses in GaN HEMT are calculated through the developed loss model in the test points with the extracted parameters from devices and circuit (specified in Table A.2). During voltage fall stage in turn-on and voltage rise stage in turn-off, two different substages are used for the calculation according to capacitance variation values in different voltage ranges (0~25V, 25V~150V). In each substage, average value of capacitance is used. Capacitance values of $C_{gd(v_{out})}$, $C_{ds(v_{out})}$ and amount of charge ($Q_{v_{out}}$) required to enable the freewheeling diode to block output voltage are obtained from datasheet of the device, in light of the exact output voltage of one test point. As indicated in Figure 4.38, the modelled loss agreed well with measurement results. It should be noted that the measured loss value in GaN HEMT at 150W was extrapolated using the lookup table.

Table A.1 Test points in a GaN HEMT based boost converter

P_{out}(W)	v_{out}(V)	I_{on}(A)	I_{off}(A)
25	61.5	1.06	1.4
50	87	1.52	1.96
75	106	1.88	2.36
100	122.5	2.16	2.72
125	137	2.4	3.12
150	150	2.64	3.36

Table A.2 Values of parameters in converter with GaN HEMT

Parameters	Values	Parameters	Values
V_{th}	1.4V	C_{gs}	480pF
g_{fs}	12	L_d	3.44nH
R_{dson}	25 mΩ	L_s	2.74nH
$C_{gd(R_{dson}I_{off})}$	90pF	L_D	16.1nH
$C_{gd(R_{dson}I_{off})}$	950pF	L_g	1.55nH
$C_{gd(25V)}$	20pF	$C_{ds(25V)}$	500pF

GaN GIT was tested at 7 different operation points in the boost converter in CCM at 100kHz and the associated losses are quantified using the lookup table in Figure A.4. Calculation of losses in GaN GIT in the test points (specified in Table A.4) are performed with the parameters obtained from both device and the circuit (values listed in Table A.3). As indicated from datasheet of GIT, values of $\mathrm{C_{gd}}$ and $\mathrm{C_{ds}}$ are almost constant when v_{ds} is greater than 255 V. Below 255 V, however, both capacitances values vary with v_{ds} , and $\mathrm{C_{gd}}$ varies dramatically. And therefore, the voltage fall stage in turn-on is divided into two substages and so does the voltage rise stage in turn-off. Capacitance values of $\mathrm{C_{gd(v_{out})}}$, $\mathrm{C_{ds(v_{out})}}$ and needed charge ($\mathrm{Q_{v_{out}}}$) of the freewheeling diode, are taken from datasheet of either the transistor or the diode, in accordance with the exact output voltage of one test point. The developed model predicts losses in GaN GIT with a reasonable accuracy, as illustrated in Figure 4.39.

Table A.3 Values of parameters in converter with GaN GIT

Parameters	Values	Parameters	Values
V_{th}	1.2V	L_d	3.13nH
g_{fs}	26	L_s	3.78nH
R_{dson}	71 mΩ	L_D	9.87nH
C_{gd1}	1.1pF	L_g	4.45nH

C_{ds1}	70pF	M_{gd}	0.54nH
C_{gd2}	22.1pF	M_{ds}	0.54nH
C_{ds2}	145pF	M_{gs}	0.29nH
C_{gs}	270pF		

Table A.4 Specifications of test points in CCM boost converter using GIT

P_{out}(W)	v_{out}(V)	I_{on}(A)	I_{off}(A)
20	100	0.35	0.44
45	150	0.51	0.65
75	200	0.70	0.88
120	250	0.87	1.09
170	300	1.04	1.31
230	350	1.20	1.52
300	400	1.40	1.70

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Summary

Electromagnetic design of high frequency PFC boost converters using Gallium Nitride devices

Ph.D dissertation

by Wenbo Wang

Throughout the history of power electronics, main driving force of developments is attribute to innovations in power semiconductor technology. With continuous technical improvements in the past 30 years, Si devices, being the most widely used power semiconductor technology, are approaching physical limits e.g. breakdown field, thermal conductivity, etc. of the basic material. Performances of power converters such as efficiency, power density, etc., therefore, has entered into a stage that further improvements are not likely to happen without revolutionary advance in power semiconductor technology.

GaN power semiconductor devices, judging from the wide bandgap nature of its material, have the potential of outperforming conventional Si counterparts in measures of high voltage, high temperature and high frequency operations. Capabilities of a GaN device, however, is influenced by more issues, which, apart from material properties, also include die design and fabrication approaches, device packaging technologies, how they are used in an application, etc. In fact, at this stage, available GaN transistors are mostly of lateral structure and, as a consequence, confined to low voltage ones (<1kW) while maximum junction temperature of these products is limited to 175 °C because of the lack of suitable packaging technologies. So far, high frequency operation performance of GaN power semiconductors is unknown and needs to be investigated.

This thesis explores high frequency operation potentials of single-die, normally-off GaN power semiconductors that are suited for high voltage, low current applications. The exploration is carried out by means of conducting loss modeling of GaN transistors, uncovering desirable operation conditions of GaN devices for high frequency operations according to analysed results from the model, identifying optimal topologies and operation modes in power converters that can facilitate such conditions for GaN to achieve optimal utilization of the new technology and demonstrating potentials of GaN power semiconductors in an application with all the developed techniques employed.

Loss modeling of GaN transistors

Loss modelling of single-die, normally-off GaN transistors is conducted analytically as a tool to assist the exploration. Losses in a GaN transistor is subjected not only to parasitic elements of the device itself, may it be die-related or package-related, but also the specific electromagnetic environment the device operates in. In particular, with the newly introduced chip-scale GaN transistors, electromagnetic volume of the transistor is negligibly small in comparison to the rest parts of a power converter and circuit parameters have profound influence on losses of the devices. A comprehensive loss model that takes all the relevant parasitic elements from both GaN device and circuit carrier is therefore developed considering behaviours and associated loss during switching and conduction of the transistors.

Desirable operation conditions of GaN for high frequency operations

Employing the developed model, loss analysis of GaN devices is performed. Influences of device and circuit parasitic elements are thoroughly studied, with the critical parasitic elements that are most contributing in loss generation of a GaN device, especially in high frequency operations, identified. Desirable switching and conduction conditions of GaN transistors for high frequency operations, under which the critical parasitic elements can be best accommodated, are then disclosed.

It was revealed that turn-on loss could contribute to more than 90% of loss in a GaN transistor in hard switching due to the large output capacitance of the device while turn-off loss will not be present until switching current is high enough (at least beyond 2.2A) thanks to the large ratio between output capacitance and miller capacitance. Besides, resulting from low on-state resistance, conduction loss in a GaN transistor is low. It was also concluded that circuit and package parasitic inductances has limited effects on switching loss in a GaN transistor, even in hard switching conditions (<5%). Low voltage, low current turn-on, low channel current turn-off are therefore desirable switching conditions of a GaN transistor for high frequency operation.

Topologies and operation modes for accommodating GaN devices at high frequency

With the knowledge on needed operation conditions to accommodate GaN devices for operating at elevated switching frequencies, exploration of topologies and operation modes that could permit such conditions is then performed, using the application of PFC as a platform. Topologies that are possible for implementing PFC are reviewed firstly with advantages and disadvantages of each topology identified. A qualitative analysis is then conducted to assess properties of these topologies when their operation frequencies are scaled up equally. It was found that boost converter, the most widely used Si technology based PFC topology, will remain as the most preferred choice when frequency of the PFC stage is pushed up as the increment in frequency hardly has any effects on merits and demerits of the topologies. Operation modes of a boost converter are then examined, the attention of which is paid to inspect switching and conduction conditions a mode enables for transistor. It was promoted that Boundary Conduction Mode with

Valley Switching (BCM-VS) is an ideal operation mode for GaN devices as all the desired conditions can be facilitated by this very mode. Besides, the mode of BCM-VS also permits other benefits which are not possible in CCM or even BCM e.g. elimination of reverse recovery effect of the freewheeling diode on loss in transistor, the exclusion of influence of parasitic inductances on turn-on loss, the possibility of paralleling external capacitors to reduce overvoltage, etc.

Optimal utilization of GaN at high frequency

Considering the fact that all the existing topologies and operation modes are mostly designed to suit Si devices, a thorough investigation on challenges and design trade-offs when applying GaN in a boost converter with BCM-VS is performed. The mode of BCM-VS, in comparison with other modes, would result in higher turn-off current that leads to higher voltage stress and, when the current is high enough, more turn-off loss. It was proposed that paralleling of external capacitors to a GaN transistor is helpful for mitigating both and, when optimal value of capacitance is added, loss in the GaN device can be minimized. Besides, in case of $V_{out} > 2V_{in}$, reverse conduction of a GaN transistor will be initiated causing high conduction loss as forward voltage drop of the transistor when conducting current in reverse direction is high (1.3V~1.7V). Turn-on of GaN transistors before reverse conduction occurs, especially at the zero voltage point (ZVS) is proved as beneficial for overall loss reduction.

To guide proper design of a GaN boost converter in BCM-VS, boundaries and limitations, in measures of switching frequency, of the mode are clarified. It was found that he ratio of dead time, which naturally comes with the mode, over a switching cycle will be enlarged with the increase of frequency, causing increases in currents in the converter and putting limits to maximum achievable frequency of the converter and affects components design and selections. The mode of BCM-VS generally enables higher operation of a boost converter than any other modes when GaN devices are applied and maximum achievable frequency of a GaN based boost converter with BCM-VS is limited by switching loss when $V_{out} \leq 2V_{in}$ and on-state conduction loss when $V_{out} > 2V_{in}$.

Demonstration of high frequency operation potentials of GaN technology

High frequency operation potentials of GaN devices, which are proved as really living up to promises of its material properties when the devices are properly used, is demonstrated in a PFC boost converter aiming for high frequency and high efficiency. Due to practical limitations of unavailability of PFC controllers and lack of suitable magnetic materials, and so does core shapes and dimensions, for MHz operations. A GaN based PFC boost converter with the mode of BCM-VS is designed. Loss minimization of the converter is achieved through the search of optimal value of extra capacitance with the help of a developed loss model of the whole PFC boost converter. Experimental demonstrator is implemented following the design. It was shown

that, even when the magnetic components is not optimized due to practical constrains, the 3MHz PFC boost converter which has a peak power of 600W reached an average efficiency of 98.5%, indicating that: a) GaN devices have the capacity of enabling high performance power converters at increased switching frequencies when the devices are well accommodated; b) PFC boost converter with BCM-VS is an ideal application of GaN transistors as the devices can be best accommodated in the application; c) pushing frequency of a power converter up is, at this stage, no longer limited by lack of switching devices but other practical issues e.g. controller design, magnetics, etc.

Samenvatting

Elektromagnetisch ontwerp van PFC boost converters op hoge frequentie met gebruikmaking van Gallium Nitride componenten

Academisch Proefschrift

door Wenbo Wang

Door de hele geschiedenis van vermogenselectronica heen is de stuwende kracht toegeschreven aan de technologie van vermogens halfgeleiders. Ondanks de doorgaande technische verbeteringen over de laatste 30 jaar naderen de op Silicium gebaseerde componenten, die de meest wijd verbreide technologie voor vermogenshalfgeleiders is, de natuurkundige grenzen (zoals doorslagveldsterkte, warmtegeleiding enz.) van het uitgangsmateriaal. Kwaliteiten van vermogensomzetters zoals efficiëntie, vermogensdichtheid enz. hebben dientengevolge een stadium bereikt waarin het niet waarschijnlijk is dat verder verbeteringen gerealiseerd kunnen worden zonder een revolutionaire vooruitgang in de technologie van vermogenshalfgeleiders.

Op GaN gebaseerde vermogenshalfgeleiders hebben - uitgaande van de grote bandgap van dit materiaal - het potentieel om hen conventionele, op Si gebaseerde tegenhangers te verslaan op zaken als hoge spanning, hoge temperatuur en hoogfrequent gebruik. De mogelijkheden van GaN componenten worden echter beïnvloed door meer aspecten, die, naast de eigenschappen van het materiaal, ook behelzen het ontwerp van de chip en het fabricageproces, omhullingstechnologie, hoe ze in de schakeling gebruikt worden, enz.. Feit is dat, in het huidige stadium, beschikbare GaN transistoren meestal een laterale structuur hebben en dientengevolge beperkt zijn tot lage spanningen (<1kV), waarbij de maximale junctietemperatuur beperkt is tot 175 °C vanwege het gebrek aan passende omhullingstechnieken. Tot nu toe is het gedrag van GaN componenten bij hoge frequenties niet bekend en moet dan ook worden onderzocht.

Dit proefschrift onderzoekt de mogelijkheden op hoge frequentie van enkelvoudige chip GaN transistors die geschikt zijn voor toepassingen met hoge spanning, lage stroom. Het onderzoek is uitgevoerd door het ontwikkelen van een model voor de verliezen in GaN transistors, waarbij de gewenste gebruikscondities voor hoog frequent gebruik blootgelegd worden in overeenstemming met de resultaten van het model, met identificatie van de optimale topologieën en gebruiksmanieren om het optimale gebruik van de nieuwe technologie te bereiken, waarbij de mogelijkheden van GaN vermogenscomponenten aangetoond worden in een toepassing waarbij al die nieuwe technieken toegepast zijn.

Modelleren van de verliezen in GaN transistors

Een analytisch model van de verliezen in normally-off GaN transistors is ontwikkeld als een hulpmiddel om het onderzoek mogelijk te maken. De verliezen in een GaN transistor zijn niet alleen gerelateerd aan parasitaire elementen van de component zelf - gerelateerd aan hetzij de chip hetzij de omhulling - maar ook aan de specifieke elektromagnetische omgeving waarin de transistor wordt gebruikt. Met de introductie van de 'chip-scale' GaN transistors, waarbij het elektromagnetische volume van de transistor zelf verwaarloosbaar is in vergelijking met de rest van de vermogensomzetter, krijgen de eigenschappen van het circuit diepgaande invloed op de verliezen in de componenten. Om die reden is er een alomvattend model ontwikkeld dat alle relevante parasitaire elementen meeneemt van zowel de GaN transistor als de drager van het circuit, met het oog op het gedrag en bijbehorende verliezen in de GaN transistor tijdens zowel geleiding als schakelen.

Gebruikmakend van het ontwikkelde model is een analyse van de verliezen in GaN componenten uitgevoerd. Invloeden van parasitaire elementen van zowel de transistor als het circuit zijn grondig onderzocht, waarbij die elementen die het meest bijdragen tot het ontstaan van verliezen in GaN transistors, met name bij hoge frequenties, zijn geïdentificeerd. Daarna is aangetoond wat de wenselijke omstandigheden zijn voor schakelen en geleiden van GaN transistors, zodanig dat de kritische parasitaire elementen de minste negatieve invloed hebben.

Aangetoond is dat aanschakelverliezen voor meer dan 90% van de verliezen van een GaN transistor verantwoordelijk zijn bij hard schakelen, tengevolge van de grote uitgangscapaciteit, terwijl er pas uitschakelverliezen zijn als de afschakelstroom hoog genoeg is (tenmiste > 2.2A bij de in het onderzoek gebruikte transistor) dankzij de grote verhouding tussen uitgangscapaciteit en Miller capaciteit. Verder zijn de geleidingsverliezen laag, dankzij de lage weerstand in aangeschakelde toestand. Een resultaat is ook dat parasitaire inductanties (omhulling en circuits samen) slechts beperkte invloed hebben op de verliezen (<5%), ook in hard-schakelende circuits. Inschakelen bij lage spanning en lage stroom, en lage stroom in het kanaal bij uitschakelen zijn daarom wenselijk condities voor gebruik bij hoge schakelfrequentie.

Topologieën en gebruiksomstandigheden om GaN toe te passen bij hoge schakelfrequentie

Met gebruikmaking van de kennis van de omstandigheden die noodzakelijk zijn om GaN transistors optimaal de gebruiken bij hogere frequenties is een onderzoek uitgevoerd naar topologieën en gebruiksomstandigheden die dat mogelijk kunnen maken, waarbij de PFC als platform is gebruikt. Allereerst is een overzicht gemaakt van de topologieën om een PFC te realiseren, waarbij voor- en nadelen van elke topologie zijn beoordeeld. Daarna is een kwalitatieve analyse uitgevoerd om de eigenschappen te beoordelen als voor elke daarvan de schakelfrequentie in gelijke mate opgevoerd wordt. Resultaat hiervan is dat de boost convertor,

die met de Si-technologie de meest gebruikte is, de meeste voorkeur zal blijven behouden, omdat het opvoeren van de schakelfrequentie nauwelijks invloed heeft op de voor- en nadelen. Vervolgens is de manieren om de omzetterr te gebruiken onderzocht, met aandacht voor wat de manier mogelijk maakt voor de transistor. Voorkeur is ontwikkeld voor Boundary Conduction Mode met Valley Switching (BCM-VS), omdat juist op die manier alle gewenste condities mogelijk gemaakt worden. Daarnaast biedt BCM-VS andere voordelen die niet mogelijk zijn in CCM of zelfs BCM, zoals eliminatie van het effect de reverse recovery van de vrijloopdiode op de verliezen in de transistor, het elimineren van de invloed van de parasitaire inductanties op de aanschakelverliezen, de mogelijkheid om een condensator parallel aan de schakelaar om overspanning te reduceren, enz..

Optimaal gebruik van GaN bij hoge frekwentie

In overweging nemend dat alle bestaande topologieën en werkingsprincipes meestal ontworpen zijn om bij Si-componenten te passen is een uitgebreid onderzoek uitgevoerd naar de uitdagingen en de afwegingen bij het toepassen van GaN in een boost convertor met BCM-VS. BCM-VS zal - in vergelijking met andere modes - leiden tot hogere afschakelstroom, wat weer zal leiden tot hogere spanning en - als de stroom hoog is - meer afschakelverliezen. Aan de schakelaar parallel schakelen van externe capaciteiten wordt aanbevolen omdat dit helpt om beide problemen te verminderen, en de verliezen in de GaN transistor kunnen geminimaliseerd worden door de juiste waarde te kiezen voor die capaciteit. Daarnaast is er het effect dat in geval Vout>2Vin, omgekeerde geleiding van een GaN transistor zal optreden doordat de spanningsval over de transistor in omgekeerde geleiding tamelijk hoog is (1.3~1.7V). Bewezen is dat aanschakelen van de GaN transistor voordat negatieve stroom optreedt, en in het bijzonder zodra de spanning over de schakelaar het nulpunt heeft bereikt (ZVS) , gunstig is om de totale verliezen te verminderen.

Om een goed ontwerp van een GaN boost convertor in BCM-VS te sturenzijn voor deze gebruiksomstandigheden de grenzen en beperkingen duidelijk gemaakt. Ontdekt is dat de verhouding van de dode tijd, die een natuurlijk gevolg is van deze modus, ten opzichte van de totale schakelcyclus, toeneemt met toenemende frequentie, wat resulteert in toenemende stromen in de omzetter en grenzen stelt aan de maximum haalbare frequentie van de convertor en ook het ontwerp en keuze van de andere componenten beïnvloedt. In het algemeen maakt BCM-VS een hogere schakelfrequentie mogelijk dan welke andere mode ook, waarbij de maximaal haalbare frequentie van een op GaN gebaseerde convertor met BCM-VS begrensd is door schakelverliezen als Vout <2Vin, en door geleidingsverliezen als Vout>Vin.

Demonstratie van de potenties van GaN technologie voor hoog frequent schakelen

Hoogfrequent gebruiksmogelijkheden van GaN componenten, waarvan bewezen is dat ze werkelijk waarmaken wat de eigenschappen van het materiaal belooft als ze op de juiste wijze

gebruikt worden, is gedemonstreerd in een PFC boost convertor bedoeld voor hoge schakelfrequentie en hoge efficiëntie. In de praktijk zijn er beperkingen vanwege het niet beschikbaar zijn van PFC regelaars voor MHz gebruik, en vanwege het ontbreken van geschikte magnetische materialen, incl. kernvormen. Desondanks is een op GaN gebaseerde PFC met BCM-VS ontworpen. Minimalisering van de verliezen in de omzetter is gerealiseerd door het zoeken naar de optimale waarde van de externe capaciteit met behulp van een model voor de verliezen in de totale PFC. Een experimentele opzet is gebouwd volgens dit ontwerp. Het is aangetoond dat ook al is de spoel niet optimaal wegens praktische beperkingen, de 3MHz PFC boost convertor met maximaal instantaan vermogen van 600W een gemiddelde efficiëntie bereikt van 98.5%. Dit geeft aan dat a) GaN componenten de mogelijkheid hebben om zeer goede vermogensomzetters met hoog frequent schakelen mogelijk te maken als ze op de goede manier gebruikt worden, b) PFCs met BCM-VS een ideale toepassing is voor GaN transistors omdat deze toepassing daar zeer geschikt voor is, c) het opvoeren van de schakelfrequentie van een vermogensomzetter in de huidige stand van zaken niet meer beperkt is door de schakelaars maar door andere praktische zaken zoals het ontwerp van de regelschakeling, de magnetica, enz.

Publications and Award

Publications

1. W. Wang, F. Pansier, J. Popovic, J. Ferreira, “An improved physics-based loss model of GaN GIT and single-die GaN HEMT”, *IEEE transaction on Power Electronics*, Under review
2. W. Wang, F. Pansier, J. Popovic, J. Ferreira, “Valley switching mode operation of GaN GIT in high frequency boost converters”, *IEEE transaction on Power Electronics*, Under review
3. W. Wang, S. de Haan, F. Pansier and J. A. Ferreira, " Novel and simple calorimetric methods for quantifying losses in magnetic core and GaN transistor in a high frequency boost converter," *Chinese Journal of Electrical Engineering*, pp. 68-75, Vol. 2, No. 2, Dec. 2016
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6. W. Wang, F. Pansier, S. de Haan, J. A. Ferreira, “Losses comparison of Gallium Nitride and Silicon transistors in a high frequency boost converter”, *8th International Conference on Integrated Power Systems (CIPS)*, Feb. 2014
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Award

Best Paper Award – in session of DC conversion systems

39th Annual Conference of the IEEE Industrial Electronics Society (IECON), Vienna, Austria, 2013

Curriculum Vitae

Wenbo Wang was born in Shandong, China, in October 1984. He obtained his bachelor degree from Northwestern Polytechical University in Xi'an China in 2008 majored in Automation and his master degree in the field of Power Electronics from the same university in 2010. Then, he began to work toward his Ph.D degree in the formerly Electrical Power Processing (EPP) now DC Systems, Energy Conversion & Storage (DCES) group in Delft University of Technology, in the Netherlands. His Ph.D project focuses on application of wide bandgap power devices in power electronics converters.

His research interests include high frequency power electronics converters, wide bandgap power devices, magnetics and renewable energy.