01 May 2004

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Recommended Citation

T. Sudo et al., "Electromagnetic Interference (EMI) of System-on-Package (SOP)," *IEEE Transactions on Advanced Packaging*, vol. 27, no. 2, pp. 304-314, Institute of Electrical and Electronics Engineers (IEEE), May 2004.
The definitive version is available at https://doi.org/10.1109/TADVP.2004.828817

Electromagnetic Interference (EMI) of System-on-Package (SOP)

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***Abstract*—Electromagnetic interference (EMI) issues are expected to be crucial for next-generation system-on-package (SOP) integrated high-performance digital LSIs and for radio frequency (RF) and analog circuits. Ordinarily in SOPs, high-performance digital LSIs are sources of EMI, while RF and analog circuits are affected by EMI (victims). This paper describes the following aspects of EMI in SOPs: 1) die/package-level EMI; 2) substrate-level EMI; 3) electromagnetic modeling and simulation; and 4) near electromagnetic field measurement. First, LSI designs are discussed with regard to radiated emission. The signal-return path loop and switching current in the power/ground line are inherent sources of EMI. The EMI of substrate, which work as coupling paths or unwanted antennas, is described. Maintaining the return current path is an important aspect of substrate design for suppressing EMI and for maintaining signal integrity (SI). In addition, isolating and suppressing the resonance of the DC power bus in a substrate is another important design aspect for EMI and for power integrity (PI). Various electromagnetic simulation methodologies are introduced as indispensable design tools for achieving high-performance SOPs without EMI problems. Measurement techniques for near electric and magnetic fields are explained, as they are necessary to confirm the appropriateness of designs and to investigate the causes of EMI problems. This paper is expected to be useful in the design and development of SOPs that take EMI into consideration.**

***Index Terms*—Crosstalk, electromagnetic interference (EMI), modeling, near field, power bus, SOP (system-on-package).**

I. Introduction

THE electromagnetic interference (EMI) mechanism in real electronic products is normally complex, because it is closely related to LSI design, package structure design, printed circuit board (PCB) wiring design, enclosure design and other factors. LSI switching operation is considered to be an inherent source of EMI. Fig. 1 shows a schematic drawing of SOP configuration with digital integrated circuits (ICs) and RF ICs. The signal transmission from one chip to another on an SOP can be considered to excite two types of noise sources. The first is normal mode type radiation due to the signal-return path loop, while the second is the common mode excitation of the power/ground plane due to switching currents from LSI. The former is strongly related to the signal integrity (SI), such as reflection noise at terminations, while the latter is strongly related to the power/ground bounce or power integrity (PI). When excited by switching currents, the power/ground plane works as an unwanted antenna at the resonant frequencies. Also, other types of common mode noises are frequently excited under a complex packaging environment (for example, return path irregularity due to a slit or unsymmetrical return current distribution in the ground plane) and contribute to electromagnetic radiation.

In the case of a cellular phone, high-frequency harmonics are generated from digital ICs. The harmonics transmit through the package and PCB wiring, and couple with sensitive circuits such as that for the RF receiver. Coupling with the enclosure also affects sensitive circuits. As a result, such couplings induce the instability or the performance degradation of the RF receiver in the cellular phone. Basically, in the design of SOPs, suppression of the energy of EMI sources is required for dies/packages, and separation of the source from coupling paths is required for designing substrates or interposers. Thus, EMI problems can then be broken into the "Source-Path-Victim" model as shown in Fig. 2 [1]. The "source" refers to noise strength accompanying the LSI operation, while the "Path" refers to conductive and radiative coupling paths between signal traces or between power supply conductors. The power/ground plane often works as an unwanted patch antenna at the resonance frequencies. The element "Victim" can also be referred to as "Antenna" when such a radiative emission is of interest.

In this paper, electromagnetic interference mechanisms are classified based on the "Source-Path-Victim" model. First, die/package-level EMI is discussed as a noise source. A typical method for modeling the on-die power supply is introduced. In this method, the on-die decoupling capacitor can localize the switching currents within a chip. Next, substrate/interposer-level EMI is discussed. Crosstalk noise between signal lines and the discontinuity of the return current path due to a slot in the ground plane or due to signal transition through via holes are considered as causes of coupling on the substrate/interposer. DC power bus design is becoming essential for the provision of an effective power supply line and for avoiding power/ground plane resonance. The electromagnetic modeling and simulation methods are discussed in order to understand the phenomena better and to estimate the level of EMI. Finally, the current state of the art in probing methods is summarized.

Manuscript received March 11, 2004; revised April 8, 2004.

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Digital Object Identifier 10.1109/TADVP.2004.828817

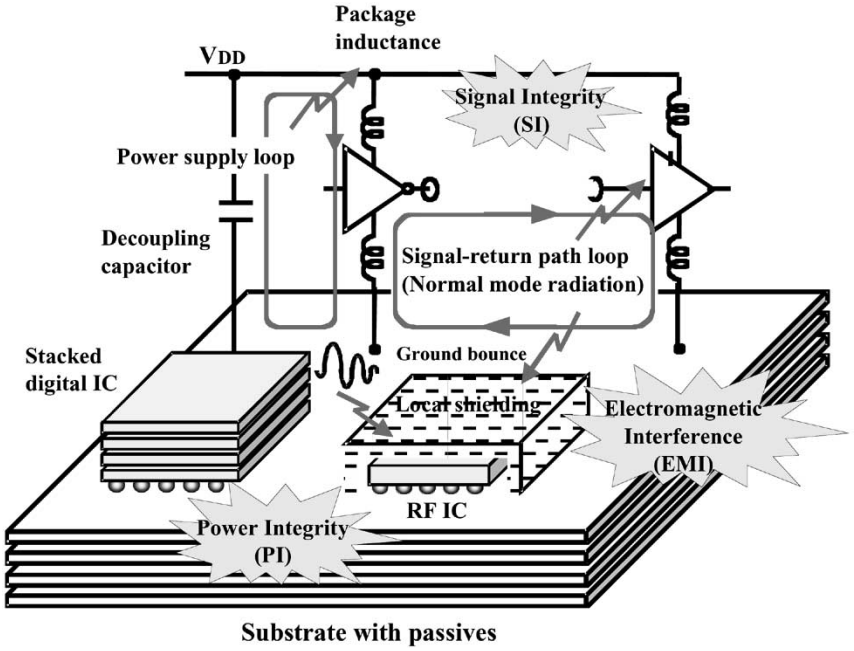

Fig. 1. EMI among digital ICs and RF ICs in a SOP. Signal transmission accompanies the excitation of normal mode radiation (signal-return path loop) and ground bounce due to switching currents.

Fig. 2. Source-Path-Victim (Antenna) model.

The miniaturized shielded loop probe is a typical probe used to measure the distributions of the electric and magnetic near field strengths. New probing methods using the magnetooptical (MO) effect or the electrooptical (EO) effect have also been developed to obtain higher spatial resolution.

II. Die/Package-Level EMI

Die/package-level EMI refers to the source strength rather than the coupling path effect. System design engineers did not recognize LSIs as noise sources for EMI till several years ago. In the car-electronics field, a microcontroller in an engine control unit (ECU) with a harness was found to be a significant noise source generating interference in the FM radio frequency band. Semiconductor manufacturers have been required to develop low-noise microcontrollers to alleviate such electromagnetic interference. This problem accelerated the study on the LSI design from EMI point of view.

A. On-Die Power Supply Modeling

Die-level EMI has been reported by many European researchers. The EMI-generating mechanism has been investigated by developing dedicated test chips [2]–[6]. Modeling of the on-chip power supply network has been proposed to identify the properties of the microcontrollers used in the ECU. Fig. 3 shows a proposed integrated circuit electromagnetic model (ICEM) submitted to the International Electronic Commission (IEC) [7]. The simplified *RLC* circuit consists of the inductance of the package and the capacitance of the internal parasitic capacitance between the power and ground line. Another research group in Okayama University in Japan is proposing a similar kind of equivalent circuit called linear equivalent circuit and current source (LECCS) model [8]–[10].

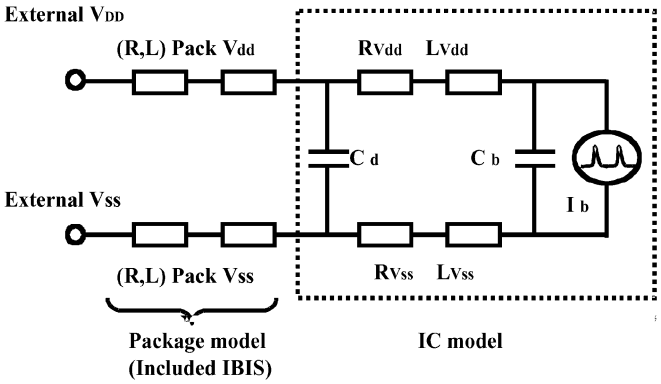

Fig. 3. ICEM model.

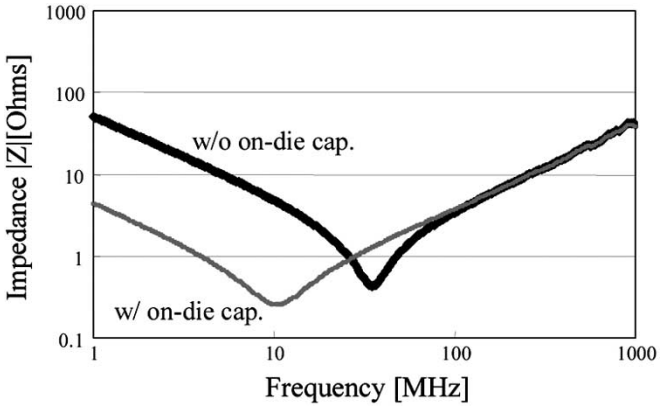

Fig. 4. An example of the measured impedance of a power supply network for a test LSI without and with on-die decoupling capacitor.

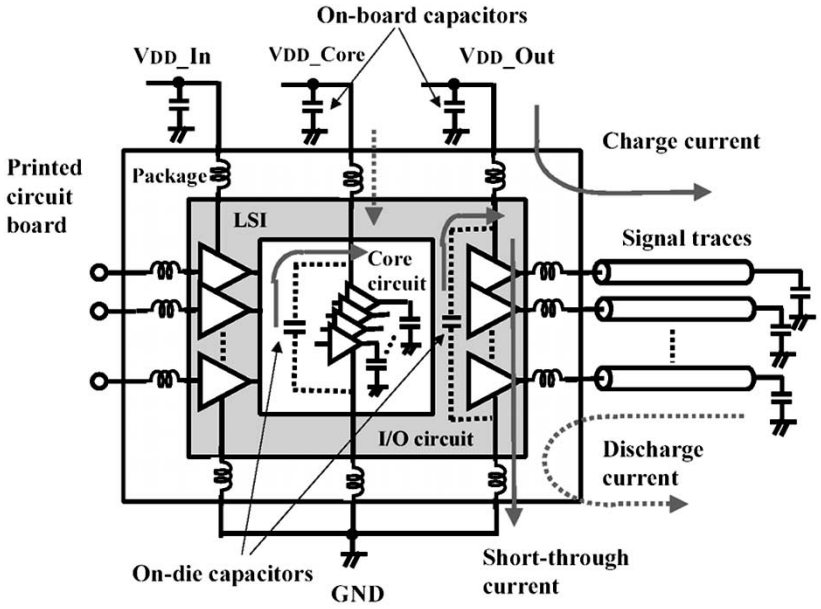

Fig. 5. Typical power supply network and current flow for the switching of core logic circuits and I/O buffer circuits.

Power supply networks on a die-level have also been investigated to reduce the level of ground bounce in high-end microprocessors and CMOS ASICs [11]–[21]. They are designed to avoid overshoots/undershoots in signal lines and to avoid ground bounce by the switching of the core circuits and output buffer circuits. The roles of the on-chip and off-chip decoupling capacitors have been investigated [22], [23].

Fig. 4. shows an example of the measured impedance characteristics of the power supply network for test LSIs without and with on-die decoupling capacitor up to 1 GHz. The equivalent series *RLC* circuit and the values can be obtained from the impedance characteristics. In this case, the equivalent *RLC* values were 0.43 ohms, 1.5 nH, 3.4 nF for the chip without on-die capacitor, while 0.25 ohms, 1.5 nH, 35.6 nF for with on-die capacitor [24].

B. Localizing Switching Currents

The on-die power supply network ordinarily consists of two types networks, one for I/O buffer circuits and the other for core logic circuits. Fig. 5 shows a typical configuration for such a separated power supply network and the current flows for the switching of the core circuits and the output buffer circuits. On-die decoupling capacitors between the power and ground supply lines are effective for localizing the switching current inside a die, especially for the core logic circuits. The charge and discharge currents at the rising and falling edges cannot be localized, because they are constrained to make a signal-return path loop. Only the short-though current generated when the I/O buffer circuits are switched can be localized inside a die.

Experiments have been performed on simultaneous switching noise and far-field radiated emission for different on-die power supply networks [24]–[26]. Two types of CMOS test LSIs were used as noise generators: one without an on-die decoupling capacitor and the other with an intentional on-die decoupling capacitor. They were assembled in a CSP (chip scale package). Fig. 6 shows the measured far-field emission for output buffer operation at a frequency of 25 MHz. Reduced radiated emission was observed for every harmonic for operation of the core logic circuits by the on-die decoupling capacitor (not shown here), while only spectra with even-order harmonics (50/100/150 MHz) were significantly reduced for switching of the output buffers due to the on-die decoupling capacitor. It is thought that the short-through current, which causes even-order harmonics, was localized inside the die due to on-die decoupling capacitor.

III. Substrate-Level EMI

The main roles of substrates and interposers for a SOP are redistribution of interconnections and expansion of pad pitch. In the redistribution layers, if sensitive analog and RF traces are parallel to high-speed digital traces and/or intersect the traces, crosstalk noise occurs between them. Crosstalk noise also occurs between adjacent power planes of different voltages when the dc power buses resonate. Moreover, in high-speed design, discontinuity of the return current is one of the most important considerations not only for signal integrity (SI) and power integrity (PI), but also for EMI. In particular, when a signal trace traverses a slit in the ground plane or when a signal transits through via holes among the power distribution planes, the return path of the signal is discontinuous. The resonance of the DC power buses is a common issue related to PI. However, original design methods are required in order to take EMI into consideration. This section describes design issues related to substrate-level EMI and introduces solutions based on state-of-the-art research results.

A. Crosstalk

Crosstalk noise is the coupling of electromagnetic energy between traces [see Fig. 7(a)]. This induced energy degrades the signal integrity of the victim trace and causes errors or instability in the circuits connected to the victim trace [27]. This coupled noise also changes into emitted energy that radiates from the cable linked to the victim trace [28]. The amount of crosstalk

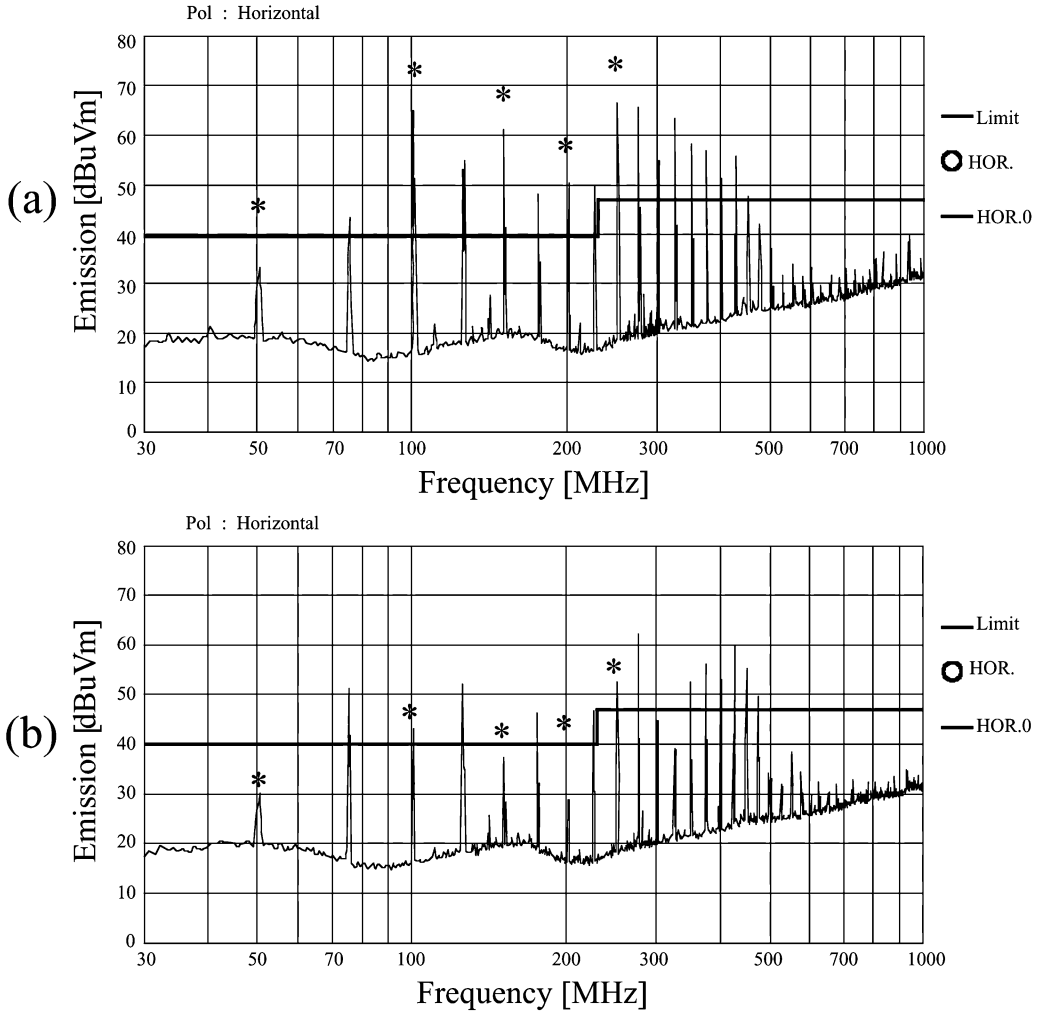

Fig. 6. Comparison of far-field radiated emission of a test LSI for 15 simultaneous switching buffers operated at 25 MHz. (a) is for without on-die capacitor. (b) is for with on-die capacitor.

noise depends on not only the space between adjacent traces, but also on the reflection due to the impedance mismatches at the driver and the terminations of the traces. To avoid such kinds of crosstalk noise, the layout of the substrate should be determined taking into consideration the sensitivities of the victim traces.

In addition, crosstalk between adjacent power planes is also an important consideration [see Fig. 7(b)]. Most of the latest LSI chips include several power supply banks for core and I/O circuits in order to decrease total power consumption. Consequently, the substrate or interposer should be provided with different power areas and planes in them. The power distribution system is essentially a route for supplying dc voltage to a chip. However, at frequencies above a few hundred megahertz, this power distribution system involves many harmonics of switching noise and it involuntarily works as a resonator [29]. Therefore, when the frequencies of the harmonics correspond to those of the power bus resonance, the dc voltage of the power distribution plane fluctuates significantly, and crosstalk occurs between the adjacent power planes [30].

B. Discontinuity of Return Current

The discontinuity of the return current is an extremely important consideration not only for SI and PI, but also for EMI.

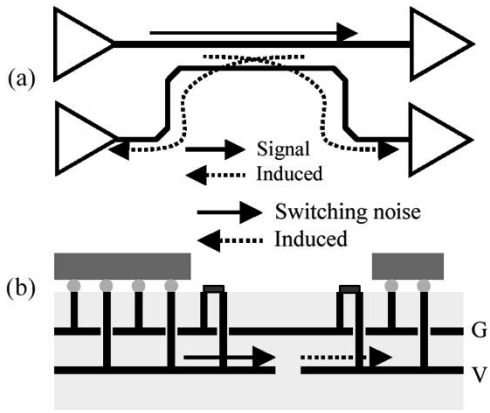

Fig. 7. Crosstalk issues due to (a) adjacent signal traces and (b) adjacent power planes. "G" indicates the ground plane and "V" indicates the power plane.

The return current of a signal trace flows beneath the trace in the metal plane. A slit in the plane beneath the trace detours the return current path or makes it discontinuous [see Fig. 8(a)], and this discontinuity causes larger radiated emissions [31] as well as degradation of SI and PI. Also, because the strengths of the near electric and magnetic fields at the slit increase, the fields

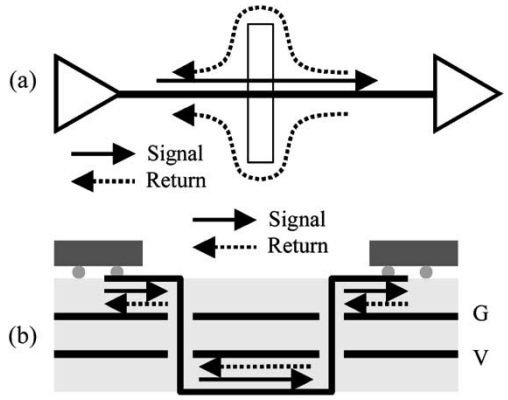

Fig. 8. Discontinuity of return current path due to (a) a slit in a ground plane and (b) via holes through the power/ground planes. "G" indicates the ground plane and "V" indicates the power plane.

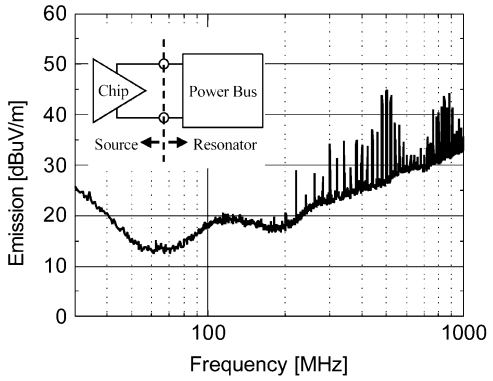

Fig. 9. Measured radiated emissions due to the resonance of the dc power bus.

easily couple with nearby signal traces and cause crosstalk problems [32].

When signals transit through via holes among the power or ground planes with different voltage, the return current path of the signal is discontinuous at the via holes [see Fig. 8(b)]. Beginning at IC_1, the current follows the conducting trace to the via, and then is carried by conduction current on the via onto the trace on the lower level through the second via and to IC_2. The return current uses the upper surface of the adjacent ground plane as the return from IC_2, following beneath the signal trace. When the return current encounters the via, it transitions through the anti-pad hole to the lower surface of the ground plane, and then through displacement current is continued to the upper surface of the voltage plane. The displacement current is a distributed property of the parallel power planes, and excites the distributed modes of the planes. The current is continued to the lower surface of the voltage plane through the antipad in the voltage plane, and follows beneath the signal trace on the lower layer to the via adjacent to IC_1, where the process is repeated. If the signal line happens to be an I/O line that goes off the substrate, there is a conductive path for radiated EMI [33], [34].

This type of discontinuity induces the dc voltage fluctuation and consequently causes PI problems [35]. It also causes strong radiation due to resonance of the power distribution plane [36]. In particular, the routing of high-speed digital signals should be designed taking the return path into consideration.

C. Resonance of DC Power Bus

From the viewpoint of PI, the lower the ac impedance of the power distribution network the better for the chip, package, and substrate [37]. From the viewpoint of EMI, however, transmission of switching noise from a chip to a package or substrate through the common impedance path is undesirable. Also, the dc power bus resonates at frequencies above a few hundred megahertz, because the power and ground planes pair up and work as a parallel plate transmission line resonator [38]. Fig. 9 shows an example of radiated emissions due to power bus resonance. The emissions increase at approximately 400 and 850 MHz, where the power bus resonates. To separate the switching noise from the resonator, isolation techniques are necessary. One of the solutions is a power island [39]. A part of the power plane is cut from the entire power plane by using a surrounding gap, and the power island is connected using a ferrite bead inductor. The inductor checks the switching noise in the island and isolates the noise from the common power distribution network (which has the potential to resonate). This approach is equivalent to using pi-network filters consisting of two capacitors and an inductor. If the ferrite bead inductor is replaced by a power trace, this method can be used for wider frequency isolation because the length and width of the trace can be controlled without the impedance limitations of the ferrite [40].

High-frequency loss suppresses the power bus resonance and consequently reduces radiated emissions. This loss reduces the quality factor of the resonance and suppresses the impedance of the power bus at high frequencies without sacrificing a dc voltage drop. The use of a thin pair of power and ground layers increases the conduction loss of these planes [41]. Dielectric loss of the substrate material also works as well. Damping using high frequency loss is one of the most effective techniques for suppressing EMI.

IV. Modeling and Simulation of EMI

Advances in SOP technologies will lead to numerous new applications. As the dimensions of devices and packages decrease, the challenges of integrating technologies with diverse signal levels, power requirements, and bandwidths for electromagnetic compatibility increase. The time and cost of developing engineering prototypes is considered to be prohibitive in the present environment, necessitating sophisticated EMI modeling and simulation for engineering design innovation early in the design cycle. Numerical EMI modeling reduces to the following three issues: what to model, how to model it, and at what scale. The first is related to incorporation of the essential features of the physical structure that captures the coupling physics, while the second and third are related to the numerical implementation of the physics in the particular tool.

The physics of the EMI coupling path depicted in Fig. 2 can be categorized as conductive, electric-field coupled, and magnetic-field coupled [42]. The unintentional noise current then exits from the package on an intended signal path and creates potential interference problems. A common electric-field coupling path is illumination of a heatsink by the IC that it is intended to cool. Magnetic-field coupling results from flux linkage between two circuits that may or may not share a

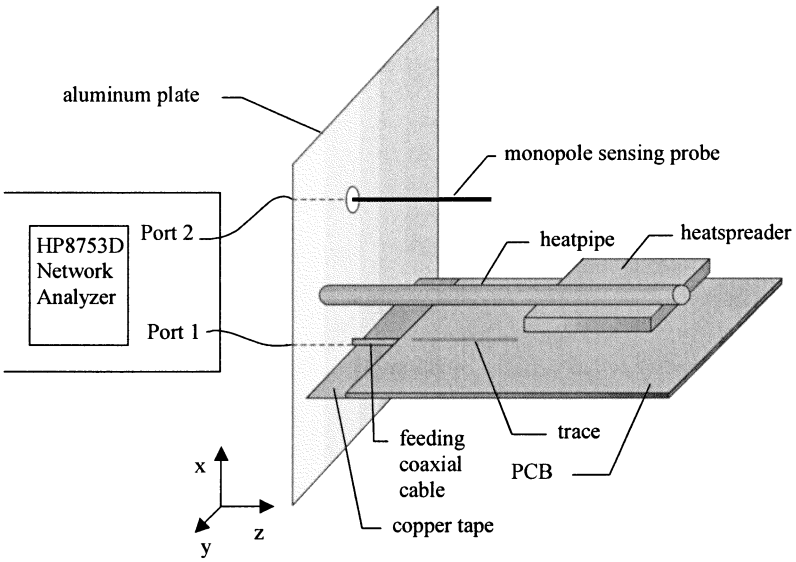

Fig. 10. Experimental setup for study of the coupling of a driven trace to a simplified heatsink/heatpipe structure.

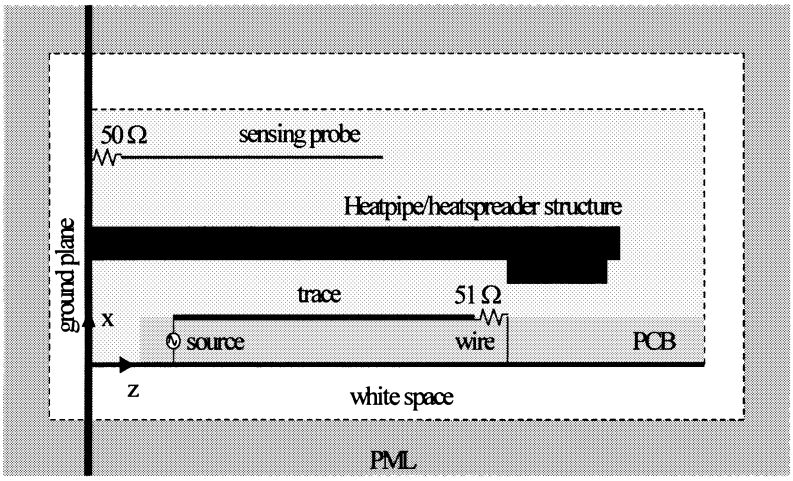

Fig. 11. Cross-section of the FDTD computational domain for coupling from a driven trace to a simplified heatspreader/heatpipe structure.

common conduction current path. For example, the currents on the vias of the ICs connected to the voltage plane are magnetically coupled by the flux from the vertical current segment penetrating the area between the voltage and ground planes in the region from the via to the adjacent IC and the substrate edge [43]. As in the case of assessing signal integrity, determination of the EMI coupling path entails tracing the current from the noise source to the "EMI antenna" or the victim and back to the source in a complete current loop.

A. Heatspreader/Heatpipe Model

The first application of numerical simulation is a cooling scheme with a heatspreader/heatpipe for high power dissipation LSIs. The cooling structure was investigated by full-wave numerical modeling and through experiments is shown in Fig. 10.

The computational domain for FDTD modeling is shown in Fig. 11. Perfectly matched layers (PML) were employed as the numerical absorbing boundary conditions [44]. The aluminum plate was modeled as a perfect electric conducting (PEC) surface extended to the PML layer. The copper ground plane on the bottom of the PCB, the trace, and the surface of the heatpipe structure were also modeled as PEC surfaces. Since only a rectangular mesh was available in the FDTD codes, the cross section of the cylindrical heatpipe was approximated as a staircase octagon. The feeding conductor, the wire connecting the SMT resistor to the PCB ground plane, and the monopole probe were modeled using a thin wire subcellular algorithm [45]. A Debye model was used in the FDTD method to take into account the dispersion in the FR4 dielectrics of the PCB [45], [46].

A sinusoidally modulated Gaussian voltage source with a 50-Ω impedance was employed at the feeding point. The magnetic fields circling the source were modeled in the same manner as a thin wire to give the cross section of the source a specified physical dimension [47]. The resistor was modeled as a lumped element using a subcellular algorithm [48], with the circling magnetic fields modified to use the thin-wire algorithm and give it the specified cross-sectional dimensions. The $|S21|$ measurement and the FDTD modeling results are shown in Fig. 12. The resonance at 557 MHz is due to the sensing probe. The

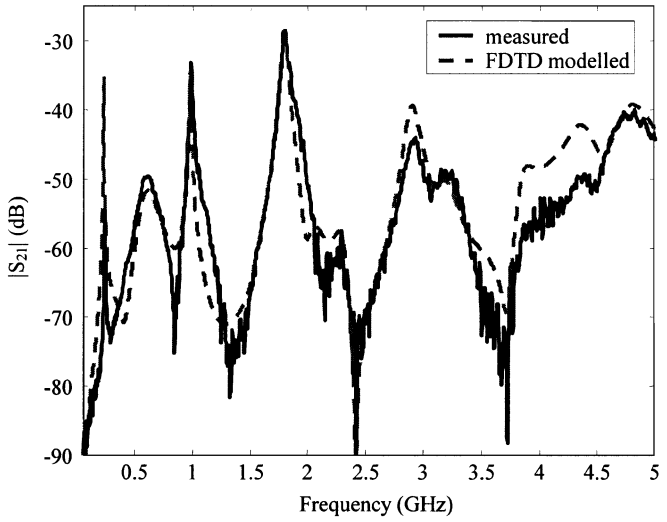

Fig. 12. Comparison between measurements and FDTD modeling for coupling from a driven trace to a simple heatspreader/heatpipe structure.

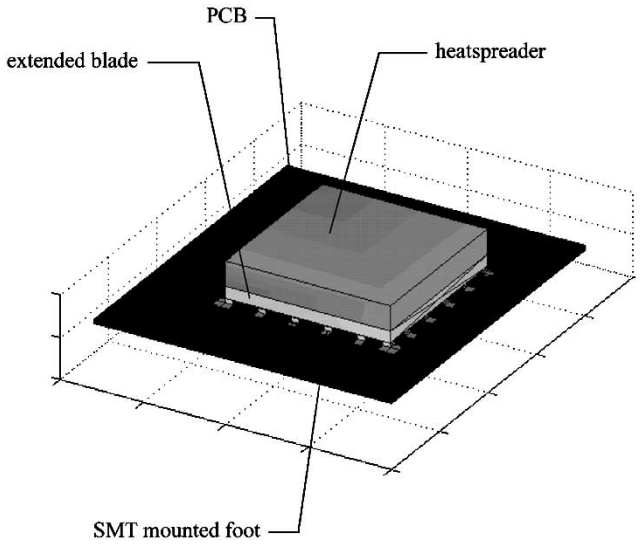

Fig. 13. Grounding of heatspreader with the extended side blades and conducting legs and feet.

resonances at 252 MHz, 980 MHz, 1.79 MHz, 2.92 GHz, and 4.75 GHz are dominated by the heatpipe/heatspreader structure. Therefore, the presence of the heatpipe/heatspreader structure introduces resonances over a wide bandwidth. Comparing the modeling results and the measurements, the discrepancies of the resonances are within 3%, and the discrepancies in magnitude are within a few dB.

The good agreement between the measured and modeled results indicates that FDTD is a suitable numerical tool to study this class of EMI problem. While the geometry is relatively simple, it is clear that a high level of detail is necessary in the modeling and that powerful numerical algorithms are required to achieve agreement with the experimental results. As the level of complexity of the geometry increases, the care and attention required in the numerical modeling increases correspondingly.

B. Grounding Model

The second application of numerical simulation for EMI mitigation is shielding. In mixed-signal designs, such as cellular telephone designs, where RF and digital functions share the same substrate and are located close to each other, a dominant coupling path is through the electric field from digital IC to RF IC. Typically, local conducting shields are applied over each IC, source and victim, to mitigate this interference. An example of grounding scheme for the heatspreader is shown in Fig. 13, which is typical of local shields that are placed around digital and RF ICs for EMI mitigation. The four edges of the heatspreader were extended down toward the PCB and truncated 60 mils above the PCB. Conducting legs and feet were used to connect the extended blades of the heatspreader to the top layer of the PCB. A practical implementation of this geometry would be a heatspreader tapered to a knife edge, which could be inserted into a PCB SMT mount receptacle made of sheet metal. The SMT-mount feet were chosen to be 100 mil wide and 300 mil apart from edge to edge so that the feet on the PCB would not severely limit routing flexibility. Three different configurations were studied and compared as detailed below.

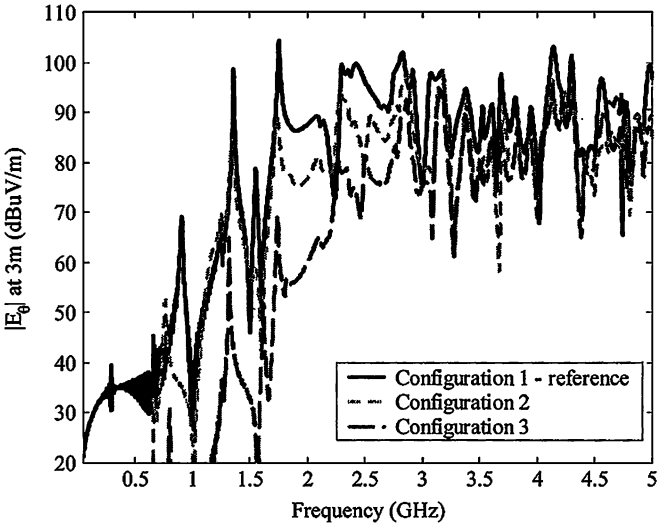

Fig. 14. Comparison of FDTD modeled results of radiated EMI from various heatsink grounding schemes.

#1— No heatspreader grounding scheme was applied. This configuration was used as a reference.

#2— The heatspreader was grounded as shown in Fig. 13. Only the four SMT-mount feet at the corners of the heatspreader were connected to the PCB ground plane using 20-mil-diameter vias. The other feet on the PCB were floating. The vias were modeled in the FDTD simulation using the thin-wire algorithm.

#3— All the feet were connected to the PCB ground plane with 20-mil-diameter vias.

A $2'' \times 2''$ metallic patch was located on the PCB directly below the heatpipe. This patch coupled energy through the electric field to the heatspreader. The entire heatspreader/heatpipe geometry with the proposed local shield was placed in an enclosure with a slot in the enclosure, and modeled with FDTD. The radiated field results at 3 m in front of the slot side of the enclosure are shown in Fig. 14.

TABLE I
PRACTICAL CHARACTERISTICS OF MINIATURE PROBES

Probe type	Principle	Spatial resolution
Shielded loop	Magnetic loop	50 μm-10 mm
One-turn coil	Differential loop	40 μm-1 mm
MO	Faraday effect	50 μm or less
EO loop	Pockels effect+loop	10 μm or less

The above example demonstrates the application of numerical EMI modeling for engineering design. However, only one specific EMI coupling path was accounted for in the modeling, i.e., coupling directly for the IC to the shield. While it appears from the results in Fig. 14, that more effective grounding can provide significant EMI reduction below 3 GHz for the PCB scale geometry considered, the conclusion holds only for the modeled EMI coupling path. The high-speed signal lines that egress from the shield will capacitively couple (electric-field) to the pads or via connections to ground of the shield.

These specific geometries were of the printed circuit board scale, the geometry is representative of both thick- and thin-film networks and the objectives of coupling circuit modeling and simulation with the full-wave aspects of interference problems are similar [49].

V. NEAR-FIELD EVALUATION

Significant improvements have been made in the measurement of high-frequency electromagnetic fields in LSIs and PCBs in the last couple of years. Table I shows typical miniature probes. In the past, near-field mapping methods were used to measure electromagnetic fields with a spectrum analyzer and display the electromagnetic distributions on-screen in order to search for unknown noise sources, paths of high-frequency current, and resonance frequencies from the metal planes of PCBs in evaluations of EMI. However, package and circuit designers have been aiming to use near-field measurements to quantitatively evaluate the high-frequency performance of packages. Therefore, the trend in electromagnetic measurements has been shifting from electromagnetic mapping to measuring currents on traces, using the magnetic near field to verify the high-frequency behavior of models for IC/LSI power circuits [50]–[52]. In addition, it is necessary to obtain high-frequency characteristics at each packaging level to develop a design method where all stages from the LSI chip to the PCB can be considered.

A. High-Resolution Spatial Measurement on Chips

A few attempts have been made to develop noncontact measuring methods at the inner-chip packaging level of LSIs by transforming the measured magnetic near field to the current in the trace. The main purpose has been to use the measured data to prepare behavioral models of the inner circuits of LSIs and verify how design changes to all blocks of their inner circuits will be reflected in the higher packaging levels, such as in the ICs. Spatial resolution increases of three- to 10-fold were demonstrated by electromagnetic mapping on devices under test

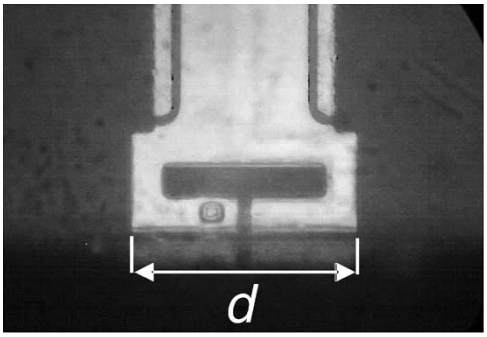

Fig. 15. Micrograph of a shielded loop coil fabricated with the thick-film process. ($\mathrm{d} = 50$ to 500 μm, with spatial $\mathrm{resolution} = 40$ μm).

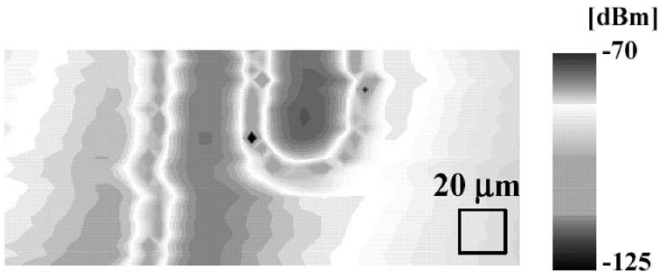

Fig. 16. X-Z mapping of the magnetic near-field using an MO crystal.

(DUT). Fig. 15 is a micrograph of a miniature shielded loop probe fabricated by NEC Corporation using a fine thick-film process [53], [54]. The magnetic near field on the power trace of an inner chip in an LSI was measured. It has been reported that the probe can be applied to separate the magnetic field at a pitch of several μm and estimate the path over which the high-frequency current is flowing [54]. It will be possible to calibrate the spectrum and waveform for a trace in an LSI chip with a technique similar to that used to calibrate the current in PCBs [55].

The method used to measure the magnetic field, which was developed by the Association of Super-Advanced Electronics Technologies (ASET), uses the MO effect [56]. ASET has fabricated a fiber edge on an MO crystal to measure the magnetic near field around the DUT and has achieved a spatial resolution of the order of 10 μm as well as a measurable GHz-range bandwidth. Fig. 16 shows the x-y mapping of the magnetic near field over a 20-μm-scale circuit. However, it is still necessary to develop a method of calibrating the current to make the probe suitable for practical use in layout design. These probes can be used at frequencies of up to 2 GHz.

B. Verification of High-Frequency Power Current

Two measurement methods, the magnetic probe (MP) method [57] and the 1-ohm/50-ohm method have been standardized for EMI evaluation at the IC/Package to PCB levels by the IEC. International standards were issued in 2002 to evaluate the EMI in LSI circuits. Although the MP method was developed to measure high-frequency power currents using the magnetic near field to quantitatively compare the noise emissions from LSIs, the measured data can be directly used to verify macromodels for power-circuit simulations [50]. For example, the high-frequency current flowing through power-supply traces has been identified as possibly the main factor causing interference and

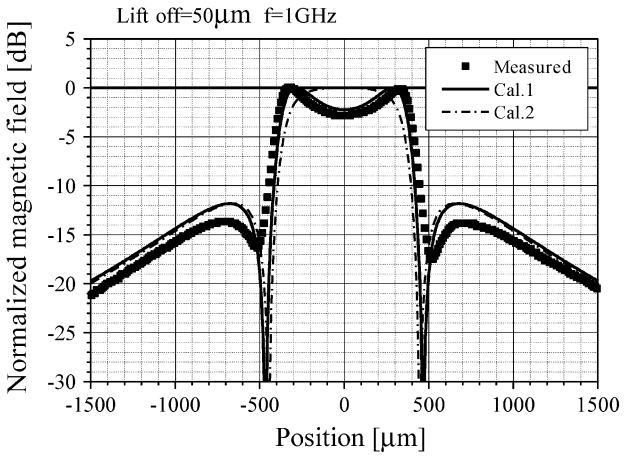

Fig. 17. Measured magnetic field over a 770-μm-wide microstrip line. Cal.1 shows the calculated results with the nonuniform distributed current model, while Cal.2 shows the calculated results with the uniform distributed current model.

degrading signal integrity (SI). Another approach has been to closely examine the characteristics of traces. Fig. 17 plots the results of observing the edge effect by measuring the x-component in the magnetic near field with the miniature shielded loop probe [53], [54].

C. Electromagnetic Mapping and Far-Field Estimation

Some improvements have been made to electromagnetic mapping at the IC/Package to PCB levels [58]–[60]. Although these mapping methods are useful in visualizing the near field and in estimating noise emissions, the obtained data are expected to be converted to more effective information such as noise source identification or far-field estimation [61].

VI. Summary

Future SOPs that integrate high-performance digital LSIs and RF/analog circuits will be required to have smaller electromagnetic radiation and to minimize electromagnetic interference inside active devices. Consequently, SOPs must be designed focusing not only on signal integrity and power integrity, but also on EMI. The design process must make full use of modeling and simulation techniques as well as validation techniques with near-field probes.

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