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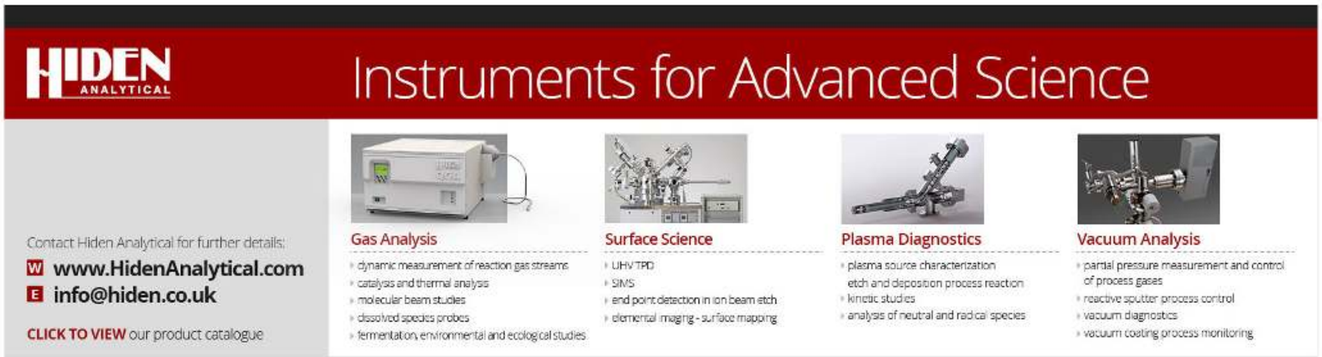
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Electromigration behavior of Cu metallization interfacing with Ta versus TaN at high temperatures

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High-temperature stability of Cu-based interconnects is of technological importance for electronic circuits based on wide band gap semiconductors. In this study, different metal stack combinations using Ta or TaN as capping- and/or barrier-layer, in the configuration cap/Cu/barrier, are evaluated electrically and morphologically prior to and after high-temperature treatments. The symmetric combinations Ta/Cu/Ta and TaN/Cu/TaN are characterized by a low and stable sheet resistance after annealing up to 700 °C. Asymmetric combinations of Ta/Cu/TaN and TaN/Cu/Ta, however, display an increase in sheet resistance values after annealing at 500 °C and above. This increase in sheet resistance is considered to result from Ta diffusion into the grain boundaries of the Cu film. The preliminary electromigration studies on the TaN/Cu/Ta and TaN/Cu/TaN structures show a twofold higher activation energy and a tenfold longer lifetime for the former, thus suggesting an important role of the interface between Cu and the cap and/or barrier. © *2016 American Vacuum Society*. [http://dx.doi.org/10.1116/1.4967372]

I. INTRODUCTION

High-temperature electrical and morphological stability of interconnect is critical for electronic systems based on wide band gap semiconductors. In this context, Cu is found to have several interesting properties, including low resistivity and high resistance to electromigration in comparison with Al.[1–3] As Cu metallization is well-studied as the dominant interconnect in advanced integrated circuits (ICs), it is a good choice to start with by examining its applicability for high-temperature applications. We have, therefore, investigated the thermal stability of various metal stacks with Cu films having Ta and TaN layers as diffusion barrier and/or as surface capping layers at temperatures from 400 to 700 °C.[4] Two distinct systems have been studied: asymmetric with Ta on one side and TaN on the other, and symmetric with either Ta or TaN on both sides. For the asymmetric systems, we have found that Ta is released from the Ta layer and moves through the Cu film to react with the TaN layer at the opposite interface via the Cu grain boundaries (GBs) after annealing at 500 °C or above.[4,5] Without a capping layer, Ta is also released from the Ta barrier layer and diffuses up to the Cu surface, most likely driven by oxidation of Ta and surface passivation of Cu by Ta.[4,5] For the symmetric systems, no Ta diffusion could be inferred from sheet resistance measurement.[4] Since Ta cannot be released from the stable TaN, the Cu/TaN interface would stay intact after annealing. This was confirmed with samples of Cu on TaN without any capping layer.[4,5] For Ta on both sides of the Cu film, lack of a driving force could explain the absence of Ta diffusion. Instead, protrusion of Ta into Cu was found to occur at 600 °C and above by means of cross-sectional transmission electron microscopy (TEM).[6]

Electromigration (EM) represents a critical reliability issue important for any integrated device or circuit. Electromigration may cause instability in, and eventually failure of, the interconnects. It usually involves complex failure mechanisms.[1–3,7] Defect formation and evolution under high-current density stressing is an essential factor. Electromigration in Cu interconnect formed according to the damascene concept has been extensively studied and is well documented in the literature.[8] But less information is available regarding the role of the commonly used TaN and Ta liner materials when it comes to integrity and reliability of the Cu interconnect.[9,10] The purpose of this work is to elucidate the pros and cons of Cu films stacked by these materials with respect to resistance to EM and electrical integrity at elevated temperatures. In order to shed some light on the role of interfaces, we focus on both symmetrically and asymmetrically layered systems, i.e., TaN/Cu/TaN and TaN/Cu/Ta, respectively. In the symmetric case, the possible presence of Ta in the Cu GBs and at the interfaces is avoided. Our results show that the latter stack with Ta as a barrier is more robust in resisting EM. This improvement is inferred to be the result of Ta diffusion into and through the Cu film up to the Cu–TaN interface. Our findings indicate that the choice of barrier has a strong impact on the reliability of the Cu interconnect.

II. EXPERIMENT

Two sets of samples were prepared, both employing blanket, (100)-oriented, p-type Si wafers with a 550 nm thick thermally grown SiO_2 film as the substrate. For material studies, four different metal stacks were deposited consecutively without breaking vacuum in a pulsed-DC mode Von Ardenne sputter system. They shared the same layer configuration with a 100 nm Cu film sandwiched between a 50 nm Ta or TaN barrier layer and a 50 nm Ta or TaN capping

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layer. The base pressure in the deposition chamber was below 10^{-4} Pa. To investigate the relation between thermal and electrical stability, samples were annealed in a vacuum chamber with the base pressure below 1.3×10^{-5} Pa. Samples were annealed from 400 to 800 °C, each temperature for 60 min. The composition, thicknesses, and interfacial reactions of as-deposited and the subsequently annealed samples were characterized by means of Rutherford backscattering spectrometry (RBS) with 2 MeV He^+ ions at a backscattering angle of 170°. Cross-sections of the as-deposited and annealed samples were studied using TEM. Sheet resistance was measured using a four-point probe as a first attempt to survey possible reactions involving Cu.

For the EM test structures, each configured as a standard four-terminal resistor, two metal stacks TaN/Cu/Ta and TaN/Cu/TaN were deposited with the aforementioned parameters. The barrier (Ta or TaN) and cap (TaN) layers were 50 nm thick and the Cu films 300 nm. The test structures were patterned by ion milling in combination with photolithography. The designed resistor line widths ranged from 2 to 20 μm while the lengths varied from 200 to 800 μm. Both patterned metal stacks were annealed at 600 °C for 60 min in a vacuum furnace. Unannealed structures were kept as references. Finally, the structures were passivated with a 200 nm thick SiN_x layer prepared by means of plasma-enhanced chemical vapor deposition (PECVD) at 300 °C. Contact openings, 200 × 200 μm in size, were lithographically defined and dry-etched. In the openings, a Pd layer, approximately 500 nm thick, was subsequently deposited on the TaN surface by means of evaporation. The contact pads were defined by lift-off technique. Variation of the resistance of the resistors was measured under thermal and electrical stresses on a probe-station (Karl Süss PM8) equipped with a hot-chuck (Temptronic TP0315). This was performed using an HP 4142B parameter analyzer equipped with a high power (current–voltage) module 41420A. The system was controlled by a PC using METRICS ICS software. Failed Cu interconnect wires, as a result of EM, were inspected using scanning electron microscope (SEM).

III. RESULTS AND DISCUSSION

The experimental results will be presented in two separate subsections. Variation in sheet resistance, R_s, of the four blanket layer stacks with temperature is first analyzed with the support of microscopic and spectrometric data for interface morphology. Attention is then directed to the patterned test structures for the EM performance of the layer stacks in real-time at elevated temperatures.

A. High-temperature behavior of the metal stacks

The measured R_s for the four blanket metal stacks is plotted in Fig. 1(a) at different annealing temperatures. The thinner Cu films of 100 nm thickness, instead of 300 nm, facilitated analysis and interpretation of Ta diffusion across the Cu films based on RBS and R_s data.[3] It is found that R_s for all samples first decreases with increasing annealing temperature up to 400–500 °C due to grain growth of Cu.[5] Further increase in temperature above 600 °C shows an appreciable increase in R_s by up to 20%–30% for the asymmetric combinations Ta/Cu/TaN and TaN/Cu/Ta. In contrast, only small changes in R_s are evident for the symmetric combinations Ta/Cu/Ta and TaN/Cu/TaN even after annealing at 800 °C. Our previous results indicate a massive Ta transport

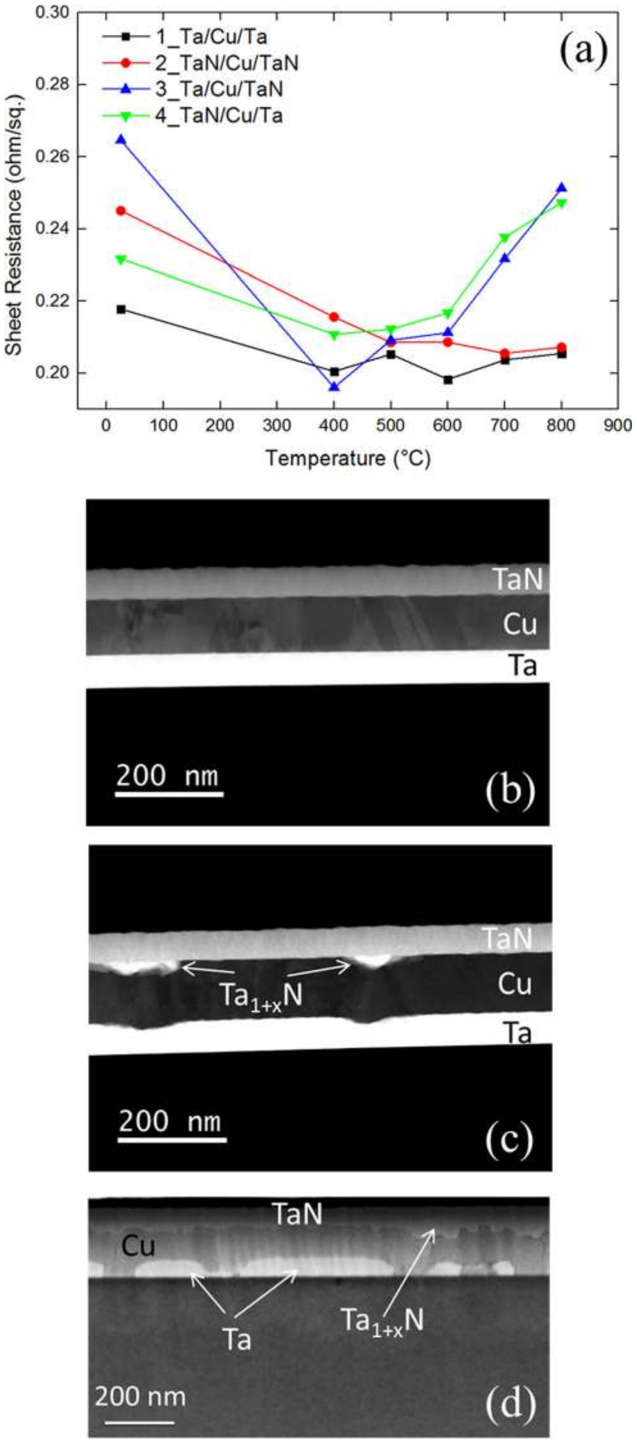

FIG. 1. (Color online) (a) Sheet resistance of the four different blanket metal stacks measured at various annealing temperatures. Cross-sectional TEM micrographs of the TaN/Cu/Ta structure: as-deposited (b), after annealing at 600 °C (c) and 700 °C (d) for 60 min.

from the Ta layer through the Cu film to react with and transform the TaN on the other side of the Cu films to $Ta_{1+x}N$.[4] As can be inferred from the R_s data for the Cu/Ta sample without any cap,[4] segregation of the Cu GBs with the in-diffused Ta can lead to an increase in R_s by about 10%. Morphological evolutions with the layer stacks associated with the Ta diffusion may also cause R_s to increase in the asymmetric combinations; the cross-sectional STEM micrographs show clear changes with the layer structure at 600 °C, cf. Fig. 1(c), but severe ones at 700 °C, cf. Fig. 1(d), with reference to the as-deposited case, cf. Fig. 1(b). Grain growth in Cu, causing the initial R_s drop, is clearly visible for the sample after annealing at 600 °C, in comparison with the as-deposited one. Such a grain growth was also observed in the symmetric combinations including both TaN/Cu/TaN and Ta/Cu/Ta (results not shown) as well as in Cu films without any cap.[11] Apart from grain growth leading to a clearly discernable difference in grain structure, no other morphological change in the symmetric combination TaN/Cu/TaN could be concluded from RBS analysis even after annealing at 700–800 °C;[4] thus, this symmetric combination is especially interesting for the EM studies below.

B. Characterization of EM test structures

In the light of the above observations with respect to Ta diffusion and R_s variation, our choice of samples for EM studies below is confined to the symmetric TaN/Cu/TaN and asymmetric TaN/Cu/Ta metal stacks. Furthermore, in order to minimize possible grain growth effects during the EM studies, the samples were first annealed at 600 °C. In addition to grain growth, annealing at 600 °C also causes Ta to diffuse through the Cu film toward the TaN cap in the asymmetric combination,[4] thereby causing the TaN to change into $Ta_{1+x}N$.[4] Both Cu surfaces will thus be in touch with Ta-rich films. The reference structures, without the 600 °C anneal, only received an unintentional 300 °C heat treatment during the PECVD SiN_x passivation, a temperature too low to expect measurable movement of Ta to occur in the Cu films. This allows us to isolate the effects of grain growth and Ta penetration on the resistance to EM.

In order to ascertain that a constant current density was attained for a sensible comparison, the actual line width was determined. This was achieved by examining the line resistance for 400 and 800 μm long lines with intermediate potential sensing terminals. For each line length, seven different line widths from 2 to 20 μm were included. The Cu film thickness was 300 nm in all cases. The measurements were carried out on all four samples at room temperature (RT) with a low current in order to avoid Joule heating. The results showed that the width deviation, ΔW, for the TaN/Cu/Ta and TaN/Cu/TaN reference samples were $\Delta W = -0.69$ and -0.54 μm, respectively. For the TaN/Cu/Ta and TaN/Cu/TaN 600-°C-annealed samples, the extrapolated ΔW were -0.47 and -0.83 μm, respectively.

The device-under-test itself was used to monitor the actual temperature during the EM stress testing caused by excessive Joule heating.[12] The hot chuck was set at different temperatures ranging from RT up to 350 °C. At each temperature, a low current of 2 mA was applied, so as to avoid Joule heating, to the line structure and the resistance value was recorded. An external thermometer attached to the wafer surface and close to the structure was used for accurate temperature calibration. Typical resistance versus temperature curves for the investigated structures are depicted in Fig. 2. These calibration curves were later used to find the real temperature of the resistor lines during EM stress testing. The respective temperature coefficient and RT resistivity of the measured structures are recapitulated in Table I. The observed data are in close agreement with reported values.[13]

C. Electromigration in Cu interconnects at elevated temperatures

The good EM robustness of Cu interconnect necessitates highly accelerated tests to obtain the results within acceptable time frames.[14] During the EM measurement, the current density was kept constant at 12 MA/cm^2 (adjusted according to the measured line width deviations) while the chuck/substrate temperature was varied from 250 to 350 °C. The measurement started with a low current to first monitor the line resistance at a given temperature whereupon the current level was ramped up to the final stress level of 12 MA/cm^2. The resulting line-resistance value, due to excessive heating, was recorded after a short stabilization period. This resistance value was compared with the calibration data and used to determine the actual stress temperature of the device. The stress was terminated when the line-resistance showed a 10% increase, since this was used as a failure criterion.[15]

At the current density of 12 MA/cm^2, the TaN/Cu/Ta structure was found to be more robust than its TaN/Cu/TaN counterpart. For instance, the TaN/Cu/Ta structure measured at 300 °C could survive for about three times longer than a similar TaN/Cu/TaN structure. Two typical resistance-versus-time traces at this temperature, one for TaN/Cu/Ta and one for TaN/Cu/TaN, are shown as a linear-log plot in Fig. 3 for

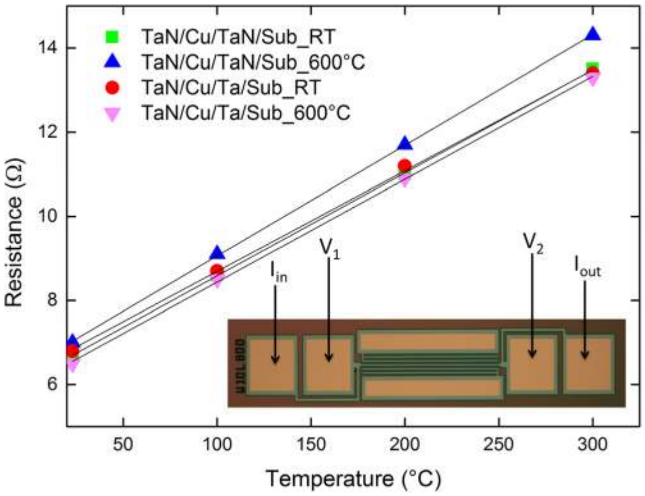

FIG. 2. (Color online) Temperature calibration curves with the extracted parameters in Table I, with the four-terminal measurement structure shown as inset.

TABLE I. Temperature coefficient, α, and RT resistance, R_0, of the TaN/Cu/TaN and TaN/Cu/Ta stacks for EM stressing studies, extracted in accordance to the definition $(R - R_0)/R_0 = \alpha \times (T - T_0)$ with R_0 as the resistance at room temperature T_0.

Sample	RT resistance, R_0 (Ω)	Temperature coefficient, α (1/°C)
TaN/Cu/TaN, RT	6.7	3.7×10^{-3}
TaN/Cu/TaN, 600 °C	7.0	3.8×10^{-3}
TaN/Cu/Ta, RT	6.8	3.5×10^{-3}
TaN/Cu/Ta, 600 °C	6.5	3.8×10^{-3}

comparison. The SEM micrographs of failed TaN/Cu/Ta and TaN/Cu/TaN lines are shown as insets.

The recorded data for the four investigated interconnect combinations, two references without intentional heat treatment and two after the 600 °C anneal, are depicted in Fig. 4 in the form of a lognormal plot of time-to-failure (TTF) characteristics. A linear fit to the curves in the graph gives the values for mean TTF (MTF) and lognormal sigma summarized in Table II. The improvement in EM endurance by the anneal at 600 °C can be explained by recourse to the current model for EM.[16] Thus, for Cu at temperatures below half of the melting point, i.e., below about 400 °C, the Cu atoms involved in the EM failure are transported along the surface where there is an ample supply of vacancies. These vacancies are more or less unperturbed by the presence of a surface layer of TaN since the interaction between TaN and Cu is rather weak, as attested to by adhesion and wetting experiments on such interfaces.[17,18] In fact, the adhesion strength between TaN_x and Cu has been found to decrease with increasing nitrogen concentration.[19] When the temperature is increased to 600 °C, the thermal energy is large enough to allow for a rapid rearrangement of the atoms and vacancies at the TaN/Cu interface. Although too small to be detectable by RBS, even after an 800 °C anneal,[4] it is also likely that the reactively sputter-deposited TaN layer is not exactly stoichiometric and will emit a small amount of Ta atoms. Tantalum is known to interact with a Cu surface[20,21] and can, therefore, be expected to interfere with the rearrangement of atoms at the Cu/TaN interface.

When larger amounts of Ta are present, as is the case at the Cu/Ta and $Cu/Ta_{1+x}N$ interfaces, the interaction is so strong that a very thin layer of amorphous Ta-Cu is formed.[20–22] Such a strong interaction will effectively block surface diffusion at the Cu/Ta interface. This interaction is probably initiated during the PECVD SiN_x step at 300 °C and is reflected already at RT in the form of the significantly improved EM resistance of the TaN/Cu/Ta interconnect without intentional heat treatment, as shown in Figs. 3 and 4. At 600 °C where the annealing was performed, the amorphization or Ta–Cu interaction at the Cu/Ta interface is fully developed.[11,20] As we have observed earlier,[4,5,11] the liberated Ta atoms will diffuse through the Cu film via the GBs in amounts readily detectable by RBS. In Cu, GB diffusion starts around half the melting point, i.e., around 400 °C. When at the Cu/TaN interface, these Ta atoms will strive to convert the TaN layer toward Ta_2N at

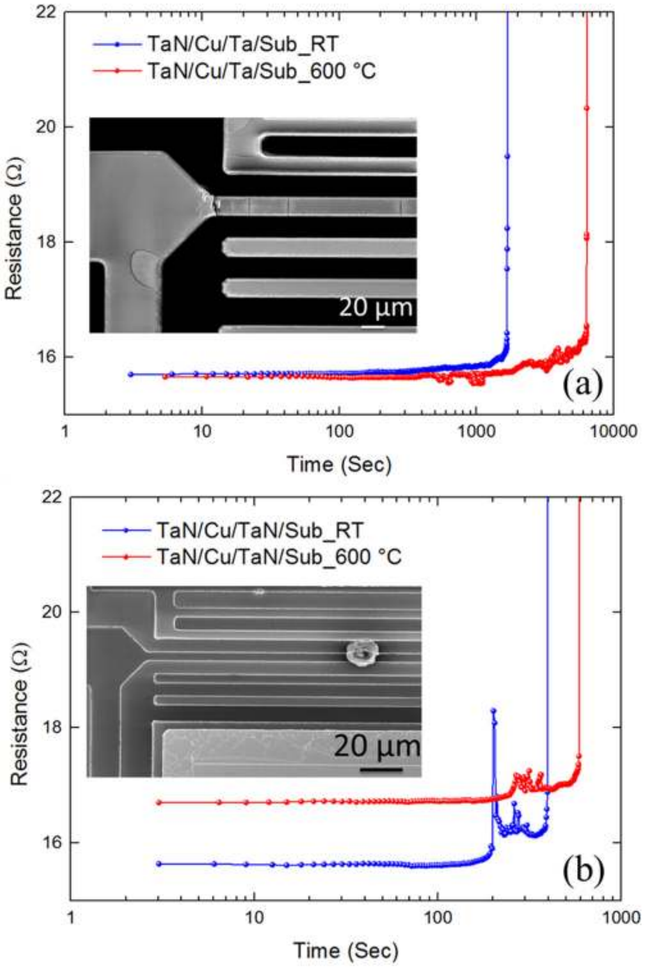

FIG. 3. (Color online) Representative resistance-vs-time traces for (a) TaN/Cu/Ta and (b) TaN/Cu/TaN both measured at 300 °C with a 12 MA/cm^2 current density, with the insets showing the failed lines for the RT cases. Note the 1-order-of-magnitude difference in scale in the x-axis between (a) and (b).

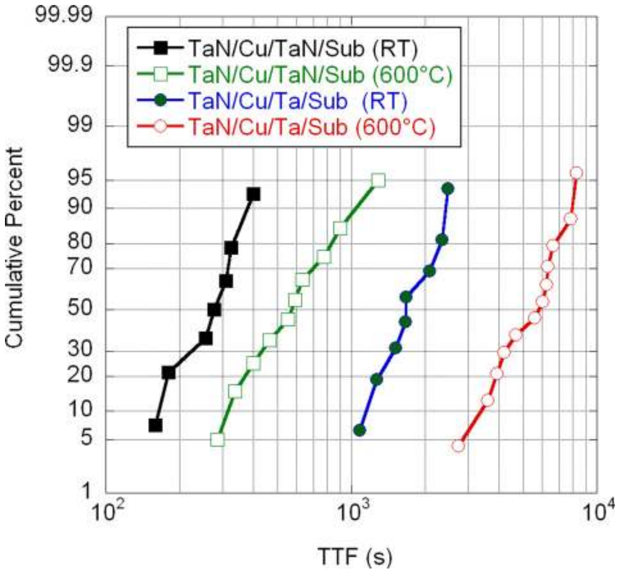

FIG. 4. (Color online) Plot of cumulative TTF for the four cases with TaN/Cu/TaN as-prepared, TaN/Cu/TaN 600 °C anneal, TaN/Cu/Ta as-prepared, and TaN/Cu/Ta 600 °C anneal.

TABLE II. MTF, lognormal sigma, and E_a for the four samples (Cu 5 μm width, 400 μm length, and 300 nm thickness) undergone the EM testing.

Sample	MTF (s)	Lognormal sigma	E_a (eV)
TaN/Cu/TaN, RT	3.1×10^2	0.13	—
TaN/Cu/TaN, 600 °C	5.7×10^2	0.15	0.47
TaN/Cu/Ta, RT	1.7×10^3	0.25	—
TaN/Cu/Ta, 600 °C	5.3×10^3	0.20	1.0

the interface, detected as $Ta_{1+x}N$ in Figs. 1(c) and 1(d). This enhanced interfacial interaction can slow down the interfacial atomic movement, thereby providing additional EM resistance, which is clearly observed in Figs. 3 and 4.

In order to shed more light on the importance of the Cu/TaN and Cu/Ta interfaces, we have determined the TTF activation energy, E_a, appropriate to the temperature range 200–400 °C for the two annealed cases. This was performed on Cu conductors that were 5 μm wide, 400 μm long, and 300 nm thick. The results for this configuration are given in Table II. Although we have not been able to find any published results for our particular layered geometry, our result for TaN/Cu/Ta is in accordance with published results for damascene structures, which are around 0.9 eV.[14] However, it should be kept in mind that in such structures the Cu conductor is surrounded on three sides by a Ta liner, whereas only one side faces Ta in our geometry. An activation energy of 1.4 eV for damascene Cu conductors in contact with Ta on all four sides is also available in the literature.[10] The activation energy for TaN/Cu/TaN is remarkably low, on the other hand. We have not been able to find any result for similar configurations in the literature. It should be kept in mind, though, that the fact that there are not only one, but two weakly interacting Cu/TaN interfaces in itself will lower the activation energy for the overall EM process, by referring to the discussion above.

IV. CONCLUSIONS

We have investigated the high-temperature behavior of four different Cu-based interconnect schemes with Ta or TaN as the cap and/or barrier. Electrically and morphologically similar, the TaN/Cu/Ta stack seems to have a better electromigration performance with higher activation energy and longer lifetime than its TaN/Cu/TaN counterpart. Interfacial characteristics in term of atomic interaction and diffusion are discussed as the root cause for this difference.

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