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Research Article

Electronically Tunable Differential Integrator: Linear Voltage Controlled Quadrature Oscillator

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A new electronically tunable differential integrator (ETDI) and its extension to voltage controlled quadrature oscillator (VCQO) design with linear tuning law are proposed; the active building block is a composite current feedback amplifier with recent multiplication mode current conveyor (MMCC) element. Recently utilization of two different kinds of active devices to form a composite building block is being considered since it yields a superior functional element suitable for improved quality circuit design. The integrator time constant (τ) and the oscillation frequency (ω_o) are tunable by the control voltage (V) of the MMCC block. Analysis indicates negligible phase error (θ_e) for the integrator and low active ω_o-sensitivity relative to the device parasitic capacitances. Satisfactory experimental verifications on electronic tunability of some wave shaping applications by the integrator and a double-integrator feedback loop (DIFL) based sinusoid oscillator with linear f_o variation range of 60 KHz~1.8 MHz at low THD of 2.1% are verified by both simulation and hardware tests.

1. Introduction

Dual-input integrators with electronic tunability are useful functional components for numerous analog signal processing and waveforming applications [1]. A number of single and dual-input passive tuned integrators using various active building blocks are available [2, 3].

However, integrators with electronically adjustable time constant (τ) find some exclusive applications [4–6], for example, in electronically tunable biquadratic phase selective filter design [7], as electronic reset controller and phase compensator [8] for process control loops.

Quadrature sinusoid oscillators are widely used in orthogonal signal mixers, in PLLs and SSB modulators; some such oscillators based on various active devices, for example, voltage operational amplifier-VOA [9], CFOA [10, 11], CDBA [12, 13], CDTA [14], DDCC [15], CCCCTA [16], OTA [17], and DVCCTA [18, 19], are reported.

Here we present a simple electronically tunable dual-input integrator (ETDI) topology based on a composite current feedback amplifier- (CFA-) multiplication mode current conveyor (MMCC) building block. It has been pointed out in the recent literature [20, 21] that utilization of two different kinds of active elements to form a composite building block yields superior functional result in analog signal processing applications.

Hence the topic of quadrature sinusoidal oscillator design and implementation with better quality is receiving considerable research interest at present. A number of such oscillators using various active building blocks [9–17] are now available. Here, we present a new simple ETDI topology, based on a composite CFA-MMCC building block with grounded capacitor; subsequently, a double-integrator feedback loop (DIFL), with one inverting and the other noninverting, is utilized to design a linear VCQO wherein a pair of grounded *RC*-section selects the appropriate signal generation band

and the control voltage (V) of the MMCC tunes oscillation frequency (f_o) linearly; no component matching constraint is involved here. This current conveyor element is quite an elegant building block with a dedicated control voltage (V) terminal; hence the MMCC is a versatile active component suitable for electronically tunable function circuit design.

It is seen in recent literature that such linear VCQO is a useful functional block which finds wide range of applications in emerging fields; namely, in certain telemetry-related areas it could convert a transducer voltage to a proportional frequency which is then modulated for subsequent processing [22], as quantizer for frequency-to-digital or time-to-digital conversion [23] and also as the spectrum monitor receiver [24] in cognitive radio communication studies.

Here, we present the design and realization of a new linear VCQO using the composite type active device; analysis shows that device imperfections, namely, port tracking errors ($|\varepsilon| \ll 1$) and parasitic capacitors ($C_{z,m}$) at current source nodes, yield negligible effects on the nominal design, whereby the active-sensitivity figures are extremely low. Experimental measurements by simulation and hardware tests on the proposed design indicate satisfactory results with f_o-tunability in the range 60 KHz–1.8 MHz following the variation of a suitable control voltage ($1 \le V(\text{d.c.volt}) \le 10$) wherein a desired band-spread may be selected by appropriate choice of the grounded RC components [25], without any component matching constraint, even with nonideal devices.

2. Analysis

The ETDI topology is shown in Figure 1(a); the nodal relations of the active blocks are $i_z = \alpha_1 i_x$, $v_x = \beta_1 v_y$, $E = \delta_1 v_z$, and $i_y = 0$ for the CFA and $i_z = \alpha_2 i_x$, $v_x = \beta_2 kEV$, $v_o = \delta_2 v_z$, and $i_{y1} = 0 = i_{y2}$ for the MMCC where $k(= 0.1/\text{volt})$ is multiplication constant [12] and V is control voltage. The port transfer ratios (α, β, and δ) are unity for ideal elements; the imperfections may be postulated in terms of some small error coefficients ($.01 \le |\varepsilon| \le .04$) as $\alpha \approx (1 - \varepsilon_i)$, $\beta \approx (1 - \varepsilon_v)$, and $\delta \approx (1 - \varepsilon_o)$. Also, shunt-$rC$ parasitic components appear [26–28] at the z-node of the blocks having typical values in the range of $3\,\text{pF} \le C_{z,m} \le 6\,\text{pF}$ and $2\,\text{M}\Omega \le r_{z,m} \le 5\,\text{M}\Omega$; since resistance values used in the design are in KΩ ranges, their ratios to $r_{z,m}$ are extremely small and hence effects of $r_{z,m}$ are negligible in the design. It may also be mentioned that a low-value internal parasitic resistance ($r_x \approx 45\,\Omega$) appears in series with the current path at x-node of the devices; its effect can be minimized by absorbing r_x-value in the load resistors at these nodes. Routine analysis assuming $V_{\text{in}} = (\beta_1 V_2 - V_1)$ yields the open-loop transfer $F \equiv V_o/V_{\text{in}}$ in Figure 1(a) as

$$F = \frac{\mu n}{\{s\tau_o(1+m)+\eta\}\{(s\tau_z+1+\sigma)\}}, \tag{1}$$

where

$$\mu = \alpha_1\alpha_2\beta_2\delta_1\delta_2 \approx (1-\varepsilon_t),$$

$$\varepsilon_t = \varepsilon_{i1} + \varepsilon_{i2} + \varepsilon_{v2} + \varepsilon_{o1} + \varepsilon_{o2},$$

$$n = \frac{r_2}{r_1}, \qquad m = \frac{C_m}{C} \ll 1, \qquad \tau_z = C_z r_2,$$

$$\eta = \frac{R}{r_m} \ll 1, \qquad \sigma = \frac{r_2}{r_z} \ll 1,$$

$$\frac{\omega}{\omega_z} \ll 1; \quad \omega_z = \frac{1}{\tau_z},$$

$$\tau_o = \frac{10RC}{V}; \qquad k = 0.1\left(\text{volt}^{-1}\right). \tag{2}$$

It may be seen that effect of C_m may be compensated by absorbing its value in C since both are grounded [25], an attractive feature for microminiaturization. The noninverting input signal is also slightly altered; in practice, however, the deviation is quite negligible as we observed during the experimental verification.

The port errors alter the magnitude response slightly by a factor $(1 - \varepsilon_t)$; however, a phase error (θ_e) is introduced at relatively higher side of frequency $\omega_z(=1/\tau_z)$, given by $\theta_e = \arctan(\omega/\omega_z)$. Since $C_z \ll C$, $\omega/\omega_z \ll 1$; that is, $\theta_e \approx 0$; typical values [27] indicate that if $C_z \approx 4\,\text{pF}$, then $f_z \approx 41\,\text{MHz}$ with $r_2 \approx 1\,\text{K}\Omega$ (typical) which yields $\theta_e \approx 3^\circ$ at 2.5 MHz around the nominal phase of $\pi/2$. The quality factor (q) of the integrator is derived as $q \approx (1/\tan\theta_e) \gg 1$.

Hence, it is seen that the effects of device nonidealities are quite negligible; assuming therefore that $\varepsilon \approx 0$ and $r_2 = r_1$ for simplicity, we get the desired ETDI transfer (F) from (1) as

$$F \equiv \frac{V_o}{(V_2 - V_1)} = \frac{1}{s\tau_o}. \tag{3}$$

3. Linear VCQO Design

The proposed oscillator is designed with DIFL using the block diagram of Figure 1(b); neglecting port errors ($\varepsilon \approx 0$) in (1), we get the loop-gain ($F_o \equiv F_1F_2$) of the DIFL, assuming $m \ll 1$ and $n = 1$, as

$$F_o = -\left\{s^2\tau_{o1}\tau_{o2}(s\tau_{z1}+1)(s\tau_{z2}+1)\right\}^{-1}. \tag{4}$$

The MMCC block is shown in Figure 1(c).

Total phase shift (Φ) of loop-gain is

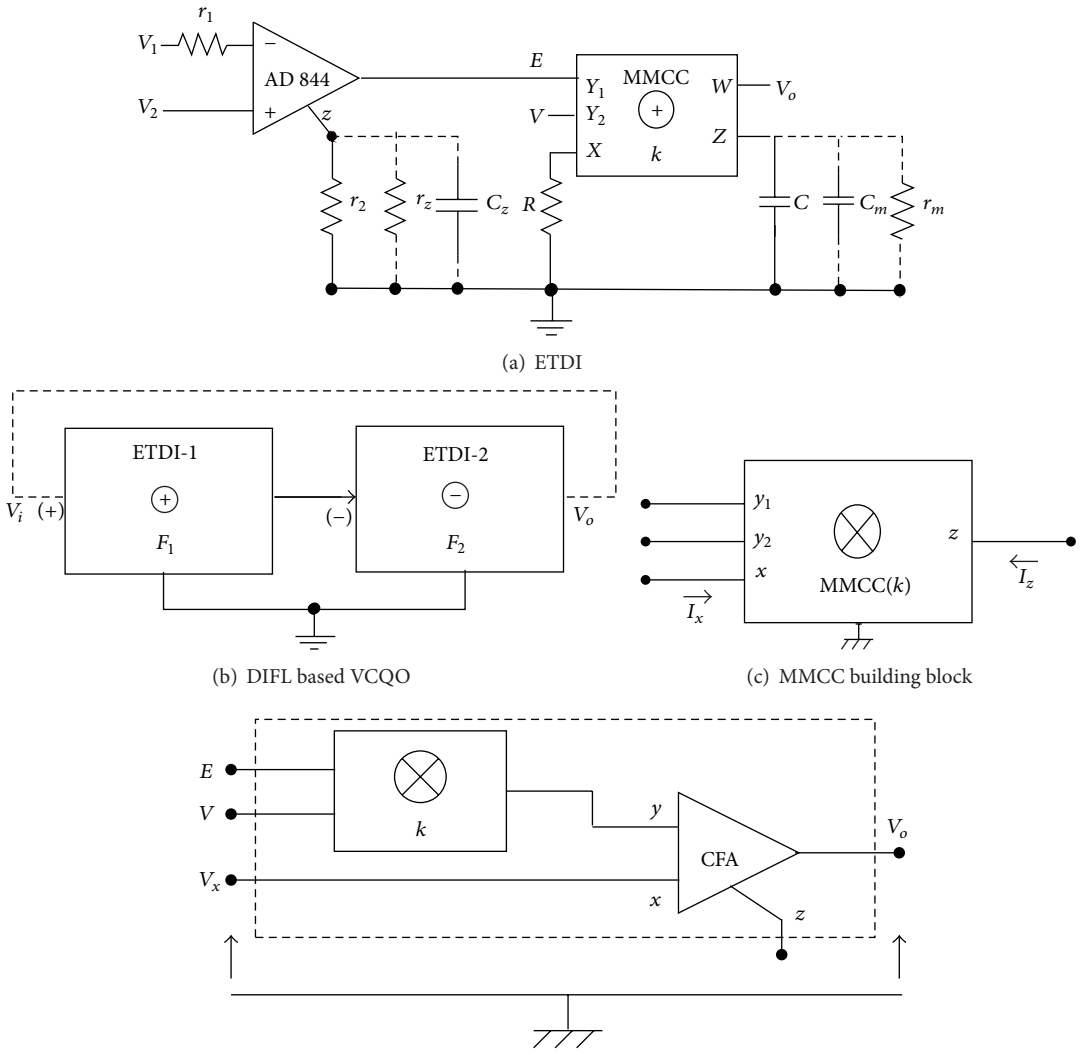
$$\Phi = \pi - \left[2\left(\frac{\pi}{2}\right) + \left\{\arctan\left(\frac{\omega}{\omega_{z1}}\right) + \arctan\left(\frac{\omega}{\omega_{z2}}\right)\right\}\right]. \tag{5}$$

The parasitic phase components are extremely low since the lossy capacitors ($C_{z,m}$) create distant pole frequencies compared to the usable frequency range; hence the input and output stimulus of the DIFL would be in same phase at unity gain and closure of loop incites sinusoid oscillations build-up; the corresponding characteristic equation is

$$\left(s^2\tau_{o1}\tau_{o2}+1\right) = 0 \tag{6}$$

which yields the oscillation frequency after putting $s \equiv j\omega$, as

$$\omega_o \equiv \frac{1}{\sqrt{\{\tau_{o1}\tau_{o2}\}}} = \frac{kV}{\left\{\sqrt{(R_1C_1R_2C_2)}\right\}}. \tag{7}$$



(a) ETDI

(b) DIFL based VCQO

(c) MMCC building block

(d) MMCC configured with a multiplier (k) and CFA

Figure 1: Proposed electronically tunable functional circuits.

With equal-value RC components and $k = 0.1$/volt, (7) yields $f_o = V/(20\pi RC)$; thus linear tunability of f_o is obtained by directly applying the control voltage (V) of MMCC unit. No additional g_m to current conversion circuitry as compared to previous realizations using OTA [14, 17] is required. The active ω_o-sensitivity is calculated as $S_{\varepsilon}^{\omega_o} = 0.5\varepsilon/(1-\varepsilon_t) \ll 0.5$. The frequency-stability (Ψ) is derived as $\Psi = 1$, using the relation $\Psi \equiv \{\Delta\Phi/(\Delta u)\}|_{u=1}$ where $u = \omega/\omega_o$.

4. Experimental Results

The proposed ETDI of Figure 1(a) is built with readily available ADF-844/846 type CFA device [28, 29]; since MMCC [30]-chip is not yet commercially available, we configured it [12, 31] as shown in Figure 1(d), with four-quadrant multiplier (ICL-8013 or AD-534) coupled with a current feedback amplifier (CFA) device (AD-844 or AD-846). The bandwidth of the CFA device is almost independent of the closed loop-gain at high slew rate values [28, 29]. This yields the element to be particularly advantageous for various signal processing/generation applications. Recently, reports on superior versions of the CFA element (OPA-695) have appeared [32] indicating very high slew rate (~2.5 KV/μs) and extended bandwidth (~1.4 GHz).

For the linear VCQO design, we formed the block diagram of Figure 1(b) using one inverting and another noninverting ETDI. The measured responses obtained by simulation and hardware tests are shown in Figure 2; linear V to f_o variation characteristics had been verified with $1 \le V$(d.c.volt) ≤ 10 which provided a satisfactory tuning range of up to about 1.8 MHz with appropriate choice of RC products.

Practical design responses of proposed circuits have been verified with both ICL-8013 and AD-534 type as multiplier

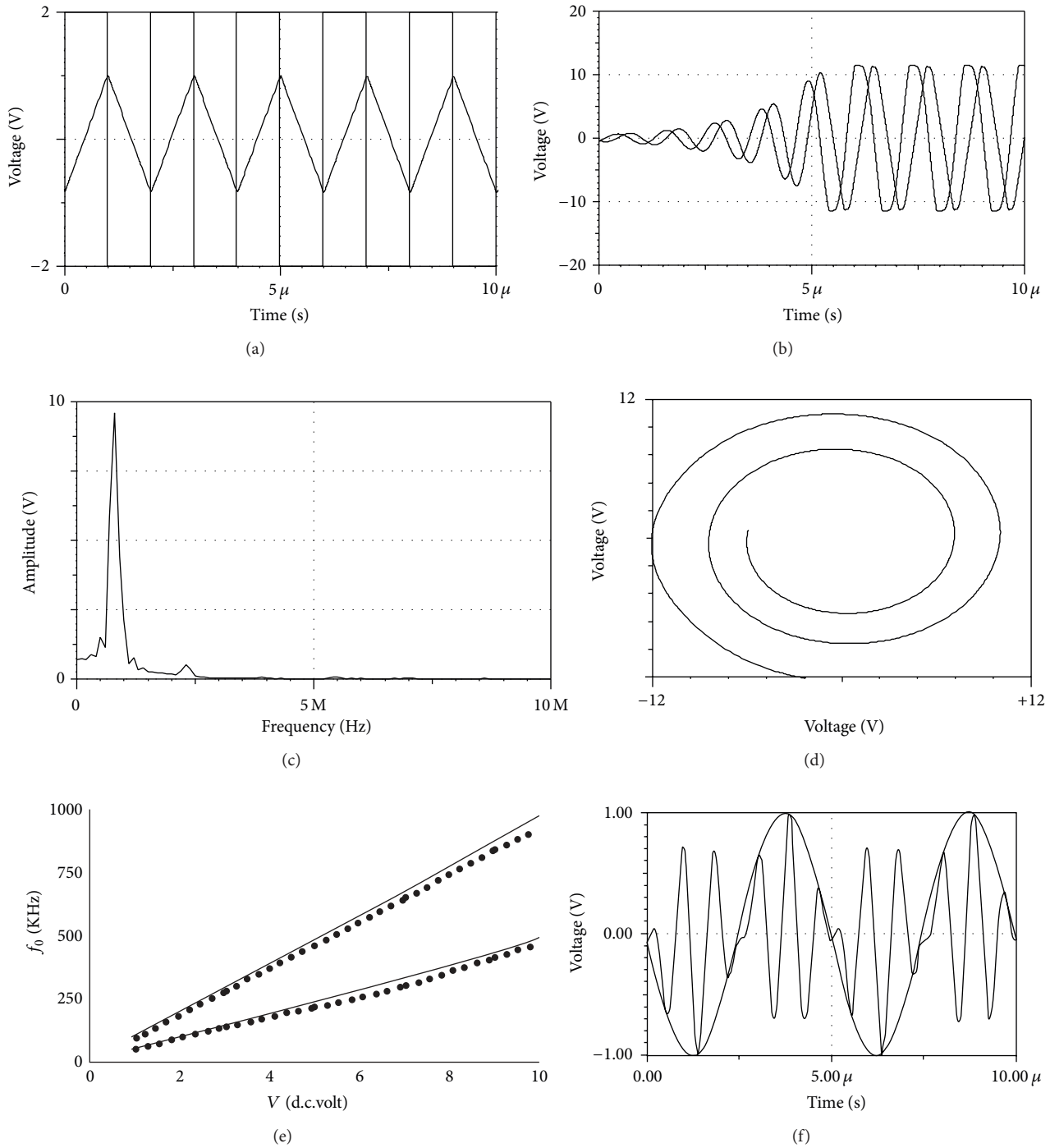


FIGURE 2: Test responses of proposed ETDI and linear VCQO. (a) Response of integrator with square wave input signals at 500 KHz: $V_2 = -V_1 = 2$ Volt(pp), $V = 5$ volt, $R = 1\,\text{K}\Omega$, and $C = 0.5\,\text{nF}$; measured $C_z \approx C_m \approx 4.2\,\text{pF}$ at $V_{cc} = 0 \pm 12$ V.d.c. (b) Quadrature oscillator response at the onset of sinusoidal wave build-up at 1.1 MHz with $R = 1\,\text{K}\Omega$, $C = 165\,\text{pF}$, and $V = 5$ volt. (c) Spectrum of the response in (b). (d) Lissajous pattern of quadrature signals. (e) VCQO tuning characteristics: dotted line: hardware test; firm line: simulation; band-spread selection: upper curve: $R = 1\,\text{K}\Omega$, $C = 165\,\text{pF}$; lower curve: $R = 1.5\,\text{K}\Omega$, $C = 220\,\text{pF}$. (f) Quadrature wave modulation: 1.2 MHz input signal $V_2 = 2$ Vpp to ETDI with $V_1 = 0$; control voltage = $V = 2$ Vpp at 200 KHz to MMCC.

elements, along with both AD-844 and AD-846 type CFA devices; satisfactory results with both sets of components had been verified. A comparative summary of some recent quadrature oscillator characteristics is described in Table 2.

5. Some Discussions

Keeping in view the measured responses, a few observations are presented here on functional unit to unit basis; this substantiates the accuracy and versatility of the proposed realization.

ETDI

(a) Voltage controlled time constant, either enhancement or tapering adjustment at dual input feature with grounded capacitor; typical time domain response shown in Figure 2(a) verifies the features.

(b) With sinusoid signals, 20 dB/decade frequency roll-off had been observed at 3.3 MHz onwards; measured CMRR $\approx$ 57 dB at $V_2 = -V_1$.

(c) Frequency domain phase error is measured as $\theta_e \approx 2.4^\circ$ at 2 MHz; adjustment of V for τ_o control did not affect this error. Also the ETDI is practically active-insensitive to port mismatch errors ($\varepsilon \ll 1$) [28, 33].

CFA-MMCC

(a) Availability of in-built control voltage node of MMCC adds flexibility to a designer; this feature is verified experimentally by generating a quadrature (integrated) wave modulation response as shown in Figure 2(f). This is a useful application of the CFA-MMCC based ETDI.

(b) Analysis shows that θ_e is dominantly caused by parasitic C_z of CFA device; another component of this error due to MMCC is negligible since $\theta_e(\text{MMCC}) \approx \arctan(\omega RC/\eta) \approx 0$ as $\eta \approx 10^3$.

Thus the overall phase error of $\angle F(\omega)$ could be limited to extremely low values for frequencies $\omega \ll \omega_z$, after selecting moderate values of r, while τ_o may be tuned by V; these two adjustments are noninteracting.

This substantiates the versatility of selecting a composite building block. Phase error had been measured as in Table 1, with $r = 1\,\text{K}\Omega$ and $C_z \approx 4\,\text{pF}$ (measured); that is, $f_z \approx 41$ MHz.

DIFL

(a) Two identical stages, with a common V terminal, are cascaded for DIFL topology having nominal phase output of 180°. Tested phase response compounded as $\theta_e(\text{DIFL}) \approx 5.5^\circ$ at 2 MHz. Loop was observed to be unable to build up oscillation beyond 2 MHz. Therefore parasitic elements tend to limit the usable range of $f_o \leq 2$ MHz.

Table 1

f (MHz)	1	2	3
θ_e°	1.2	2.4	3.6

VCQO

(a) Literature shows that albeit some quadrature oscillators were presented earlier, very few [10, 17] provide electronically tunable linear f_o tuning law. These designs are based on electronic tuning by a bias current (I_b) that is replicated from g_m which requires additional current processing circuitry/hardware consuming extra quiescent power; moreover such g_m-to-I_b conversion involves thermal voltage [18] and hence temperature sensitivity issues. In view of these comparative attributes, the proposed design appears to be superior.

6. Conclusion

The realization and analysis of a new ETDI and its applicability to the design of linear VCQO using the CFA-MMCC composite building block are presented.

The effects of the device imperfections are examined which are seen to be quite negligible as indicated by low phase and magnitude deviations. The linear V-to-f_o tuning characteristics had been experimentally verified in a range of 60 KHz–1.8 MHz with good quality low distortion sine-wave generation response. It may be mentioned that here the linear f_o tuning feature is obtained by the simple and direct application of the same control voltage (V) to the appropriate terminal of the MMCC building blocks for the two ETDI stages. Additional current processing circuitry for g_m –to-bias current (I_b) conversion and its associated hardware complexity with additional quiescent power requirement would not be needed as compared to previous OTA based electronically tunable realizations; moreover, this conversion involves thermal voltage (V_T) that may ensue temperature sensitivity issue [18]. Also, use of the superior quality devices [28, 32] in the proposed topology is believed to exhibit low distortion generation at extended range of frequencies. A comparative study of similar designs, presented in a concise table, indicates the superiority of the proposed implementation.

As further study, we plan to utilize the linear VCQO for some cognitive radio spectrum assessment applications after translating the proposed design using suitable building blocks with appropriate high frequency specification.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

Table 2: Comparative summary on the characteristics of some recent quadrature oscillators.

Reference	Device used	Electronic tunability	f_o (KHz) reported	Linear tuning law	THD (%)
[9]	VOA	No	160	No	No mention
[10]	CFA	Yes	80	Yes	2.0
[12]	CDBA	Yes	900	No	3.1
[11]	CFOA	No	159	No	3.16
[14]	CDTA	Yes	1730	No	3.0
[15]	DDCC	No	1060	No	No mention
[16]	CCCCTA	Yes	1100	No	1.15~2.94
[13]	CDBA	No	16	No	1.94
[17]	OTA	Yes	64	Yes	No mention
[18]	DVCCTA	Yes	348	No	4.66
[19]	DVCCTA	Yes	3183	No	No mention
Proposed	CFA-MMCC	Yes	1800	Yes	2.1

Frequency stability $\Psi = 1$ in proposed design; also reported $\Psi = 1$ in [10]; no mention of Ψ in other references above.

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