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Research Article

Electronically Tunable Quadrature Sinusoidal Oscillator with Equal Output Amplitudes during Frequency Tuning Process

Den Satipar,[1] Pattana Intani,[1] and Winai Jaikla[2]

[1]*Department of Electrical Engineering, Faculty of Engineering, Pathumwan Institute of Technology, Bangkok 10330, Thailand*
[2]*Department of Engineering Education, Faculty of Industrial Education and Technology, King Mongkut's Institute of Technology Ladkrabang, Bangkok 10520, Thailand*

Correspondence should be addressed to Winai Jaikla; winai.ja@hotmail.com

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A new configuration of voltage-mode quadrature sinusoidal oscillator is proposed. The proposed oscillator employs two voltage differencing current conveyors (VDCCs), two resistors, and two grounded capacitors. In this design, the use of multiple/dual output terminal active building block is not required. The tuning of frequency of oscillation (FO) can be done electronically by adjusting the bias current of active device without affecting condition of oscillation (CO). The electronic tuning can be done by controlling the bias current using a digital circuit. The amplitude of two sinusoidal outputs is equal when the frequency of oscillation is tuned. This makes the sinusoidal output voltages meet good total harmonic distortions (THD). Moreover, the proposed circuit can provide the sinusoidal output current with high impedance which is connected to external load or to another circuit without the use of buffer device. To confirm that the oscillator can generate the quadrature sinusoidal output signal, the experimental results using VDCC constructed from commercially available ICs are also included. The experimental results agree well with theoretical anticipation.

1. Introduction

Quadrature sinusoidal oscillators are very important circuits in numerous applications such as communication, sound system, instrumentation, control system. Especially in modulation system, the quadrature oscillator is used to generate the carrier signal for quadrature amplitude modulation (QAM) and single-sideband modulation (SSB) [1, 2]. Most of sinusoidal oscillator designs required the following features: low THD of the quadrature sinusoidal output, independent control of frequency of oscillation (FO) and condition of oscillation (CO) [3], using minimum number of active and passive element [4], electronic controllability [5] and so on. However, the amplitude of quadrature sinusoidal output should be considered too. To avoid the use of external amplifier, the expected amplitude of quadrature output should be equal for all frequency or during tuning FO.

The design of electronic circuit in analog signal processing has been emphasized in the use of active building block [6–8]. Particularly, the electronically tunable active building blocks have attracted significant research attention since analog circuits using electronically tunable active building block give more fine-tuning than adjusting the value of passive device. The voltage differencing current conveyor (VDCC) [9, 10] is a recently reported versatile active building block used in the realization of analog signal processing circuits. VDCC is also attractive due to its capability of electronic controllability. The analog circuits using VDCC as active element have been found in the literature, for examples, universal filter [11–14], first-order all-pass filter [15], ladder filter [16], passive element simulator [10, 17–21], and square and triangular wave generator [22]. The VDCC-based sinusoidal oscillators have been proposed in [19, 23–26]. In [19], the Colpitts oscillator using VDCC-based capacitance multiplier was proposed. In this oscillator, the FO and CO can be independently tuned. It can provide quadrature output waveform but the amplitude of quadrature output voltage is not equal during tuning the frequency. Also it requires dual output terminal VDCC (W_n and W_p terminal). The simple current-mode oscillator using single

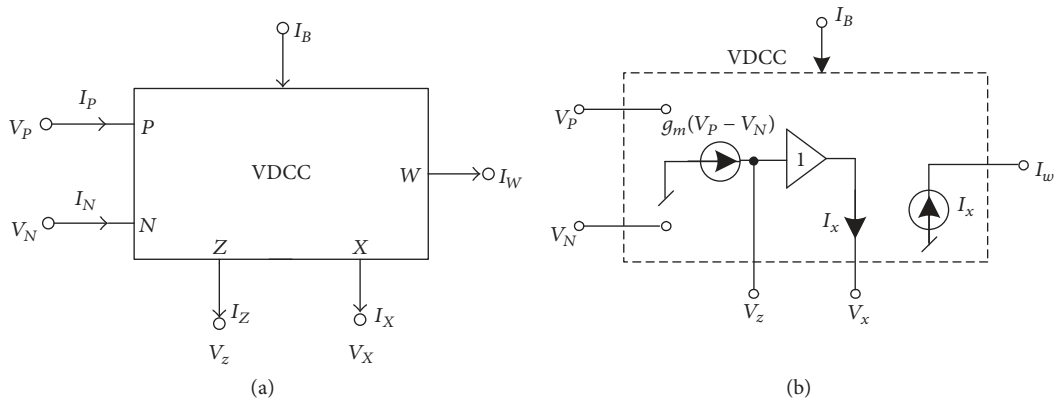

Figure 1: VDCC: (a) circuit symbol of VDCC; (b) equivalent circuit.

VDCC and grounded passive elements was presented in [23]. The FO and CO can be orthogonally controlled. The current-mode quadrature sinusoidal waveform is obtained. However, the FO cannot be electronically tuned without affecting CO. Also the amplitude of quadrature output waveform is not equal during tuning the frequency. The simple voltage-mode quadrature oscillator using single VDCC, two grounded resistors, and two grounded capacitors was implemented in [24]. The FO and CO can be orthogonally controlled. The FO can be electronically tuned without affecting the CO. However, the amplitude of quadrature output waveform is not equal during tuning the frequency. In [25], the quadrature oscillator using two VDCC, two grounded resistors, and two grounded capacitors was presented. The FO and CO can be independently/electronically controlled. However, the amplitude of quadrature output waveform is not equal during tuning the frequency. In [26], the quadrature oscillator using single controlled gain VDCC (CG-VDCC) and two grounded capacitors was presented. The FO and CO can be independently/electronically controlled. However, the amplitude of quadrature output waveform is not equal during tuning the frequency. Also the internal construction of CG-VDCC using the commercially available ICs is quite complicated.

The idea behind this work is to present the quadrature sinusoidal oscillator emphasized on the use of VDCC as active element. The amplitude of quadrature output waveform is equal during tuning of frequency. Also, the frequency of oscillation can be electronically tuned without affecting the condition of oscillation.

2. Proposed Circuit and Operation

2.1. Voltage Differencing Current Conveyor (VDCC). In this design, the active building block (ABB) called voltage differencing current conveyor (VDCC) is used as main active device. The international construction of CMOS VDCC was proposed by Kaçar et al. [10] in 2014. It is five-port device, namely, P, N, Z, X, and W port. The high impedance voltage input ports are P and N. The high impedance current output ports are Z and W port. The low impedance voltage output port is X port. In the original version of VDCC the output current at W port provides the output current both positive and negative direction called W_n and W_p ports. However, in this purpose, only single W port is required. This can reduce the current tracking error at W port and can reduce the number of transistor in VDCC. The electrical symbol and equivalent circuit of VDCC are shown in Figure 1. The ideal electrical properties of VDCC are shown in

$$\begin{bmatrix} I_N \\ I_P \\ I_Z \\ V_X \\ I_{WP} \\ I_{WN} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \\ I_X \end{bmatrix}, \tag{1}$$

where g_m is the transconductance gain. For CMOS VDCC, g_m is controlled by DC bias current I_B as follows:

$$g_m = \sqrt{I_B \mu_n C_{\text{ox}} \left(\frac{W}{L}\right)}, \tag{2}$$

where I_B is bias current, μ_n is mobility of the carrier for MOS transistors, C_{ox} is gate-oxide capacitance per unit area, W is effective channel width, and L is effective channel length, respectively. The internal construction of CMOS VDCC is shown in Figure 2 [10]. The VDCC can be constructed from commercially available ICs as shown in Figure 3. It consists of LM13700 [27] and AD844 [28]. This construction contains only single w terminal. g_m for this construction is given as

$$g_m = \frac{I_B}{2V_T}, \tag{3}$$

where V_T is the thermal voltage.

2.2. Proposed Oscillator. The proposed oscillator consists of two VDCCs, two resistors, and two grounded capacitors. The quadrature output voltages V_{o1} and V_{o2} are the voltage dropped at Z port of VDCC1 and VDCC2, respectively.

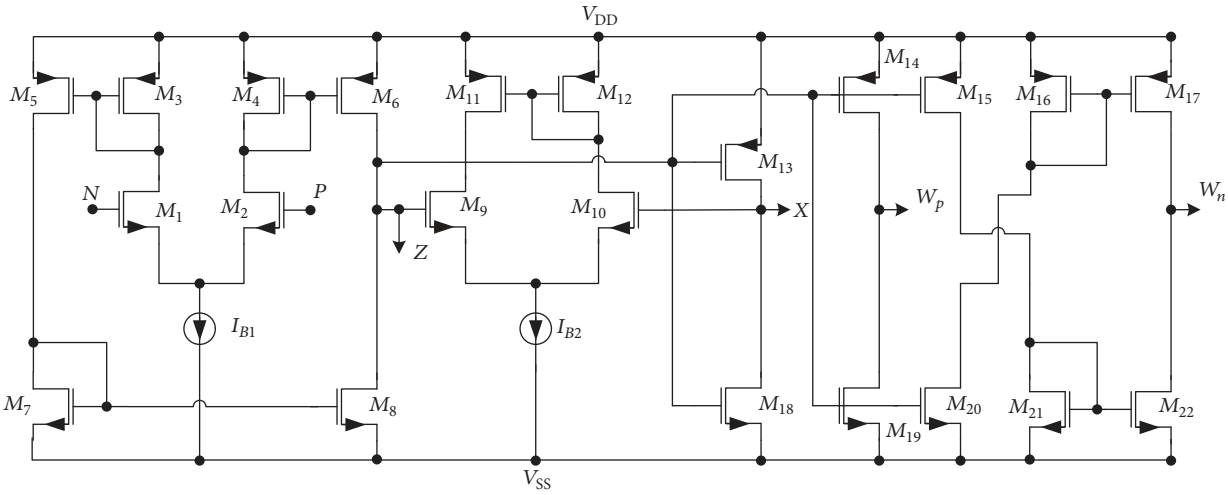

Figure 2: Internal construction of CMOS VDCC [10].

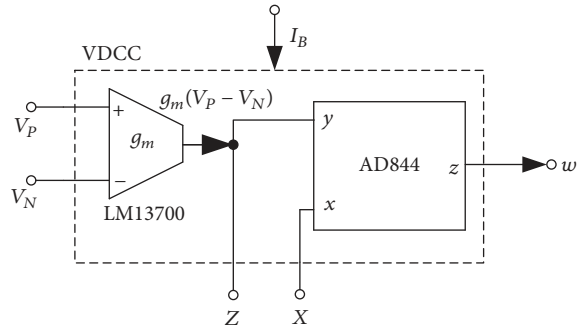

Figure 3: VDCC (without dual W terminal) constructed from commercially available ICs.

However, the output voltages are taken from the non-low-impedance output nodes, so the voltage buffers are needed for cascading. The output current I_O with high impedance flows from W port of VDCC2. Taking into consideration the ideal port characteristics involved in VDCC as referred above (2) and the relevant notations appearing in Figure 4, the characteristic equation is as follows:

$$s^2 + s\left(1 - \frac{R_2}{R_1}\right)\frac{g_{m1}}{C_1} + \frac{R_2 g_{m1} g_{m2}}{R_1 C_1 C_2} = 0. \tag{4}$$

From (4), the frequency of oscillation is given as

$$\omega_0 = \sqrt{\frac{R_2 g_{m1} g_{m2}}{R_1 C_1 C_2}}. \tag{5}$$

Subsequently, the condition of oscillation is given as

$$R_2 \geq R_1. \tag{6}$$

It is evident from (5) and (6) that the frequency of oscillation can be controlled by g_{m1} and g_{m2} without affecting the condition of oscillation. Moreover, the frequency of oscillation can be electronically tuned via g_{m1} and g_{m2}. If $R_2 \cong R_1$, the frequency of oscillation is rewritten as

$$\omega_0 = \sqrt{\frac{g_{m1} g_{m2}}{C_1 C_2}}. \tag{7}$$

From the circuit in Figure 4, the voltage ratio of V_{o1} and V_{o2} is as follows:

$$\frac{V_{o2}}{V_{o1}} = \frac{g_{m2}}{sC_2}. \tag{8}$$

It is found from (8) that the output voltages V_{o2} and V_{o1} are 90-degree phase difference which is called quadrature signal. The phase of output voltage V_{o1} leads the phase of output voltage V_{o2} to 90 degrees. At frequency of oscillation (ω_0), the magnitude of output voltage ratio in (8) becomes

$$\left|\frac{V_{o2}}{V_{o1}}\right| = \frac{g_{m2}}{\omega_0 C_2}. \tag{9}$$

Substituting (7) into (9), the magnitude of output voltage ratio in (9) becomes

$$\left|\frac{V_{o2}}{V_{o1}}\right| = \sqrt{\frac{g_{m2} C_1}{g_{m1} C_2}}. \tag{10}$$

If $C_1 = C_2$ and $g_{m1} = g_{m2}$, the magnitude of output voltage ratio is equal to unity. Therefore, the tune of frequency of oscillation with electronic method can simultaneously change g_{m1} and g_{m2} to keep the amplitude of output voltages V_{o1} and V_{o2} equal. This makes the sinusoidal output voltages meet low total harmonic distortions (THD). Moreover, if VDCC is constructed from commercially available ICs as illustrated in Figure 3 where its g_m is linearly tuned by bias current, the frequency of oscillation can be linearly controlled.

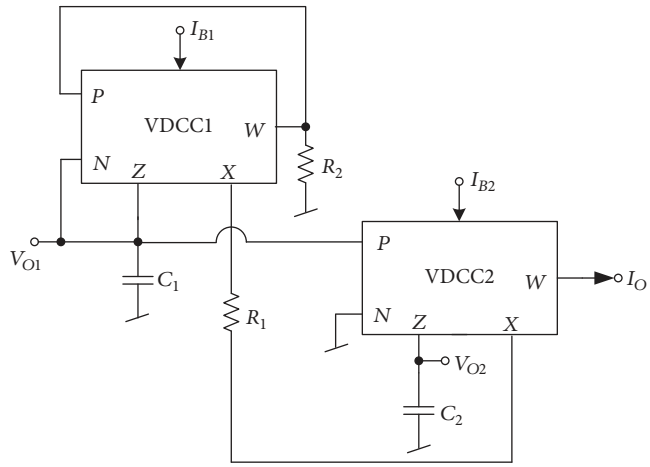

Figure 4: Proposed quadrature oscillator.

3. Analysis of Frequency Stability

The analysis of frequency stability of the proposed circuit is done by using the definition of the frequency stability factor (S_F) given in [29, 30]

$$S_F = \left.\frac{d\phi(u)}{du}\right|_{u=1}, \tag{11}$$

where $u = \omega/\omega_0$ is normalized frequency and $\phi(u)$ is the phase expression of the open loop transfer function of circuit in Figure 4 and its transfer function is expressed as follows:

$$T(s) = \frac{s\left(R_2 g_{m1}/R_1 C_1\right)}{s^2 + s\left(g_{m1}/C_1\right) + R_2 g_{m1} g_{m2}/R_1 C_1 C_2}. \tag{12}$$

With the above definition, the frequency stability factor of the proposed oscillator is given as

$$S_F = 2\sqrt{n}, \tag{13}$$

where $C_1 = C_2 = C$, $R_1 = R_2 = R$, $g_{m1} = 1/R$, and $g_{m2} = n/R$.

4. Effect of Nonideal Current/Voltage Gains and Parasitic Elements

Practically, the influence of nonideal current/voltage gain and parasitic element in VDCC will affect the performances of the proposed oscillator. Considering the these gains, the electrical properties of VDCC are given as $I_z = g_m(V_P - V_N)$, $V_x = \beta V_z$, and $I_z = \alpha I_x$, where β and α represent the voltage and current gain error, respectively. At high impedance ports V_P, V_N, Z, and W, a parallel parasitic combination of a resistance and a capacitance appears and they are denoted as R_P, C_P, R_N, C_N, R_Z, C_Z, R_W, and C_W, respectively. At low impedance port x, a series parasitic resistance appears and it is denoted as R_x. These parasitic impedances affect the performance of the proposed oscillator. Taking them into account, the characteristic equation of the circuit in Figure 4 is obtained as

$$\begin{aligned} &Y_1 Y_2 + Y_2 g_{m1}\left(1 - \frac{\alpha_1\beta_1}{R_1^*\left[1/R_2 + Y_3\right]}\right) \\ &\quad + \frac{\alpha_1\beta_2 g_{m1} g_{m2}}{R_1^*\left(1/R_2 + Y_3\right)} = 0, \end{aligned} \tag{14}$$

where $Y_1 = s(C_1 + C_{N1} + C_{Z1} + C_{P2}) + G_{N1} + G_{Z1} + G_{P2}$, $Y_2 = s(C_2 + C_{z2}) + G_{z2}$, $Y_3 = s(C_{P1} + C_{W1}) + G_{P1} + G_{W1}$, and $R_1^* = R_1 + R_{x1} + R_{x2}$. If the operational frequency $f_{\text{op}} \ll 1/[(C_{P1} + C_{W1})(R_{P1} \parallel R_{W1})]$, the characteristic equation in (13) becomes

$$\begin{aligned} &s^2 C_1^* C_2^* \\ &\quad + s\left[C_1^* G_{z2} + C_2^* G_1^* + C_2^* g_{m1}\left(1 - \frac{\alpha_1\beta_1 R_2}{R_1^*}\right)\right] \\ &\quad + G_1^* G_{z2} + G_{z2}\left(1 - \frac{\alpha_1\beta_1 R_2}{R_1^*}\right) \\ &\quad + \frac{\alpha_1\beta_2 R_2 g_{m1} g_{m2}}{R_1^*} = 0, \end{aligned} \tag{15}$$

where $C_1^* = C_1 + C_{N1} + C_{Z1} + C_{P2}$, $G_2^* = G_{N1} + G_{Z1} + G_{P2}$, and $C_2^* = C_2 + C_{z2}$. From (14), the frequency of oscillation is obtained as

$$\begin{aligned} &\omega_0^* \\ &= \sqrt{\frac{1}{\left(C_1 + C_{N1} + C_{Z1} + C_{P2}\right)\left(C_2 + C_{z2}\right)}\left[\left(\frac{1}{R_{N1}} + \frac{1}{R_{Z1}} + \frac{1}{R_{P2}}\right)\frac{1}{R_{z2}} + \frac{1}{R_{z2}}\left(1 - \frac{\alpha_1\beta_1 R_2}{R_1 + R_{x1} + R_{x2}}\right) + \frac{\alpha_1\beta_2 R_2 g_{m1} g_{m2}}{R_1 + R_{x1} + R_{x2}}\right]}. \end{aligned} \tag{16}$$

Subsequently, the condition of oscillation is given as

$$\left[\frac{1}{g_{m1}R_{z2}}\left(\frac{C_1+C_{N1}+C_{Z1}+C_{P2}}{C_2+C_{z2}}\right)+\frac{1}{g_{m1}}\left(\frac{1}{R_{N1}}+\frac{1}{R_{Z1}}+\frac{1}{R_{P2}}\right)+1\right] \leq \frac{\alpha_1\beta_1R_2}{R_1+R_{x1}+R_{x2}}. \quad (17)$$

From the circuit in Figure 4, the nonideal voltage ratio of V_{o1} and V_{o2} is as follows:

$$\left|\frac{V_{o2}}{V_{o1}}\right|^* = \frac{g_{m2}}{\sqrt{\left[\omega_0^*\left(C_2+C_{z2}\right)\right]^2+\left[G_{z2}\right]^2}}. \quad (18)$$

Substituting (16) into (18), the magnitude of output voltage ratio in (18) becomes

$$\left|\frac{V_{o2}}{V_{o1}}\right|^* = \frac{g_{m2}}{\sqrt{\left(\left(C_2+C_{z2}\right)/\left(C_1+C_{N1}+C_{Z1}+C_{P2}\right)\right)\left[\left(1/R_{N1}+1/R_{Z1}+1/R_{P2}\right)\left(1/R_{z2}\right)+\left(1/R_{z2}\right)\left(1-\alpha_1\beta_1R_2/\left(R_1+R_{x1}+R_{x2}\right)\right)+\alpha_1\beta_2R_2g_{m1}g_{m2}/\left(R_1+R_{x1}+R_{x2}\right)\right]+\left[1/R_{z2}\right]^2}}. \quad (19)$$

It is found in (19) that although $C_1 = C_2$, $R_1 = R_2$, and $g_{m1} = g_{m2}$, the magnitude of output voltage ratio is not equal to unity. According to (19), the phase response of V_{o2} to V_{o1} becomes

$$\theta^*_{V_{o2}/V_{o1}} = -\tan^{-1}\frac{\omega_0^*\left(C_2+C_{z2}\right)}{G_{z2}}. \quad (20)$$

5. Experimental Results

In order to verify the performances of the proposed oscillator in Figure 4, the experiment was performed by using VDCC constructed from commercially available ICs, LM13700 from Texas Instruments Incorporated and AD844 from Analog Devices, Inc. as illustrated in Figure 3. The power supply voltages of experiment were ±5 V. The oscillator was designed to obtain the frequency of oscillation, $f_0 = 50$ kHz. From (7), an experimental setup was made by taking $C_1 = C_2 = 10$ nF, $R_1 = 7.23\,\text{k}\Omega$, $R_2 = 7.52\,\text{k}\Omega$, and $I_{B1} = I_{B2} = 163\,\mu$A. With the above component values, the experimented frequency of oscillation becomes $f_0 = 47$ kHz. The deviation of theoretical and experimental frequency of oscillation is about 6%. The deviation of theoretical and experimental value stems from the parasitic resistances and capacitances as shown in (16). However, $f_0 = 50$ kHz was obtained when I_{B1} and I_{B2} were set as 180 μA. The measured sinusoidal quadrature waveforms V_{o1}, V_{o2} and their frequency spectrums are illustrated in Figure 5. The output current waveform and its spectrum which is measured from the voltage dropped on load resistor 10 kΩ are depicted in Figure 6. To obtain the frequency of oscillation $f_0 = 100$ kHz, the bias currents I_{B1} and I_{B2} were set to 370 μA. Figure 7 represents the output waveforms V_{o1} and V_{o2} and their frequency spectrums. The output current waveform and its spectrum at $f_0 = 100$ kHz is depicted in Figure 8. Tuning of experimental and theoretical FO is shown in Figure 9, where I_{B1} and I_{B2} are equal and were adjusted from 100 μA to 500 μA. The range of FO controlled from 27 kHz–131 kHz was obtained. Figure 10 shows simulated dependence of output amplitudes V_{O1} and V_{O2} on FO. It can be clearly seen that the ratio of amplitudes V_{O1} and V_{O2} is quite constant on the tuning of FO if I_{B1} and I_{B2} are simultaneously tuned as predicted in (10). As stated above, VDCC consists of operational transconductance amplifier (OTA) where it is well known that the BJT OTA gives the linear range if input voltage is lower than $2V_T$ (≅52 mV). With the result in Figure 10, it is found that the amplitude of output voltages which dropped on input voltage of OTA is close to linear range of OTA. This implies that sinusoidal output waveforms provide good THD. However, at high value of bias current, the deviation of amplitude ratio of V_{o1} and V_{o2} obviously appears. This phenomenon results from the fact that the increment of bias current will decrease the value of parasitic resistance. Therefore, the amplitude of V_{o1} and V_{o2} is slightly different as analyzed in (19). The measured phase difference between the two outputs, V_{o1} and V_{o2}, is illustrated in Figure 11.

6. Comparison with Recent Quadrature Oscillators

A comparison between the proposed quadrature oscillator and recent quadrature oscillator published in scientific journals is shown in Table 1. The terms that will be taken into account are as follows: the used active building block (ABB), number of active and passive element, the way to tune FO and CO, amplitude of the quadrature output waveforms during tuning process, the used ABB without multiple or extra terminals, additional current output with high impedance, the connection of capacitors, and the way to test the circuit.

7. Conclusion

In this contribution, the quadrature sinusoidal oscillator using voltage differencing current conveyor as active element is presented. The proposed circuit comprises two VDCCs, two resistors, and two grounded capacitors. The proposed oscillator provides quadrature voltage output and a high impedance current output. The frequency of oscillation can be electronically tuned without affecting the condition of oscillation. During tuning of the frequency of oscillation, the amplitude of the quadrature output voltages V_{o1} and V_{o2}

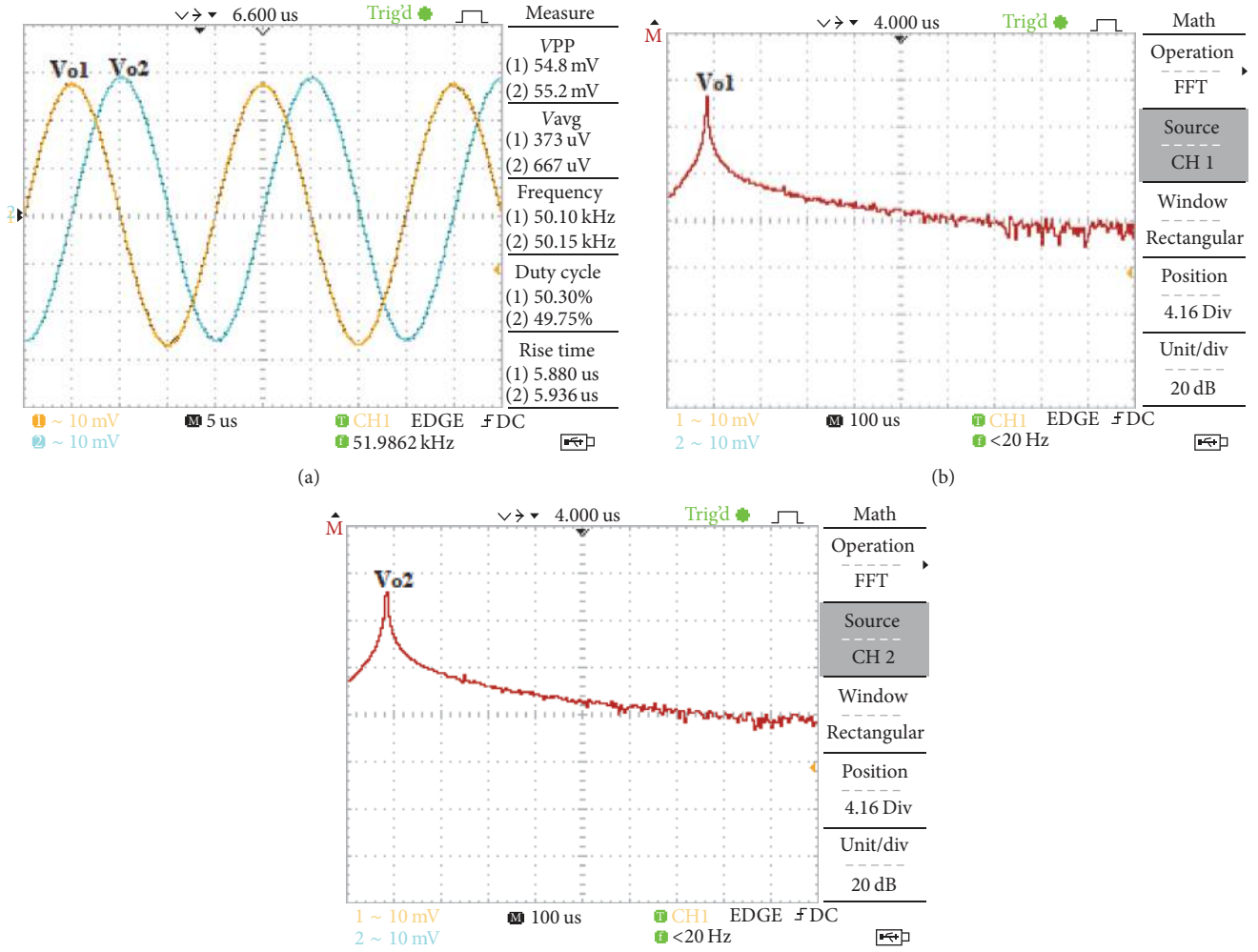

Figure 5: Measurement of output voltages and their spectrums at $f_0 = 50$ kHz.

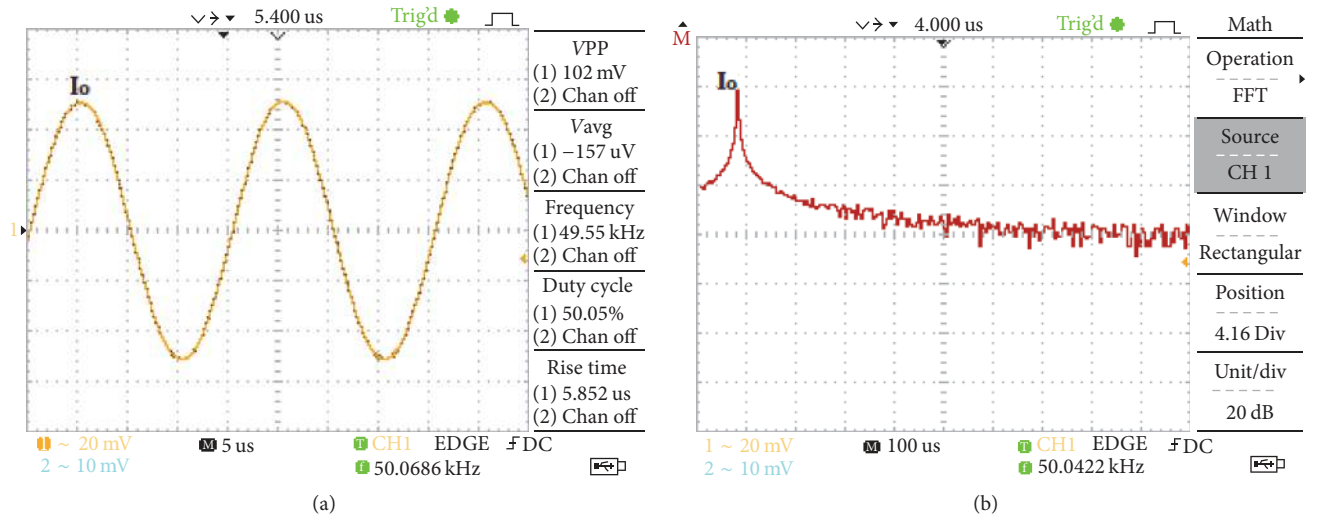

Figure 6: Measurement of output current and its spectrum at $f_0 = 50$ kHz.

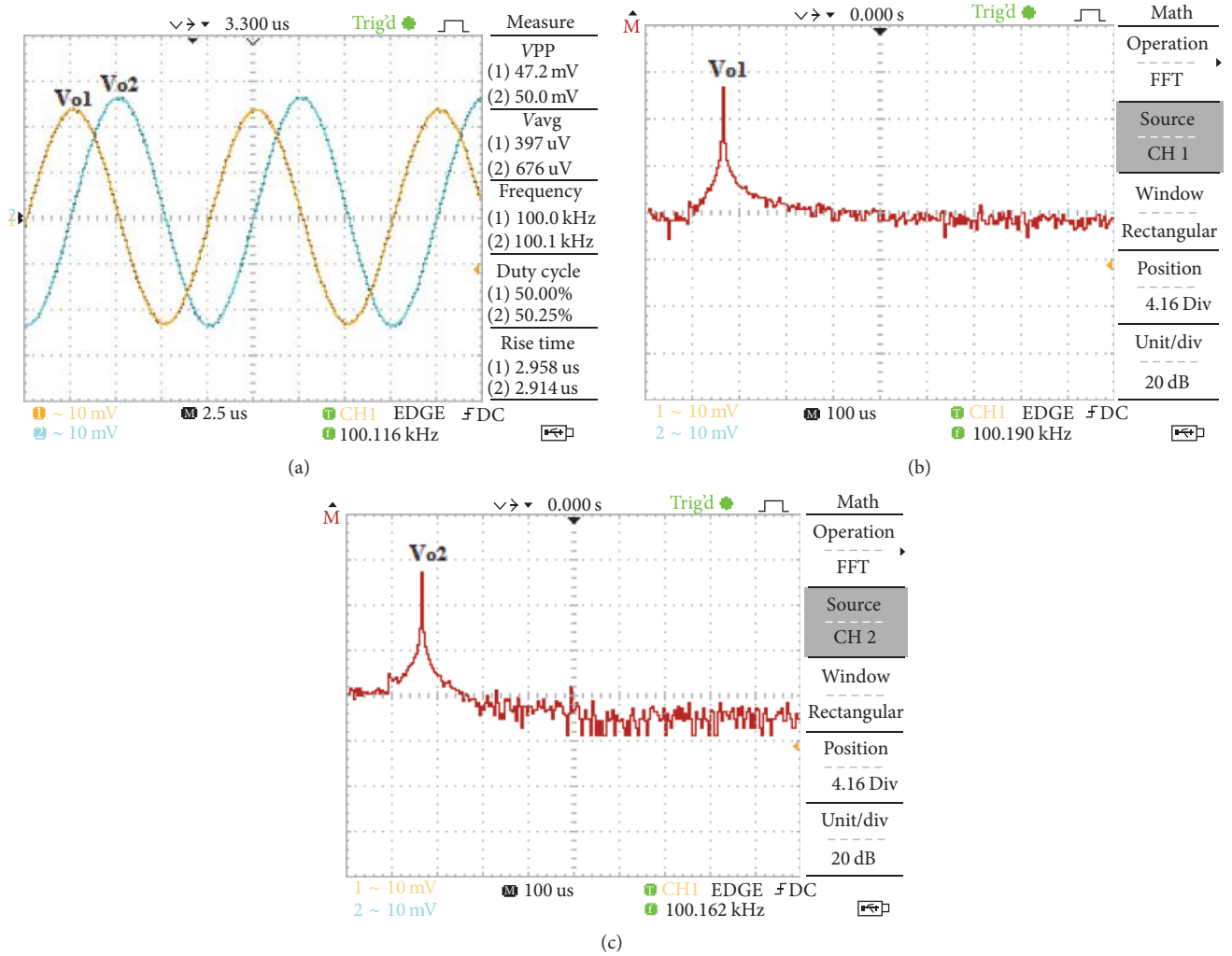

Figure 7: Measurement of output voltages and their spectrums at $f_0 = 100$ kHz.

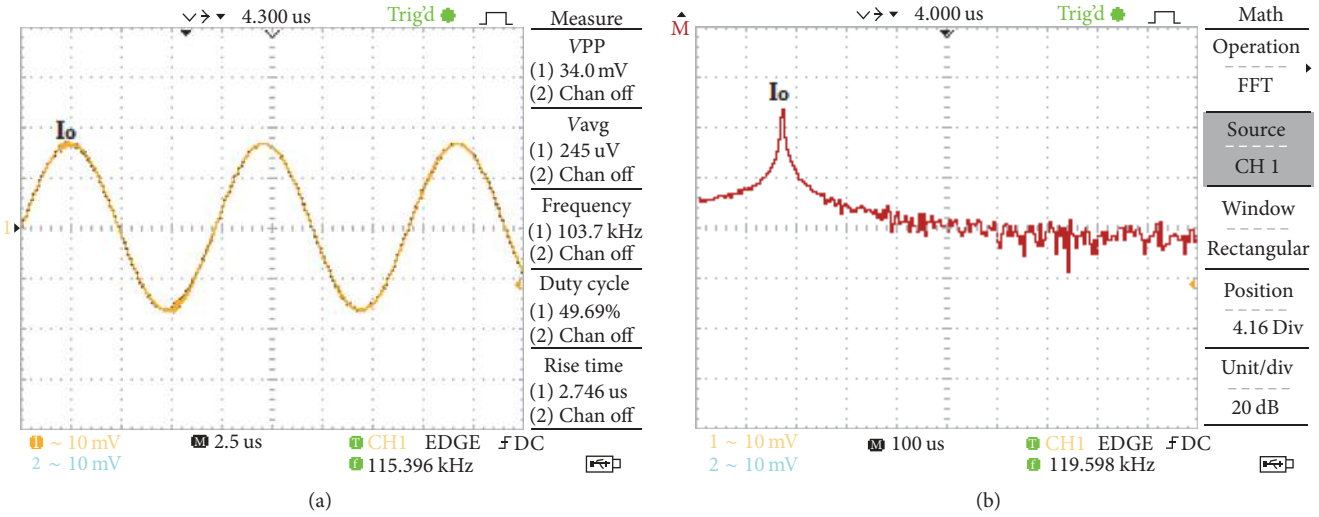

Figure 8: Measurement of output current and its spectrum at $f_0 = 100$ kHz.

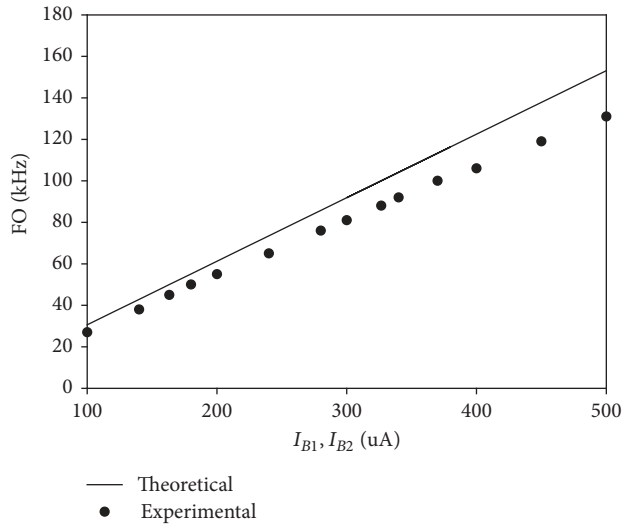

Figure 9: Tuning of experimental and theoretical FO by adjusting bias current.

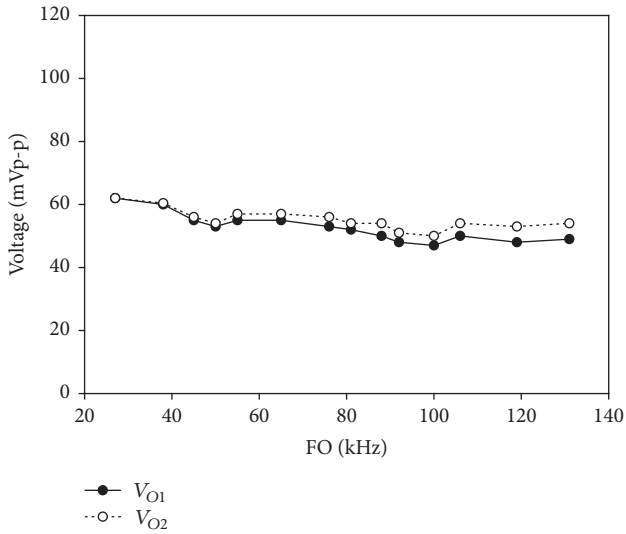

Figure 10: Dependence of amplitudes of V_{O1} and V_{O2} on FO.

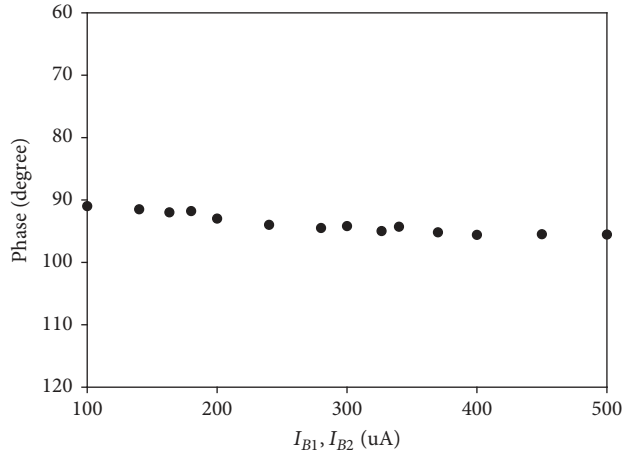

Figure 11: The measured phase difference of V_{O1} and V_{O2}.

Table 1: Comparison results of this work and recent works.

Ref	ABB	Number of ABB	Number of R + C	Electronic tune of FO without affecting CO	Equal amplitudes during frequency tuning	No need of multiple output ABB	Providing additional sinusoidal current output with high impedance	Grounded C only	Experimental results
[23]	VDCC	1	2 + 2	No	No	No	Yes	Yes	No
[24]	VDCC	1	2 + 2	Yes	No	No	No	Yes	Yes
[25]	VDCC	2	2 + 2	Yes	No	No	Yes	Yes	No
[26]	CG-VDCC	1	0 + 2	Yes	Yes	No	No	Yes	No
[31]	CCCCTA	1	2 + 2	Yes	No	No	Yes	Yes	No
[32]	CCCCTA	2	2 + 2	Yes	No	No	Yes	Yes	No
[33]	CCII & BF	3	4 + 2	No	No	Yes	No	Yes	Yes
[34]	CCII	3	2 + 2	Yes	No	Yes	No	Yes	No
[35]	CDTA	2	0 + 3	Yes	No	No	Yes	Yes	No
[36]	CFOA	2	2 + 2	No	No	Yes	No	Yes	Yes
[37]	CFOA	2	3 + 2	No	No	Yes	No	Yes	Yes
[38]	DD-DXCCII	1	3 + 2	No	No	No	No	Yes	No
[39]	MDVCC	1	2 + 2	No	No	Yes	No	Yes	No
[40]	DVCCTA	1	3 + 2	Yes	No	No	Yes	Yes	No
[41]	FBVDBA	1	1 + 2	No	No	No	No	Yes	Yes
[42]	OTRA	2	3 + 3	No	No	Yes	No	No	Yes
[43]	MVDVTA	1	1 + 2	No	No	No	No	Yes	No
This work	VDCC	2	2 + 2	Yes	Yes	Yes	Yes	Yes	Yes

is almost constant with slight differences due to the effect of the parasitic resistances and capacitances of the VDCC. The experimental results using VDCC constructed from commercially available ICs confirm the performance of the theoretical analysis.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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References

[1] R. K. Sharma, T. S. Arora, and R. Senani, "On the realisation of canonic single-resistance-controlled oscillators using third generation current conveyors," *IET Circuits, Devices & Systems*, vol. 11, no. 1, pp. 10–20, 2017.

[2] M. T. Abuelma'atti, "New two CFOA-based sinusoidal RC oscillators with buffered outlet," *Analog Integrated Circuits and Signal Processing*, vol. 66, no. 3, pp. 475–482, 2011.

[3] D. R. Bhaskar, S. S. Gupta, R. Senani, and A. K. Singh, "New CFOA-based sinusoidal oscillators retaining independent control of oscillation frequency even under the influence of parasitic impedances," *Analog Integrated Circuits and Signal Processing*, vol. 73, no. 1, pp. 427–437, 2012.

[4] J.-W. Horng, Z.-R. Wang, and T.-Y. Yang, "Single ICCII sinusoidal oscillators employing grounded capacitors," *Radioengineering*, vol. 20, no. 3, pp. 608–613, 2011.

[5] S. Maheshwari and R. Verma, "Electronically tunable sinusoidal oscillator circuit," *Active and Passive Electronic Components*, vol. 2012, Article ID 719376, 2012.

[6] M. T. Abuelma'atti and Z. J. Khalifa, "A novel operational amplifier-based square/triangular/sinusoidal oscillator," *International Journal of Electrical Engineering Education*, vol. 52, no. 3, pp. 276–283, 2015.

[7] S. Sangyaem, S. Siripongdee, W. Jaikla, and F. Khateb, "Five-inputs single-output voltage mode universal filter with high input and low output impedance using VDDDAs," *International Journal for Light and Electron Optics*, vol. 128, pp. 14–25, 2017.

[8] R. Senani, "On the transformation of grounded inductors to floating inductors using of a and FCCII," *Journal of Circuits, Systems and Computers*, vol. 21, no. 5, Article ID 1250044, 2012.

[9] D. Biolek, R. Senani, V. Biolkova, and Z. Kolka, "Active elements for analog signal processing: classification, review, and new proposals," *Radioengineering*, vol. 17, no. 4, pp. 15–32, 2008.

[10] F. Kaçar, A. Yeşil, S. Minaei, and H. Kuntman, "Positive/negative lossy/lossless grounded inductance simulators employing single VDCC and only two passive elements," *AEU - International Journal of Electronics and Communications*, vol. 68, no. 1, pp. 73–78, 2014.

[11] F. Kaçar, A. Yeşil, and K. Gürkan, "Design and experiment of VDCC-based voltage mode universal filter," *Indian Journal of Pure and Applied Physics*, vol. 53, no. 5, pp. 341–349, 2015.

[12] M. Sagbas, U. E. Ayten, M. Koksal, and N. Herencsar, "Electronically tunable universal biquad using a single active component," in *Proceedings of the 38th International Conference on Telecommunications and Signal Processing (TSP '15)*, pp. 698–702, July 2015.

[13] J. Jerabek, R. Sotner, J. Polak, K. Vrba, and T. Dostal, "Reconnection-less Electronically Reconfigurable Filter with Adjustable Gain Using Voltage Differencing Current Conveyor," *Elektronika ir Elektrotechnika*, vol. 22, no. 6, pp. 39–45, 2016.

[14] P. Lamun, P. Phatsornsiri, and U. Torteanchai, "Single VDCC-based current-mode universal biquadratic filter," in *Proceedings of the 7th International Conference on Information Technology and Electrical Engineering (ICITEE '15)*, pp. 122–125, October 2015.

[15] R. Sotner, N. Herencsar, J. Jerabek et al., "Novel first-order all-pass filter applications of z-copy voltage differencing current conveyor," *Indian Journal of Pure and Applied Physics*, vol. 53, no. 8, pp. 537–545, 2015.

[16] D. Prasad, A. Ahmad, A. Shukla, A. Mukhopadhyay, B. B. Sharma, and M. Srivastava, "Novel VDCC based low-pass and high-pass Ladder filters," in *Proceedings of the 12th IEEE International Conference Electronics, Energy, Environment, Communication, Computer, Control (INDICON '15)*, December 2015.

[17] A. Kartci, U. E. Ayten, N. Herencsar, R. Sotner, J. Jerabek, and K. Vrba, "Application possibilities of VDCC in general floating element simulator circuit," in *Proceedings of the European Conference on Circuit Theory and Design (ECCTD '15)*, August 2015.

[18] A. Kartci, U. E. Ayten, R. Sotner, and R. Arslanalp, "Electronically tunable VDCC-based floating capacitance multiplier," in *Proceedings of the 23rd Signal Processing and Communications Applications Conference (SIU '15)*, pp. 2474–2477, May 2015.

[19] A. Kartci, U. E. Ayten, N. Herencsar, R. Sotner, J. Jerabek, and K. Vrba, "Floating capacitance multiplier simulator for grounded RC colpitts oscillator design," in *Proceedings of the 20th International Conference on Applied Electronics (AE '15)*, pp. 93–96, September 2015.

[20] D. Prasad and J. Ahmad, "New Electronically-Controllable Lossless Synthetic Floating Inductance Circuit Using Single VDCC," *Circuits and Systems*, vol. 05, no. 01, pp. 13–17, 2014.

[21] M. Srivastava, P. Bhanja, and S. F. Mir, "A new configuration for simulating passive elements in floating state employing VDCCs and grounded passive elements," in *Proceedings of the 1st International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES)*, pp. 1–4, Delhi, India, July 2016.

[22] R. Sotner, J. Jerabek, N. Herencsar, T. Dostal, and K. Vrba, "Design of Z-copy controlled-gain voltage differencing current conveyor based adjustable functional generator," *Microelectronics Journal*, vol. 46, no. 2, pp. 143–152, 2015.

[23] D. Prasad, D. R. Bhaskar, and M. Srivastava, "New single VDCC-based explicit current-mode SRCO employing all grounded passive components," *Electronics*, vol. 18, no. 2, pp. 81–88, 2014.

[24] R. Sotner, J. Jerabek, R. Prokop, and V. Kledrowetz, "Simple CMOS voltage differencing current conveyor-based electronically tunable quadrature oscillator," *Electronics Letters*, vol. 52, no. 12, pp. 1016–1018, 2016.

[25] M. Srivastava and D. Prasad, "VDCC based dual-mode quadrature sinusoidal oscillator with outputs at appropriate impedance levels," *Advances in Electrical and Electronic Engineering*, vol. 14, no. 2, pp. 168–177, 2016.

[26] R. Sotner, J. Jerabek, J. Petrzela, and T. Dostal, "Voltage differencing current conveyor based linearly controllable quadrature oscillators," in *Proceedings of the 21st International Conference on Applied Electronics (AE '16)*, pp. 237–240, September 2016.

[27] http://www.ti.com/lit/ds/symlink/lm13700.pdf.

[28] http://www.analog.com/media/en/technical-documentation/data-sheets/AD844.pdf.

[29] D. R. Bhaskar and R. Senani, "New current-conveyor-based single-resistance-controlled/voltage-controlled oscillator employing grounded capacitors," *Electronics Letters*, vol. 29, no. 7, pp. 612–614, 1993.

[30] D. R. Bhaskar, D. Prasad, and K. L. Pushkar, "Fully Uncoupled Electronically Controllable Sinusoidal Oscillator Employing VD-DIBAs," *Circuits and Systems*, vol. 04, no. 03, pp. 264–268, 2013.

[31] H.-P. Chen, S.-F. Wang, and Y.-T. Ku, "CCCCTA-based resistorless voltage and current mode quadrature oscillator," *IEICE Electronics Express*, vol. 12, no. 13, article 014, 2015.

[32] A. Jantakun, "Current-mode quadrature oscillator using CCC-CTAs with non-interactive current control for CO, FO and amplitude," *Informacije MIDEM*, vol. 19, no. 2, pp. 47–56, 2015.

[33] F. Yucel and E. Yuce, "CCII based more tunable voltage-mode all-pass filters and their quadrature oscillator applications," *AEU - International Journal of Electronics and Communications*, vol. 68, no. 1, pp. 1–9, 2014.

[34] S. B. Salem, A. B. Saied, and D. S. Masmoudi, "High-performance current-controlled quadrature oscillator using an optimized CCII," *Informacije MIDEM*, vol. 46, no. 2, pp. 91–99, 2016.

[35] J. Jin, C. Wang, and J. Sun, "Novel third–order quadrature oscillators with grounded capacitors," *Automatika*, vol. 56, no. 2, pp. 207–216, 2015.

[36] H.-P. Chen, S.-F. Wang, Y.-T. Ku, and M.-Y. Hsieh, "Quadrature oscillators using two cfoas and four passive components," *IEICE Electronics Express*, vol. 12, no. 2, 2015.

[37] H.-P. Chen, Y.-S. Hwang, Y.-T. Ku, S.-F. Wang, and C.-H. Wu, "Voltage-mode universal biquadratic filter and quadrature oscillator using CFAs," *IEICE Electronics Express*, vol. 13, no. 15, 2016.

[38] B. Chaturvedi and J. Mohan, "Single DD-DXCCII based quadrature oscillator with simultaneous current and voltage outputs," *Electronics*, vol. 19, no. 2, pp. 94–100, 2015.

[39] A. Abaci and E. Yuce, "Modified DVCC based quadrature oscillator and lossless grounded inductor simulator using grounded capacitor(s)," *AEU - International Journal of Electronics and Communications*, vol. 76, pp. 86–96, 2017.

[40] P. Uttaphut, "New current-mode quadrature sinusoidal oscillator using single DVCCTA as active element," *Przegląd Elektrotechniczny*, vol. 92, no. 9, pp. 229–232, 2016.

[41] A. Yesil, F. Kacar, and K. Gurkan, "Design and experimental evaluation of quadrature oscillator employing single FB-VDBA," *Journal of Electrical Engineering*, vol. 67, no. 2, pp. 137–142, 2016.

[42] B. C. Nagar and S. K. Paul, "Voltage mode third order quadrature oscillators using OTRAs," *Analog Integrated Circuits and Signal Processing*, vol. 88, no. 3, pp. 517–530, 2016.

[43] H. Alpaslan, "A modified VDVTA and its applications to floating simulators and a quadrature oscillator," *Microelectronics Journal*, vol. 51, pp. 1–14, 2016.