Electrostatic Characteristics of High-k Stacked Gate-All-Around Heterojunction Tunnel Field Effect Transistor using Superposition Principle

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Electrostatic Characteristics of High-k Stacked Gate-All-Around Heterojunction Tunnel Field Effect Transistor using Superposition Principle

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Abstract

We use superposition method to model the electrostatic characteristics of high-k stacked Gate-All-Around Hetero Junction TFETs (GAA-HJTFETs). The hetero junction is set up by using Ge/Si material in the source/channel respectively. The modeling is accomplished by considering the space charge regions at the source-channel/drain-channel junctions and the channel region. The surface potential in the channel region is obtained by applying superposition principle, where as in source/drain it is derived by solving 2-D/1-D Poisson's equation respectively. Furthermore, the electric field and drain current are modeled from the surface potential and Kane model respectively. The results are confirmed using ATLAS TCAD simulation.

Keywords

Gate All Around Tunnel Field Effect Transistor, Heterojunction, Superposition Principle, Surface Potential, Electric Field, Drain Current and TCAD

1. Introduction

With years of continuous down-scaling the transistors in CMOS technology leads to deteriorate the subthreshold swing (SS), leakage current and threshold voltage (VT) [1-3]. In addition, the power crisis faced by the device engineers, entail the gateway to the multi-gate/gate-all-around FETs, group III-V based FETs, super steep subthreshold slope FETs, and graphene/carbon-nanotube based FETs . Tunnel FETs is one such device which earned the awareness of researchers, because of its low sub-threshold swing (< 60 mV/decade) and reduced short channel effects [4, 5]. A three-terminal p-i-n device, where the source and drain are doped contrary, besides the channel is either intrinsic or lightly doped is called TFETs. It has two junctions namely, drain-channel junction (JDC) and source-channel (JSC). The carrier transport in TFETs is controlled by inter-band tunneling (BTBT), while thermionic emission in Metal Oxide Semiconductor FETs (MOSFETs). Though the device exhibits low SS and Ioff, but also suffers from low ION and ambipolar conduction [6, 7]. In this regard, alternative approach such as gate engineering (i.e., employing of multi-gate/gate-all-around structures) [8-10], gate dielectric engineering (i.e., make use of high-k material as a gate dielectric) [11], work function engineering (i.e., employing asymmetric gate work

functions instead of symmetric) [12], tunnel engineering (i.e., bring in a heavily doped source pocket at the JSC such that its completely depleted) [13] and materials engineering (i.e., using lower band-gap materials like InAs, GaAs, InGaAs, SiGe and Ge as an alternative to Si) [14] mechanisms have been proposed to mitigate the shortcomings of TFETs.

Over the decades, quite a few analytical models for the electrical parameters in particular surface potential, electric field, threshold voltage and drain current for single/double gate and GAA-TFETs [15-17] with single/dual material gate (SMG/DMG) electrode were reported. The electrical outcomes of the aforementioned devices were examined by Verhulst et al. [15]. The 2-D electrostatic response of DG and GAA TFETs were reported by Pan et al. [16]. Vishnoi et al. [17] proposed the BTBT current model for DG-GAA-TFETs irrespective of the depletion regions at JSC and JDC by pseudo-2-D analytic modeling. The DMG in DG-TFETs exhibits better drive current and SS than SMG counterpart as reported by Kumar et al. [18] and Jain et al. [19]. Kumar et al. [20] and Prabhat et al. [21] reported the modeling of drive current and surface potential for DMG with SG/DG TFET structures respectively. The device performance by can be enhanced by replacing SiO2 with pile up SiO2 and a high-k dielectric in DG TFETs as reported by Kumar et al [22]. The proposed Ge-Si-Si hetero stacked gate dielectric GAA-TFET device provides better ION per unit area than its counterpart planner devices. Hence, developing an accurate model for surface potential, electric field and drain current becomes important.

The corroboration of this model is verified against previously published reports and 3D-numerical simulators [23]. The paper is presented as follows: Section 2 and 3 discuss about the device architecture and results followed by conclusion.

2. Device Structure

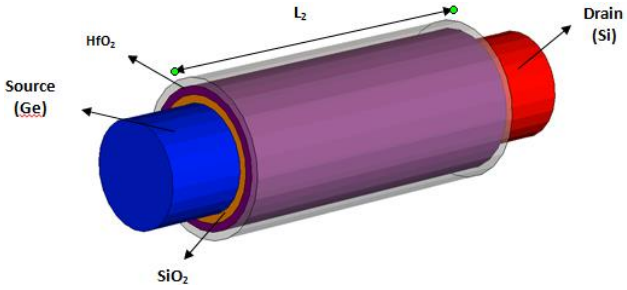

Fig. 1a. 3-D view of high-k stacked GAA HJ-TFET

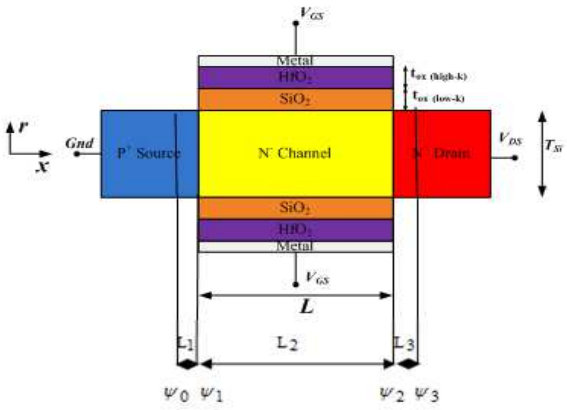

Fig. 1b. Cross sectional 2-D view of high-k stacked GAA HJ-TFET

Fig. 1(a) and Fig. 1(b) shows the 3-D and 2-D view of proposed TFETs, where the high-k dielectric is deposited on top of the low-k dielectric. The device specifications are tabulated in the table 1. Three depletion regions are considered for modeling namely region I, II and III are source-channel, channel and drain-channel respectively. The length of three corresponding regions are considered as L_1, L_2 and L_3. The potentials across the corresponding regions are ψ_0, ψ_1, ψ_2 and ψ_3.

Table 1. List of parameters for High-k stacked GAA HJ-TFET

Sl.N	Symbo	Description	Value
1	N_S	Source	1×10^{20}
2	N_C	Channel	1×10^{16}
3	N_D	Drain	5×10^{18}c
4	L_2	Length of the	50 nm
5	ϕ_m	Work function	4.3 eV
6	t_{ox}	Thickness of	1 nm
7	t_k	Thickness of	2 nm
8	t_{si}	Thickness of Si	13 nm
9	ε_o	Permittivity of	8.854×10
10	ε_{si}	Permittivity of	$11.9\ \varepsilon_o$
11	ε_{ox}	Permittivity of	$3.9\ \varepsilon_o$

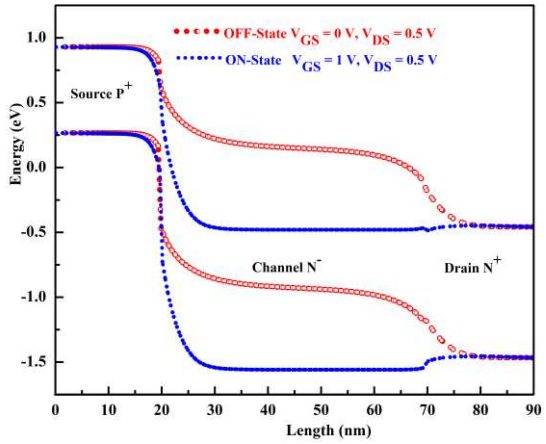

Fig. 2. Energy Band profile of proposed GAA HJ-TFET

Fig. 2. depicts the band profile of the proposed device. When V_{GS} = 0 V (OFF-State) the inter-band tunneling is inhibited, as a result no electrons tunnel through the depletion region at J_{SC}. When V_{GS} = 1 V (ON-State) the energy band gap reduces and inter-band tunneling is permitted which allows the electrons to tunnel from the source to channel. The tunneling rate of electrons is high in hetero-junction devices compared to homo-junction devices due to narrow bandgap materials at source.

3. MODEL DERIVATION

Figure 1(b) shows the 2-D view of the device considered for modeling. The co-ordinates of the device were denoted by z and r- axes and the junction potentials were given by ψ_0, ψ_1, ψ_2 and ψ_3 at $z=0, z_1=L_1, z_2=L_1+L_2$ and $z_3=L_1+L_2+L_3$.

3.1. Modeling of Potential in the channel

The distribution of potential in the gate all around device is same as the double gate device structure. The tubular symmetry nature of the proposed device leads to an angular co-ordinate independent of surface potential. Thus, the 2-D Poisson's equation of cylindrical co-ordinates is considered for modeling and in channel region it is given by

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial \psi_{ch(z,r)}}{\partial r}\right)+\frac{\partial^2 \psi_{ch}(z,r)}{\partial r^2}=\frac{q}{\varepsilon_{si}}\eta \quad (1)$$

Where $\psi_{ch}(z,r)$ is potential across the channel, ε_{si} - permittivity of silicon. The charge density of mobile carriers across the channel is given as

$$\eta=\eta_i \exp\left(\frac{\psi_{ch(z,r)}-V(z,r)}{V_T}\right) \quad (2)$$

Where $V_T=\frac{KT}{q}$ the thermal voltage at 300 K and V the non-equilibrium quasi-Fermi level referred to Fermi level of source region with the boundaries given by [24].

$$V(0,r)=0 \quad (3)$$

$$V(L_2,r)=V_{DS} \quad (4)$$

The quasi-Fermi level is almost constant in the radial direction [25]. V_{DS} is approximated to be drain-source voltage along the channel expect at the left verge of the channel. At the channel electrostatic potential boundary conditions are

$$C_d\left[V_{GS}-\phi_{ms1,i}-\psi_{ch}\left(z,r=r_0\right)\right]=\varepsilon_{si}\left.\frac{\partial\psi_{ch}\left(z,r\right)}{\partial r}\right|_{r=r_0}\quad\left.\frac{d\varphi_1\left(r\right)}{dr}\right|_{r=0}=0 \tag{13}$$

(5)

$$\psi_{ch}\left(0,r\right)=\phi_{0s} \tag{6}$$

$$\psi_{ch}\left(L,r\right)=\phi_{0d} \tag{7}$$

Where C_d the capacitance dielectric per unit area.

$$C_d=\frac{\varepsilon_{ox}}{r_0\ln\left(1+\frac{t_{ox}}{r_0}\right)} \tag{8}$$

Where $r_0=\frac{t_{si}}{2}$, $\phi_{ms1,i}$ the work function of gate referenced to the silicon material

$$\phi_{ms1,i}=\phi_m-\left(\chi_{si}+\frac{E_{gsi}}{2q}\right) \tag{9}$$

ϕ_m, χ_{si}, E_{gsi}, ϕ_{os} and ϕ_{od} are the work function of gate, electron affinity of Si, energy band gap of Si, the left end and right end potentials respectively.

$$\psi_{ch}\left(z,r\right)=\varphi_1\left(r\right)+\varphi_2\left(z,r\right) \tag{10}$$

Where $\varphi_1(r)$ is the solution of 1-D Poisson's equation obtained as shown below

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial\varphi_1\left(r\right)}{\partial r}\right)=\frac{q}{\varepsilon_{si}}n_i\exp\left(\frac{\varphi_1\left(r\right)-V}{V_T}\right) \tag{11}$$

The boundary condition at the interface of silicon-dielectric is

$$C_{ox}\left[V_{GS}-\phi_{ms}-\varphi_1\left(r=r_0\right)\right]=\varepsilon_{si}\left.\frac{d\varphi_1\left(r\right)}{dr}\right|_{r=r_0} \tag{12}$$

Considering the symmetric of the structure by

Using equation (12) and (13), 1-D potential is obtained as

$$\varphi_1\left(r\right)=V+U_T\ln\left(\frac{8B\varepsilon_{si}}{qn_i\left(Br^2+1\right)^2}\right) \tag{14}$$

Substituting equation (14) in equation (12), we can determine B

$$\frac{V_{GS}-\phi_{ms}-V}{U_T}-\ln\left(\frac{8B\varepsilon_{si}}{qn_i\left(Br_0^2+1\right)^2}\right)=-\frac{4BU_Tr}{Cox\left(Br^2+1\right)} \tag{15}$$

From equation (10) the solution $\varphi_2(z,r)$ 2-D potential equation is obtained from residual 2-D equation

$$\nabla^2\varphi_2\left(z,r\right)=\frac{q}{\varepsilon_{si}}\times n_i\exp\left(\frac{\varphi_1\left(r\right)-V}{U_T}\right)\times\left[\exp\left(\frac{\varphi_2\left(z,r\right)}{U_T}\right)-1\right] \tag{16}$$

The boundary conditions to be satisfied by $\varphi_2(z,r)$ are [24]

$$\varphi_2\left(0,r\right)=\varphi_{os}-\varphi_1\left(r\right) \tag{17}$$

$$\varphi_2\left(L,r\right)=\varphi_{oD}-\varphi_1\left(r\right) \tag{18}$$

$$C_{ox}\left[-\varphi_2\left(z,r=r_0\right)\right]=\varepsilon_{si}\left.\frac{\partial\varphi_2\left(z,r\right)}{\partial r}\right|_{r=r_0} \tag{19}$$

Assuming φ_2/U_T is small equation (16) is reduced to 2-D Laplace equation. This approximation is valid in TFETs [26]. The separation of variable method is used to derive the $\varphi_2(z,r)$. The expression attained is

$$\varphi_2\left(z,r\right)=\left[C_0e^{\frac{\lambda}{r_0}z}+C_1e^{-\frac{\lambda}{r_0}z}\right]J_0\left(\lambda,r\right) \tag{20}$$

where *Ji (x)* is the first kind Bessel function of the order i . Using (20) in (18) gives the separation factor λ relation (should be a positive value)

$$C_{ox}\frac{r_0}{\varepsilon_{si}}=\lambda\frac{J_1(\lambda)}{J_0(\lambda)} \tag{21}$$

Consider $C_r=C_{ox}\frac{r_0}{\varepsilon_{si}}$. Applying the boundary conditions (17) and (18) in equation (20) to obtain the expression for the co-efficient of equation (20) (detailed derivation is given in Appendix).

$$C_0=\frac{1}{2NSinh\left(\frac{\lambda L}{r_0}\right)}\left[\frac{J_1(\lambda)}{\lambda}\left(\phi_{oD}-\phi_{0S}\right)\exp\left(-\frac{L\lambda}{r_0}\right)+S_1V_a\right] \tag{22}$$

$$C_1=\frac{1}{2NSinh\left(\frac{\lambda L}{r_0}\right)}\left[\frac{J_1(\lambda)}{\lambda}\left[\varphi_{0S}\exp\left(\frac{L\lambda}{r_0}\right)-\varphi_{0D}\right]+S_2V_a\right] \tag{23}$$

Based on the device dimensions, S_1, S_2 and N are given by

$$S_1=\exp\left(-\frac{L\lambda}{r_0}\right)-1 \tag{24}$$

$$S_2=1-\exp\left(\frac{L\lambda}{r_0}\right) \tag{25}$$

$$N=\frac{J_0^2(\lambda)}{2}\left[\left(\frac{C_r}{\lambda}\right)^2+1\right] \tag{26}$$

The total potential across the channel of proposed device is gained by adding the potential terms obtained from equations (14) and (20).

3.2. Modeling of Potential in the depletion region of Source

The depletion region across the source cannot be neglected for higher voltages, thus the voltage drop along this region is to be considered. The 2-D Poisson's equation in region R1 is given by

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial\varphi_s(z,r)}{\partial r}\right)+\frac{\partial^2\varphi_s(z,r)}{\partial z^2}=\frac{qN_A}{\varepsilon_{si}}\qquad -L_1\le x\le 0 \tag{27}$$

Where $\varphi_s(z,r)$ is electrostatic potential that refers to the fermi level in the source region and N_A is the doping concentration in the source. The electrostatic potential along the r direction is approximated to parabolic approximation equation [27].

$$\varphi_s(z,r)=A_0(z)+A_1(z)r+A_2(z)r^2 \tag{28}$$

The boundary conditions to obtain the co-efficient of the parabolic approximation equation are

$$\varphi_s(z,r)=\varphi_s(z) \tag{29}$$

$$\left.\frac{d\varphi_s(z,r)}{dr}\right|_{r=0}=0 \tag{30}$$

$$C_f\left[V_{GS}-\phi_{ms,i}-\phi_s(z)\right]=\varepsilon_{si}\left.\frac{\partial\varphi_s(z,r)}{\partial r}\right|_{r=r_0} \tag{31}$$

Where $C_f=\frac{2}{\pi}C_{ox}$ is the fringing field effect considered by the conformal mapping techniques as[28]. Applying the boundary conditions to equation (28), we obtain the co-efficient as

$$A_0(z)=-\frac{r_0C_{ox}}{\pi\varepsilon_{si}}\left(V_{GS}-\phi_{ms,i}\right)+\left(1+\frac{r_0C_{ox}}{\pi\varepsilon_{si}}\right)\varphi_s(z) \tag{32}$$

$$A_1(z)=0 \tag{33}$$

$$A_2(z)=\frac{C_{ox}}{\pi r_0 \varepsilon_{si}}\left(V_{GS}-\phi_{ms,i}-\phi_s(z)\right) \quad (34)$$

Substituting $A_0(x), A_1(x)$ and $A_2(x)$ in the parabolic equation (28), we get

$$\frac{\partial^2 \phi_s(z)}{\partial z^2}-\frac{4C_{ox}}{\pi r_0 \varepsilon_{si}}\phi_s(x)=\eta \quad (35)$$

Where $\eta=\frac{qN_A}{\varepsilon_{si}}-\frac{1}{K_d^2}\left(V_{GS}-\phi_{ms,i}\right)$,

$K_d=\sqrt{\frac{\pi r_0 \varepsilon_{si}}{4C_{ox}}}$

The general solution of equation (35) is

$$\phi_s(z)=B_0\exp\left(\frac{z+L_1}{K_d}\right)+B_1\exp\left(-\frac{z+L_1}{K_d}\right)+\eta \quad (36)$$

The φ_s expression has to satisfy the boundary conditions as below

1. $\phi_s(0)=\varphi_{0s}$ (37)
2. $\phi_s(-L_1)=-V_T\ln\left(N_A/n_i\right)$ (38)
3. $\left.\frac{d\phi_s(z)}{dz}\right|_{z=-L_1}=0$ (39)

On applying the above boundary conditions from equation (37) to equation (39) in equation (36), the expression is obtained as

$$\phi_s(z)=\eta-\left(\left(\eta+V_T\ln\left(N_A/n_i\right)\right)\cosh\left(\frac{z+L_1}{K_d}\right)\right) \quad (40)$$

The length of the depletion region at the source is obtained from the potential model when z=0 in equation (36)

$$L_1=K_d\cosh^{-1}\left(\frac{\eta-\varphi_{0S}}{\eta-V_{F,S}}\right) \quad (41)$$

Where $V_{F,S}=-V_T\ln\left(\frac{N_A}{n_i}\right)$, equation (40) represents the depletion length L_1 depends on the gate to source voltage and through η and φ_{0s}

3.3. Modeling of Potential in the depletion region of Drain

For lower gate voltages the drain length cannot be neglected. Thus the modeling of potential at the drain depletion region is derived by neglecting the radial direction. The 1-D Poisson's equation in region (R3) is given as

$$\frac{\partial^2 \varphi_D(z)}{\partial z^2}=-\frac{qN_D}{\varepsilon_{si}} \qquad L_2 \le z \le L_2+L_3 \quad (42)$$

Where $\varphi_D(z)$ is electrostatic potential that refers to the Fermi level in drain region and N_D is the doping concentration of drain region. The fringing field is ignored in this modeling. The boundary conditions are

1. $\varphi_D(L_2)=\varphi_{0D}$ (43)
2. $\varphi_D(L_2+L_3)=V_{DS}+V_T\ln\left(\frac{N_D}{n_i}\right)$ (44)

On integrating equation (41) twice and applying boundary condition the following expression is obtained as

$$\varphi_D(z)=-\frac{qN_D}{2\varepsilon_{si}}(z-L_1-L_3)^2+\left(\frac{V_{F,D}-\varphi_{0D}}{L_3}-\frac{qN_DL_3}{2\varepsilon_{si}}\right)(z-L_2-L_3)+V_{F,D} \quad (45)$$

Where $V_{F,D}=V_{DS}+V_T\ln\left(N_D/n_i\right)$. The electric field in lateral direction approaches to zero at the right edge of drain depletion region.

$$\left.\frac{d\varphi_D(z)}{dz}\right|_{z=L_2+L_3} = 0 \tag{46}$$

The depletion length at the drain region is gained by the potential model

$$L_3 = \pm\sqrt{\frac{2\varepsilon_{si}}{qN_D}\left(V_{F,D} - \varphi_{0D}\right)} \tag{47}$$

3.4. Modeling of Drain Current

The drain current modeling is derived using Kane's Model. The minimum tunneling path length is taken into consideration for calculating tunneling current. The tunneling path is defined as path between conduction band energy point and valance band energy point at the tunneling junction where inter-band tunneling mechanism takes place. Its length show a discrepancy from shortest tunneling path (l_{short}) to longest tunneling path (l_{long}).

In Kane's Model, the band BTBT generation rate (G_{BTBT}) of carriers per unit volume per unit time is given as [29]

$$G_{BTBT} = \frac{A_{kane}}{\sqrt{E_g}} \cdot \left|E_{z,r}\right|^{\alpha} \cdot \exp\left(-B_{kane} \cdot \frac{E_g^{\frac{3}{2}}}{\left|E_{z,r}\right|}\right) \tag{48}$$

Where $\left|E_{z,r}\right|$ is the magnitude of electric field expressed as $\left|E_{z,r}\right| = \sqrt{E_z^2 + E_r^2}$, α is 2 for the direct and 2.5 for indirect band gap tunneling, A_{kane} and B_{kane} are the Kane's constant with values $A_{kane} = 3.5\times10^{21} eV^{0.5}/cm\ .s.\ V^2$ and $B_{kane} = 2.25\times10^{7} V/cm\ .\ eV^{1.5}$ [29][30].

The drain current is derived by integrating G_{BTBT} over the tunneling volume [31]

$$I_{BTBT} = \frac{qA_{kane}}{\sqrt{E_g}} \cdot \int_V E_z \ . \ E_{avg}^{\alpha-1} \cdot \exp\left(-B_{kane} \ . \ \frac{E_g^{\frac{3}{2}}}{E_{avg}}\right) dV \tag{49}$$

Since equation (47) represents the exponential function of electric field, radial term is neglected in G_{BTBT}. The channel lateral electrical field is obtained from the derivative of equation (20), which is expressed as

$$E_z(z,r) = \frac{\lambda}{r_0} \ . \left[C_0 \exp\left(\lambda \frac{z}{r_0}\right) - C_1 \exp\left(-\lambda \frac{z}{r_0}\right)\right] . \times J_0(\lambda \ . \ r) \tag{50}$$

E_{avg} Is an average electric field in the z-direction over the tunneling path and can be expressed as [31]

$$E_{avg} = \frac{E_g}{qL_T} \tag{51}$$

Where L_T is tunneling path length, substituting average and lateral electric field in equation (49)

Yields,

$$I_{BTBT} = \frac{2\pi\lambda qA_{kane}}{r_0\sqrt{E_g}} \int_0^{r_0} \int_{l_{short}}^{l_{long}} \left[C_0 \exp\left(\lambda \frac{z}{r_0}\right) - C_1 \exp\left(-\lambda \frac{z}{r_0}\right)\right] r J_0(\lambda \ . \ .r) \times \exp\left(-qB_{kane} E_g^{\frac{1}{2}} .. \ z\right) . \left(\frac{E_g}{qz}\right)^{\alpha-1} dzdr \tag{52}$$

The I_{BTBT} is calculated by integrating equation (52) over the exponential terms due

rapid change of exponential term than the polynomial term ($1/z^{\alpha-1}$)

$$I_{BTBT} = \frac{2\pi\lambda q A_{kane}}{r_0\sqrt{E_g}}\left(\frac{E_g}{q}\right)^{\alpha-1} \times \left[H(l_{short}) - H(l_{long})\right] \times \left(\frac{r_0}{\lambda}\right) \times . \; J_1(\lambda \, . \, r_0) \quad (53)$$

Where $H(z)$ is defined as

$$H(z) = \frac{1}{z^{\alpha-1}}\left(A_0 \exp\left[\frac{C_0}{A_0} z\right] + B_0 \exp\left[-\frac{C_1}{B_0} z\right]\right) \quad (54)$$

Where $A_0 = \dfrac{C_0}{\dfrac{\lambda}{r_0} - qB_{kane}E_g^{\frac{1}{2}}}$ and

$$B_0 = \frac{C_1}{\dfrac{\lambda}{r_0} + qB_{kane}E_g^{\frac{1}{2}}}$$

3.5 Modeling of transconductance

The transconductance is derived from drain current as

$$g_m = \frac{\partial I_{BTBT}}{\partial V_{GS}} \quad (55)$$

4. Result and Discussion

In this section, the results are plotted for the analytical modeling and validated using the ATLAS TCAD Simulation tool. The channel length of the proposed model is of 50 nm with source and drain length of 20 nm. The simulation models used for the simulation of the device are Concentration Dependent, Lombardi Model, Boltzmann, Shockley-Read-Hall, Auger and Band-to-Band.

Fig. 3. represents the surface potential profile along the channel length for gate to source voltage of 0 V and 1 V. It is studied that electron density across the channel increases with increase in gate voltage, especially near the drain region. The extension of drain/source depletion regions is observed at low/high gate voltages. The surface potential profile of model is close to the simulation results. Fig. 4. shows the surface potential profile along the channel length for different silicon thickness 13 nm, 14 nm and 15 nm. It is observed from plot that higher the thickness of silicon higher the surface potential value. As the thickness of silicon is high the electron density increase, due to which the conductivity increases along the channel, further increases the surface potential value.

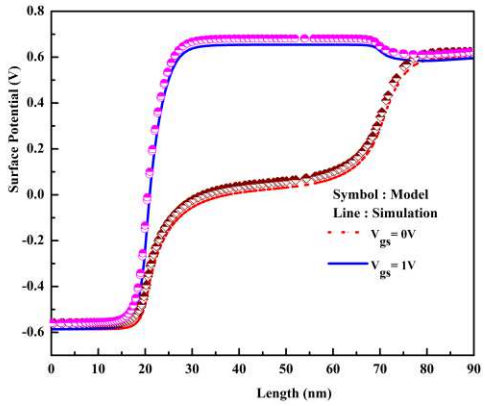

Fig. 3. Surface potential profile along the channel of the TFET for different V_{GS}

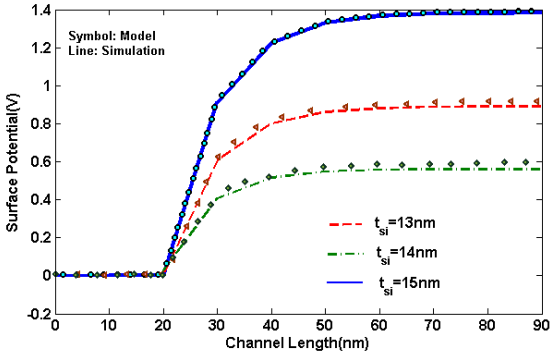

Fig. 4. Surface potential profile for different t_{si}

Fig. 5. depicts the surface potential profile along the channel for different drain voltages of 0 V and 1 V. Plot represents the variation of potential across the drain region and constant over the source and channel region. As the drain voltage is varied the potential profile changes across the drain region due to increase in carrier density. Fig. 6. comparison plot of lateral electric field profile for with high-k and without high-k GAA HJTFET. It is studied that the high-k stacked GAA HJTFET has higher electric field profile than GAA TFET. The peak across the source and channel region is due to variation of the potential. The peak is low at the drain to channel region of high-k GAA HJ TFET than GAA TFET. Figure 7 shows the comparison of drain current variation with the gate voltage, it is observed that high-k stacked GAA-HJTFET is having higher drain current than GAA-HJTFET due to the higher tunneling rate.

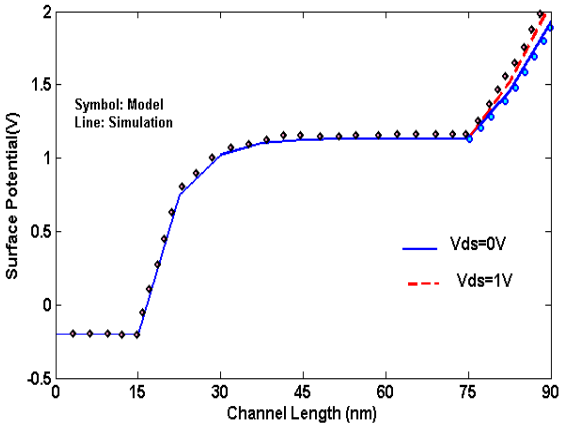

Fig. 5. Surface potential profile along the channel length for different V_{DS}

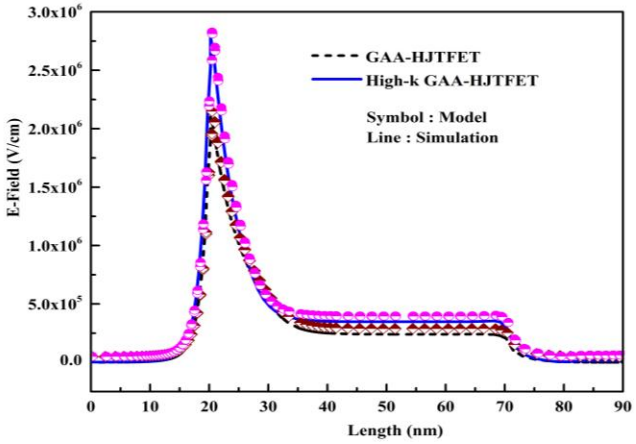

Fig. 6. Comparison plot of Electric Field profile along the channel

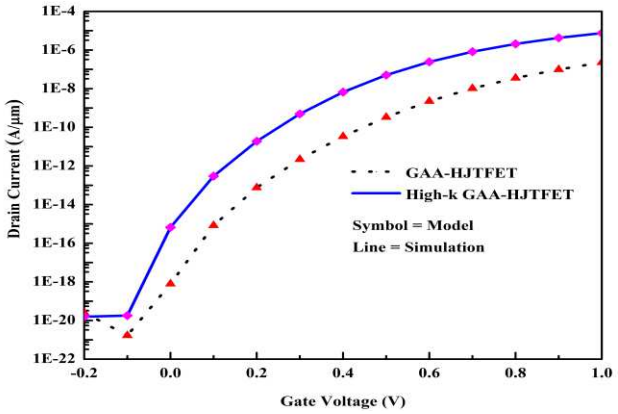

Fig. 7. Comparison I_D vs V_{GS} with and without high-k GAA-HJTFET

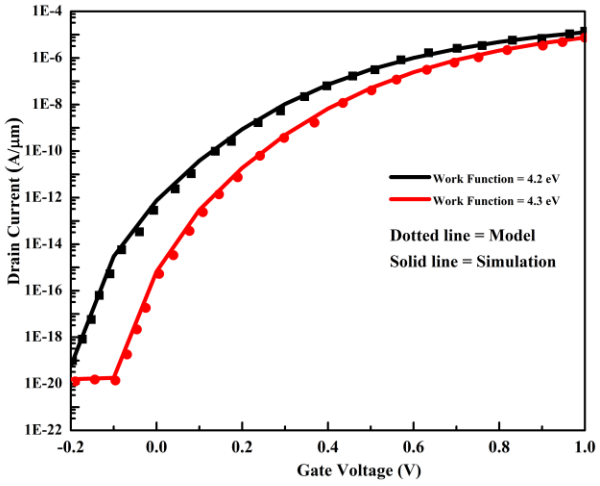

Fig. 8. I_D vs V_{GS} for different work function

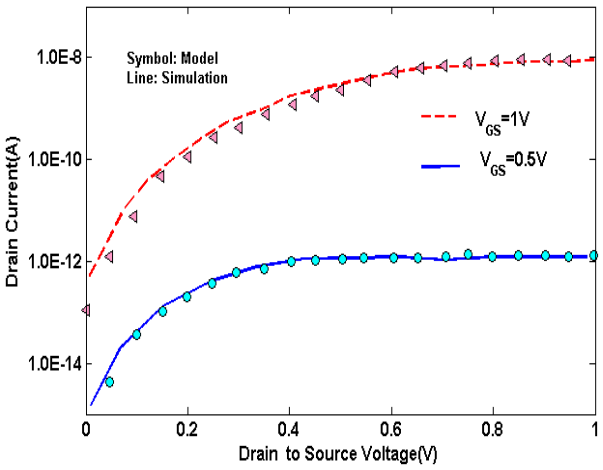

Fig. 9. I_D vs V_{DS} for the proposed device at different V_{GS}

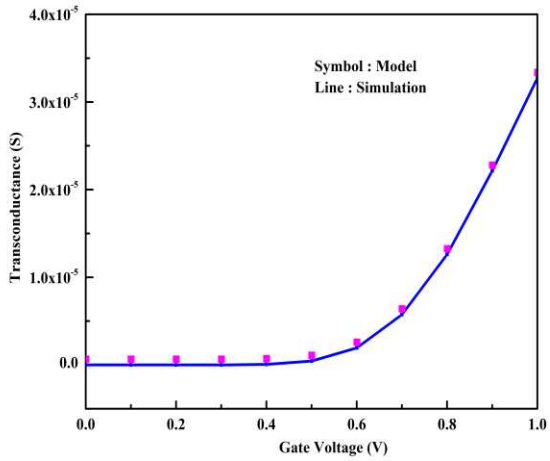

Fig. 10. g_m vs V_{GS} of the proposed device

Fig. 8. depicts the drain current variations with gate voltage for different work functions of 4.2 eV and 4.3 eV. It is observed that OFF-state current is low and ON-state current is high, thus the I_{ON}/I_{OFF} ratio is high of 10^{15}. Fig. 9. shows the drain current variation with drain voltage for different gate voltages of 0.5 V and 1 V. It represents that higher the gate to source voltage higher the drain current. Fig.10. shows the transconductance variation with the gate voltage. The transconductance is high for the high-k stacked GAA-HJTFET which in turn increases the sensitivity of the device operation.

5. Conclusion

In this paper, analytical modeling of high-k stacked GAA-HJTFET is developed. First the electrostatic potential modeling of high-k GAA-HJTFET is considered. To enhance the performance and reliability of model compared to previously reported devices the charge carriers across the depletion regions and channel were taken into account. The analysis is accomplished considering three depletion regions such as channel, source and drain. The analytical modeling in the channel is derived using the superposition technique, in which 1-D Poison's and 2-D Poison's equations are considered. The modeling in the source region is derived using 2-D Poison's equation with the parabolic approximation techniques. The drain region is modeled using the 1-D Poison's equation. The potential distribution modeling is used to develop the lateral electric field, minimum tunneling length and current of the model proposed. The drain current is modeled using the Kane's Model, in which the drain current is derived by integrating the BTBT generation rate. The results plotted showed the excellent match with the simulation results. The model suggested is appropriate for the low-power VLSI applications.

Appendix A

Using the continuity of lateral electric field across the source/channel interface, the potential φ_{0S} is expressed as

$$\left.\frac{d\phi_s(z)}{dz}\right|_{z=0} = \left.\frac{\partial\varphi_C(z,\ r=r_0)}{\partial x}\right|_{z=0} \qquad \text{(A1)}$$

From equation (A1), we obtain

$$-\frac{1}{k_d}\left(\phi_0 + V_T \ln\left(\frac{N_A}{n_i}\right)\right)\sinh\left(\frac{L_1}{k_d}\right) = \frac{\lambda}{r_0}(C_0 - C_1)J_0(\lambda \,.\, r_0) \quad \text{(A2)}$$

Using the continuity of lateral electric field across the drain/channel interface, the potential φ_{0D} is expressed as

$$\left.\frac{\partial \varphi_C(z, r = r_0)}{\partial z}\right|_{z=L_2} = \left.\frac{d\varphi_D(z)}{dz}\right|_{z=L_2} \quad \text{(A3)}$$

From equation (A3) we obtain

$$\frac{V_{F,D} - \varphi_{0D}}{L_3} + \frac{qN_D L_3}{2\varepsilon_{si}} = \frac{\lambda}{r_0}\left(C_0 \exp\left(\frac{\lambda L_2}{r_0}\right) - C_1 \exp\left(-\frac{\lambda L_2}{r_0}\right)\right)J_0(\lambda \,.\, r_0) \quad \text{(A4)}$$

Further simplifying using (A2) and (A4) the φ_{0S} and φ_{0D} are solved to obtain expressions.

Appendix B

Substituting potential model equation (20) in the boundary condition equation (17), we get

$$\sum_{m=1}^{\infty}(C_0 + C_1)J_0\left(\frac{\lambda_m}{r_0} r\right) = \varphi_{0S} - \varphi_{1D}(r) \quad \text{(B1)}$$

The above equation is solved by Fourier-Bessel series

$$C_0 + C_1 = \frac{1}{N}\left(\varphi_{0S}\,\frac{J_1(\lambda)}{\lambda} - V_a\right) \quad \text{(B2)}$$

Where

$$V_a = \frac{1}{r_0^2}\int_0^{r_0} r\; r\; \varphi_{1D}(r) \,.\, J_0\left(\frac{\lambda}{r_0} \,.\, r\right) . \, dr \quad \text{(B3)}$$

Similarly using boundary condition equation (18) we get

$$\sum_{m=1}^{\infty}\left[C_0 \exp\left(\frac{\lambda_m L_2}{r_0}\right) + C_1 \exp\left(-\frac{\lambda_m L_2}{r_0}\right)\right] \times J_0\left(\frac{\lambda_m}{r_0} r\right) = \varphi_{0D} - \varphi_{1D} \quad \text{(B4)}$$

and

$$C_0 \exp\left(\frac{\lambda L_2}{r_0}\right) + C_1\left(-\frac{\lambda L_2}{r_0}\right) = \frac{1}{N}\left(\varphi_{0D}\,\frac{J_1(\lambda)}{\lambda} - V_a\right) \quad \text{(B5)}$$

The C_0 and C_1 can also be obtained from (B2) and (B5)

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