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Electrostatic Force Assisted Exfoliation of Prepatterned Few-Layer Graphenes into Device Sites

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ABSTRACT

We present a novel fabrication method for incorporating nanometer to micrometer scale few-layer graphene (FLG) features onto substrates with electrostatic exfoliation. We pattern highly oriented pyrolytic graphite using standard lithographic techniques and subsequently, in a single step, exfoliate and transfer-print the prepatterned FLG features onto a silicon wafer using electrostatic force. We have successfully demonstrated the exfoliation/printing of 18 nm wide FLG nanolines and periodic arrays of 1.4 μm diameter pillars. Furthermore, we have fabricated graphene nanoribbon transistors using the patterned graphene nanoline. Our electrostatic force assisted exfoliation/print process does not need additional adhesion layers and could be stepped and repeated to deliver the prepatterned graphitic material over wafer-sized areas and allows the construction of graphene-based integrated circuits.

Recently, few-layer graphene (FLG) has been extensively studied as a material for making future electronic devices. FLG has exceptional properties, such as high carrier mobility (up to 20000 $cm^2/(V\ s)$), high saturation velocities, a stable two-dimensional (2D) crystal structure, potential to realize ballistic transport at room temperature, and processing compatibility with state-of-the-art silicon technology.[1−3] Graphene-based electronic devices have been fabricated to study its superior transport properties.[4−9] Two of the challenges to making commercially viable graphene-based electronics are incorporating FLG material over large areas and fabricating nanoscale features to achieve the desired electronic properties (e.g., to open band gap in the electronic structure of graphene). Several approaches have been attempted to produce graphene for large area electronics, including epitaxial growth,[10−13] transfer-printing,[6,14] and solution-based deposition.[15,16] At the same time, efforts have been made to tailor graphene sheets into nanoscale features (e.g., nanoribbons).[8,17−19] Obviously, a method to simultaneously achieve nanoscale features over large areas would be a benefit to graphene-based electronics fabrication.

In this Letter, we demonstrate a novel micro and nano fabrication process for exfoliating and printing FLG over large areas, termed electrostatic force-assisted exfoliation of prepatterned graphene (EFEG). In this approach, ordered nano- and microscale FLG features are exfoliated from a prepatterned, pristine, HOPG surface and printed on a regular semiconductor substrate (e.g., Si) by applying an electrostatic force. Such electrically exfoliated FLG flakes can be used to make working transistors showing good performance. In the future, this novel technique in combination with other nanolithography approaches may be employed to fabricate graphene-based large-scale integrated (LSI) circuits.

Figure 1 shows the schematic flowchart of electrostatic force assisted exfoliation of graphenes (EFEG). First, nanometer and micrometer scale relief features are patterned on the surface of a highly oriented pyrolytic graphite (HOPG) disk by using lithographic techniques followed with reactive ion etching (RIE) (Figure 1a). This structured HOPG disk serves as a template and is brought into contact with a SiO_2/Si substrate. A voltage between HOPG and semiconducting Si produces an electrostatic attraction force acting between the surface of prepatterned graphitic features and the silicon substrate (Figure 1b). As the HOPG template is vertically moved away from the substrate, the electrostatic force exfoliates the prepatterned few-layer graphenes and attaches them onto the SiO_2 surface (Figure 1c). The thin screening depth in HOPG (less than 0.5 nm) assures that the electrostatic force in the EFEG process acts only on the outmost graphene monolayers during each exfoliation/print cycle.[3] Such a highly localized drag force can modify the flatness or morphology of the outmost graphene layers and make them conformal to the flat substrate, but it barely affects the rest of the graphene layers in the graphite bulk. As a result, the boundary between electrically dragged graphene layers

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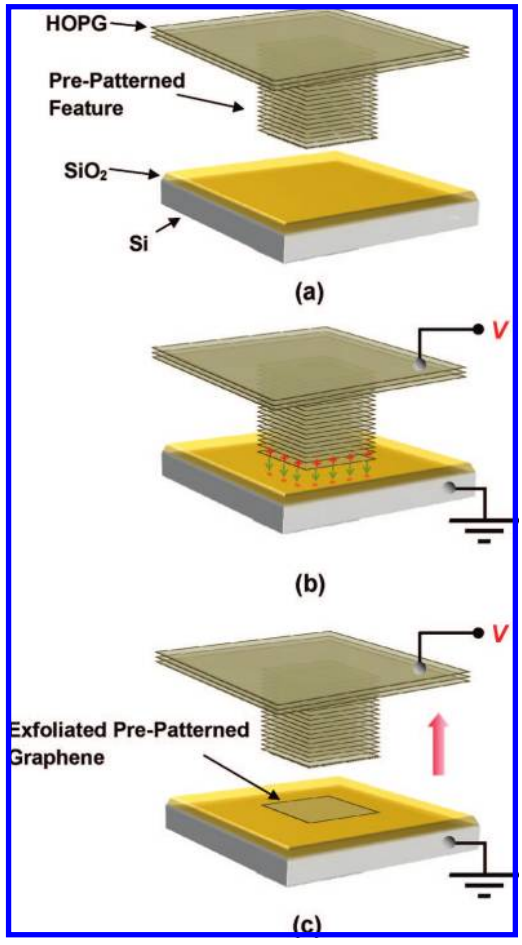

Figure 1. Schematic flowchart of electrostatic force assisted exfoliation of prepatterned few-layer graphenes (EFEG), which includes (a) initial setup with a HOPG template bearing prepatterned relief features, (b) application of a voltage between the HOPG template and the Si substrate after they are brought into contact, and (c) exfoliation of prepatterned few-layer graphenes by electrostatic force as the HOPG template is separated from the substrate. In EFEG, due to the thin screening depth in graphite (<0.5 nm), only several outmost graphene monolayers are dragged by the electrostatic force, preferably leading to a thin exfoliation thickness of FLGs.

and the rest of the layers likely serves as an exfoliating site because of modified interlayer spacing and accordingly weakened binding force. Therefore, it is expected that the EFEG process favorably produces thin exfoliated FLG flakes. The pristine FLG features, once exfoliated and printed onto substrate surface, can remain the original pattern arrangement predefined on the HOPG template. This exfoliation/print approach does not need any additional adhesive layer and could be repeated to print prepatterned graphitic features over the whole wafer area. Furthermore, with using prepatterned align marks, EFEG could also be used to place graphene nanostructures into specific locations with nanometer scale precision.

For the EFEG process, HOPG disks (SPI, Inc., 1 cm^2) were exfoliated with flexible Scotch tape to achieve a flat and pristine graphite surface. In order to fabricate microscale relief features on the graphite disk, a 1.3 μm thick photoresist layer was spun onto the HOPG surface and exposed on an ABM contact printer. After development, the features were etched into the HOPG using an O_2-based RIE recipe with an etching rate of ~50 nm/min. Finally, the photoresist was removed by soaking the HOPG disk in acetone for 10 min. The nanoscale graphitic features were fabricated using electron beam induced deposition (EBID) followed by RIE. A SiO_x mask was patterned using a Zeiss XB 1540 focused ion beam/SEM etching/deposition system equipped with an XENOS pattern generator. The 15−50 nm wide SiO_x nanolines were deposited onto the pristine graphite surface irradiated by a 20 keV electron beam. Afterward, the nanoscale graphitic features were etched with the same O_2 plasma recipe with the SiO_x features acting as the etching mask. Finally, the SiO_x mask was removed in a diluted hydrofluoric acid solution. The EFEG process was used to exfoliate and print the FLG features onto a Si substrate coated with 50 nm thick SiO_2, thermally grown in a Tystar oven at 1000 °C. For the exfoliation/printing process, the HOPG template and the SiO_2/Si substrate were clamped between a pair of homemade parallel plates, and a B&K Precision model 1715 dc power supply (0−50 V) was used to apply voltage between plates. In addition, an atomic scanning microscope (Veeco caliber SPM−AFM) was employed to measure the thickness of exfoliated FLG features in the tapping mode.

To determine the field strengths needed for performing the EFEG process, the electrostatic exfoliation process was simulated using commercially distributed software (Ansoft Maxwell SV). Figure 2a visualizes the 2D simulation model, in which a graphite template bearing a 1 μm diameter, 0.5 μm high pillar is pressed against a silicon substrate coated with 50 nm thick SiO_2, and a dc voltage is applied between the HOPG template and the silicon substrate. The field distribution and the total electrostatic force were solved using a finite element analysis (FEA). Figure 2b plots the electrostatic strength (megapascals) acting on the graphite surface as a function of the average field magnitude in the SiO_2 layer, which is compared with the exfoliation strength of graphenes that is defined as the minimum stress required for fully separating a graphene monolayer from the bulk graphite (~0.4 MPa marked by the dashed line).[20−22] Figure 2b indicates that the minimum field magnitude required to exfoliate graphene flakes is ~1.7 MV/cm, which is far below the typical breakdown limit of thermally grown SiO_2 (~10 MV/cm) and thus should not result in electrical damage. Given a SiO_2 thickness of 50 nm, Figure 2c plots the electrostatic strength versus applied voltage, which indicates that the minimum voltage required for graphene exfoliation is about 8.5 V for this particular setup.

Figure 3 shows scanning electron micrographs (SEMs) of raised microscale and nanoscale features patterned on a HOPG disk by using either photolithography or electron beam induced deposition (EBID) followed with RIE, which include periodic pillars with average diameter of 1.4 μm (Figure 3, panels a and b) and 15 nm wide nanolines (Figure 3c). The heights of microscale and nanoscale features are about 0.5 μm and 40 nm, respectively. The high-magnification SEMs in panels b and c of Figure 3 display that the

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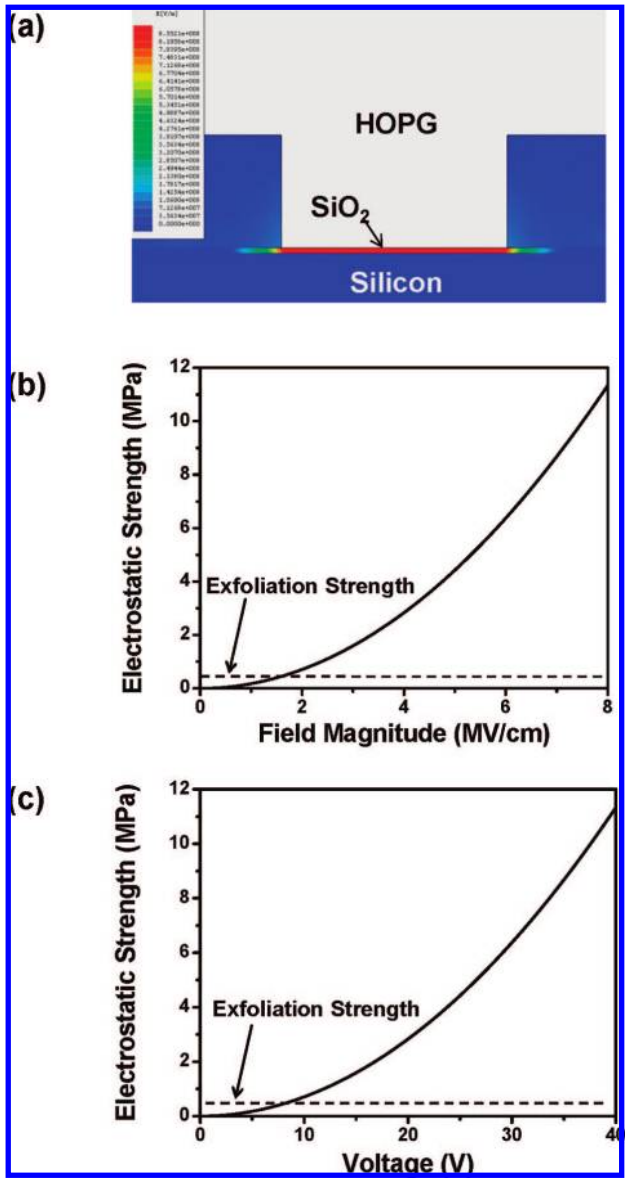

Figure 2. (a) A 2D simulation model of EFEG, in which a graphite template bearing a 1 μm diameter, 0.5 μm high pillar is pressed against a silicon substrate coated with 50 nm thick SiO_2, and a voltage is applied between the HOPG template and the substrate to create electric field and electrostatic force. The simulation was performed to calculate electrostatic strength acting on the graphite surface as a function of (b) field magnitude in the SiO_2 layer and (c) voltage. The dashed line marks the required exfoliation strength for separating a graphene monolayer from the graphite surface (~0.4 MPa).

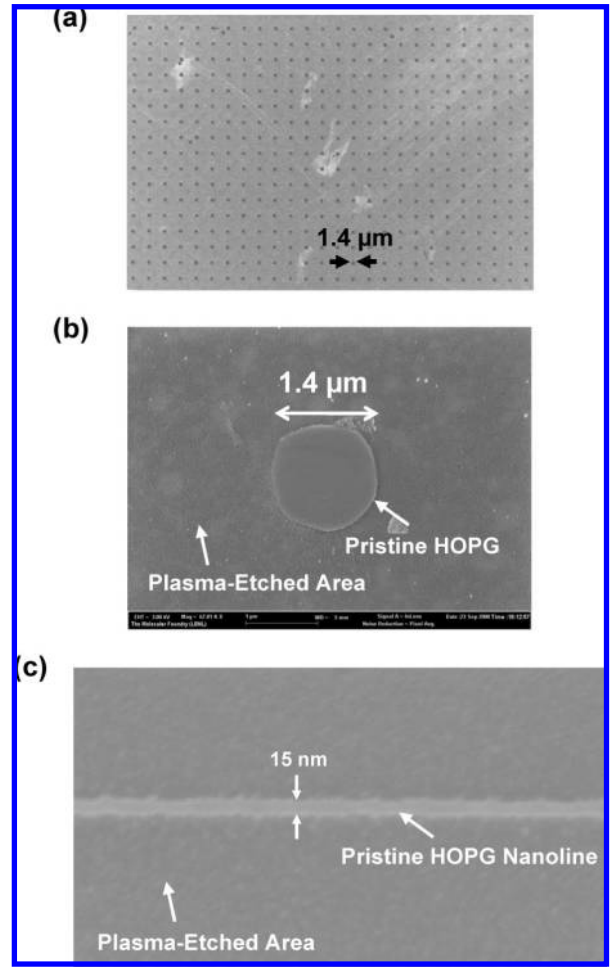

Figure 3. Scanning electron microscopy (SEM) images of relief features prepatterned on a pristine HOPG surface, which include (a) array of 1.4 μm diameter pillars, (b) zoomed view of an individual 1.4 μm diameter, 0.5 μm high pillar, and (c) a 15 nm wide, 40 nm high nanoline. The microscale and nanoscale features were patterned by photolithography and electron-beam-induced deposition (EBID) followed with O_2-based RIE, respectively.

O_2-plasma-etched area has a higher roughness than a pristinie HOPG surface, and this is attributed to the oxidation of graphite surface.[23,24] However, the feature area protected by the etching masks (photoresist or SiO_x) is still as smooth as a pristine graphite surface. This should yield a conformal contact with the flat substrate during an EFEG process and therefore a high transfer-printing efficiency of graphene.

Figure 4 shows the SEMs of microscale and nanoscale FLG features electrically exfoliated and printed on a SiO_2 surface by EFEG. Figure 4a shows a low-magnification SEM of the array of 1.4 μm diameter FLG pillars. We attribute the grayscale variation of the graphitic flakes over the large area to the variation of FLG thickness over the wafer and/or the ripples in the surface of graphene. We analyzed these variations using atomic force microscopy (AFM) which is described subsequently. Figure 4a demonstrates that the EFEG process can exfoliate and print graphitic material over large areas without using any adhesion coating layer, and the exfoliated flake can retain the arrangement and periodicity of the original pattern on the HOPG template. The high-magnification SEM in Figure 4b shows the zoomed view of an exemplary FLG pillar, which shows that most of the area of the flake was conformably adhered to the flat SiO_2 surface by electrostatic force despite a partially wrapped edge. We believe this arises due to the interlayer drag force in the graphite during the graphene exfoliation. Figure 4c shows the SEM of 18 nm wide, 1.5 μm long graphene nanolines with a spacing of 300 nm printed on the same SiO_2 surface, and Figure 4d shows the zoomed view of an individual 18 nm wide graphene nanoline, which demonstrates that the EFEG process is also capable of directly incorporating nanoscale pre-engineered graphene features (e.g., nanoribbons) into device sites (e.g., transistors). So far the maximum

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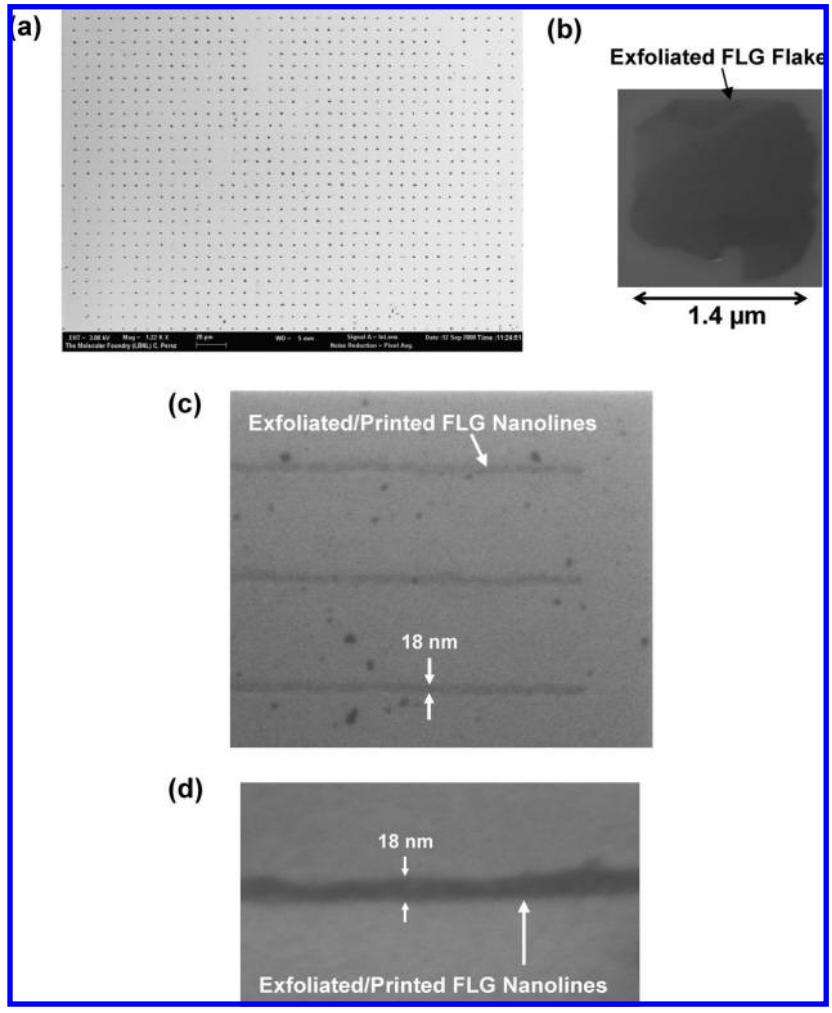

Figure 4. SEM images of exfoliated and printed prepatterned FLG features on a SiO_2/Si substrate by using EFEG, which include (a) an array of 1.4 μm diameter FLG pillars, (b) a zoomed view of an exemplary 1.4 μm FLG pillar, (c) 18 nm wide graphene nanolines, and (d) a zoomed view of an individual 18 nm wide graphene nanoline.

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SiO_2 area incorporated with graphene is limited by our HOPG disk area, but the EFEG process could be performed in a step-and-repeat fashion to extend the total processing area. In addition, as a control experiment, we performed the transfer-printing of prepatterned FLGs on the same SiO_2 surface without applying the electric field, and we found that the area incorporated with FLG flakes is about 2 orders of magnitude smaller than that generated by EFEG. Therefore, we conclude that the electrostatic force indeed plays a critical role in the exfoliation of graphene features from the HOPG template.

AFM images were obtained to measure the thickness of exfoliated FLG features, and the thickness value was interpreted into the number of graphene monolayers on the basis of the recent work by Nemes-Incze et al.[25] Figure 5a shows the AFM image of an individual 1.4 μm wide FLG flake printed on the SiO_2 surface. The AFM image clearly displays a variation of FLG thickness over the whole flake. We pose three possible causes for this variation: (1) the folding or wrapping of graphene edge, (2) the variation of the number of graphene monolayers over the whole FLG flake, and (3) the rippling of the graphene surface generated during the printing/exfoliation course. The scanline denoted by the solid line and accordingly plotted in Figure 5b explicitly exhibits a variation of FLG thickness from t_{min} = 0.72 nm (1 monolayer) to t_{max} = 1.94 nm (5 monolayers) with an average value of t_{avg} = 1.54 nm (4 monolayers) (standard deviation σ = 0.25 nm). Furthermore, the average thickness data of 135 1.4 μm wide FLG flakes exfoliated in a single EFEG cycle is presented as a stacked column chart (Figure 5c). Figure 5c shows an interflake variation of the average FLG thickness over the whole printed area ($\sim$1 cm^2), which ranges from 0.5 nm (1 monolayer) to 30 nm (87 layers) with a most-likely value of $\sim$2.7 nm (7 layers), average thickness of 4.5 nm (12 layers) (standard deviation of 3.0 nm).

In order to evaluate the electronic characteristic of FLGs exfoliated and printed with the EFEG process, we fabricated graphene nanoribbon field effect transistors (GFETs) using exfoliated FLG nanolines on SiO_2/Si substrates. In our specific fabrication, a cross-beam system equipped with a pattern generator was used to deposit platinum finger contacts to define drain/source contacts on FLG nanolines, which also connect the graphene channel with the large metal contact pads (4 nm Cr/75 nm Au), which are fabricated by photolithography followed with lift-off in acetone after the

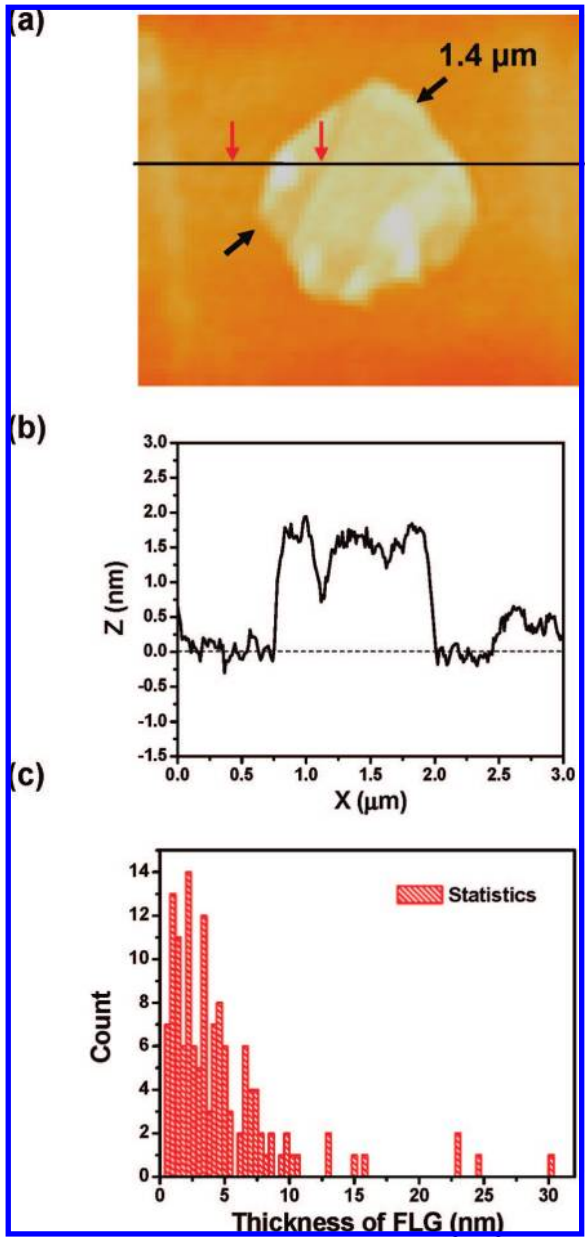

Figure 5. (a) An atomic force microscopy (AFM) image of a 1.4 μm diameter FLG flake exfoliated and printed on the SiO_2 surface. The solid line indicates a scanning trace across the flake, which is also plotted in (b). (c) The stacked column chart of the average thickness data collected from 135 exfoliated/printed 1.4 μm wide FLG flakes on SiO_2 surface.

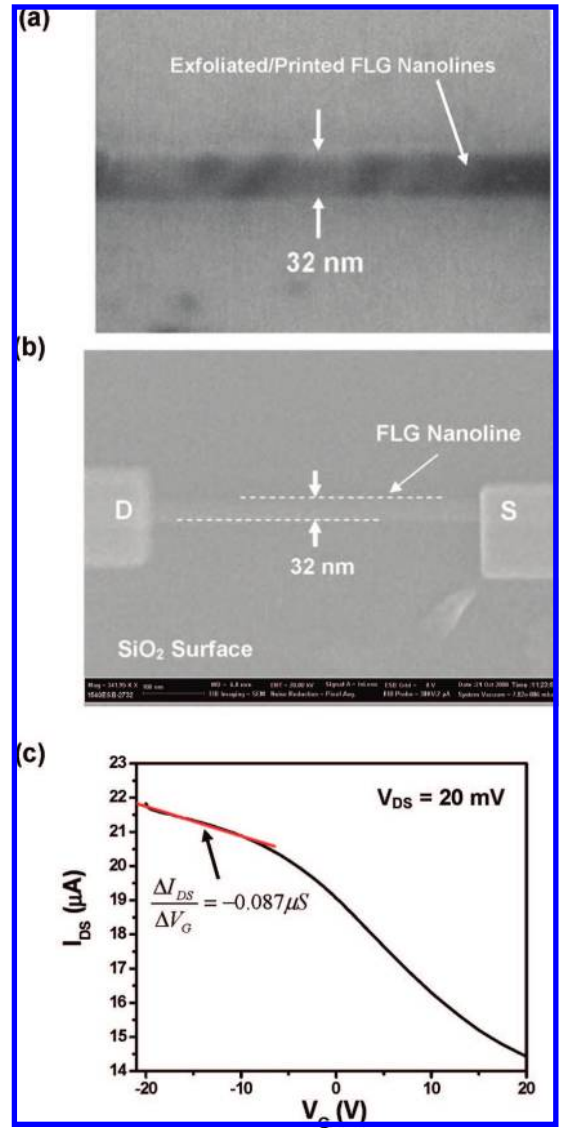

Figure 6. (a) A SEM image of an as-exfoliated 32 nm wide FLG nanoline. (b) A SEM image of a back-gated graphene field-effect transistor with channel width of 32 nm, channel length of 0.53 μm, gate dielectric (SiO_2) thickness of 50 nm, in which platinum finger contacts were deposited as drain and source contacts, and the silicon substrate serves as a back gate. (c) Drain−source current I_{DS} as a function of gate voltage V_G under a fixed drain−source voltage V_{DS} = 20 mV.

EFEG process. Finally, another metallic contact is made onto the Si substrate, which serves as a back gate contact. Figure 6a shows the SEM of an as-exfoliated 32 nm wide FLG nanoline, which was used to fabricate a back-gated graphene nanoribbon FET with channel length of L = 0.53 μm and gate dielectric thickness of d = 50 nm, as shown in Figure 6b. The device characteristic curves of this GFET device were measured using an Agilent-4155 semiconductor parameter analyzer. Figure 6c plots the drain−source current (I_{DS}) as a function of the gate voltage (V_G) under a fixed drain−source voltage (V_{DS} = 20 mV). As shown in Figure 6c, this back-gated graphene nanoribbon FET exhibits a typical gate modulation behavior for the hole-dominated conduction in the range of V_G from V_G = −20 to 20 V (field magnitude ξ = −4 to 4 MV/cm), and the curve slope value (or transconductance) at the linear region was obtained to be $\Delta I_{DS}/\Delta V_G$ = −0.087 μS by the linear fitting (denoted with the red solid line). The hole mobility was subsequently extracted to be μ_h = 1,050 $cm^2/(V\ s)$ by using eq 1, where ε_0 is the vacuum permittivity; $\varepsilon_r \sim 3.9$ is the dielectric constant of SiO_2; C_{ox} is the gate capacitance; w/L is the width/length ratio of the graphene channel.[26] This hole mobility value is among the highest mobility values reported for few-layer graphenes contacting a supporting material surface[4,5,8,9,15,27] and indicates that the EFEG approach can be used to build nanoscale graphene devices with excellent performance. For our GFETs, we do not observe electron conduction in the range of V_G from −20 to 20 V. The loss

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of electron conduction may be attributed to the unexpected contamination of HOPG during the material handling, which may shift the bipolar transition point out of the measurement range.[5,6,8]

$$\mu = \frac{\Delta I_{DS}}{C_{ox}\frac{W}{L}V_{DS}\Delta V_G} \quad (1)$$

$$C_{ox} = \frac{\varepsilon_0 \varepsilon_r}{d}$$

In summary, we developed and demonstrated a novel approach for printing prepatterned few-layer graphenes into the device locations, named as electrostatic-force-assisted exfoliation of few-layer graphenes (EFEG). In this process, the microscale and nanoscale features are prepatterned onto a HOPG disk, which serves as both a template and source of material. When the HOPG template is brought into a conformal contact with a Si substrate coated with SiO_2, a voltage is applied between HOPG and Si that generates an electrostatic force, which can exfoliate the prepatterned FLG features as the HOPG template is removed. With this approach, we have successfully demonstrated the exfoliation/printing of FLG features with critical dimensions ranging from 18 nm to 1.4 μm. In addition, the electrically printed FLG flakes have been used to build graphene nanoribbon transistors with excellent performance. This novel printing approach does not need any additional adhesion layer and can be repeatedly performed to incorporate graphitic materials over a large area in a parallel fashion.

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