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***Abstract*—The electrostatics of nanowire transistors are studied by solving the Poisson equation self-consistently with the equilibrium carrier statistics of the nanowire. For a one-dimensional, intrinsic nanowire channel, charge transfer from the metal contacts is important. We examine how the charge transfer depends on the insulator and the metal/semiconductor Schottky barrier height. We also show that charge density on the nanowire is a sensitive function of the contact geometry. For a nanowire transistor with large gate underlaps, charge transferred from bulk electrodes can effectively "dope" the intrinsic, ungated region and allow the transistor to operate. Reducing the gate oxide thickness and the source/drain contact size decreases the length by which the source/drain electric field penetrates into the channel, thereby, improving the transistor characteristics.**

***Index Terms*—Electrostatic analysis, nanotecnology, transistors.**

I. Introduction

With the scaling limit of conventional silicon transistors in sight, there is rapidly growing interest in nanowire transistors with one-dimensional (1-D) channels, such as carbon nanotube transistors [1], [2] and silicon nanowire transistors [3]. Due to the 1-D channel geometry, the electrostatics of nanowire devices can be quite different from bulk silicon devices. Previous studies of carbon nanotube p/n junctions and metal/semiconductor junctions demonstrated unique properties of nanotube junctions [4]–[6]. For example, the charge transfer into the nanowire channel from the metal contacts (or heavily doped semiconductor contacts) can be significant [4], [5].

In this paper, we extend previous studies by looking at the dependence of the charge transfer on the metal/semiconductor Schottky barrier height, the insulator dielectric constant, and the metal contact geometry. We show that if an intrinsic nanowire is attached to bulk metal contacts at two ends, large charge transfer can be achieved if the Schottky barrier is low and the insulator dielectric constant is high. If, however, the intrinsic nanowire is attached to 1-D metal contacts, the charge density on the nanowire depends critically on the electrostatic environment rather than the properties of the metal contacts. Reducing the gate oxide thickness and the contact size decreases the distance over which the source/drain field penetrates into the nanowire channel and can, therefore, help to suppress the short channel effects and improve the transistor performance.

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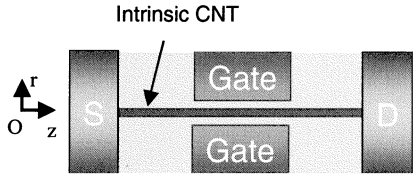

Fig. 1. Modeled, coaxially gated carbon nanotube transistor. The intrinsic nanotube channel has a diameter of 1.4 nm and the flat band voltage of the gate is zero. The cylindrical coordinates for solving the Poisson equation is also shown.

II. Approach

We simulated the coaxially gated carbon nanotube transistor shown in Fig. 1. Although the calculations are for carbon nanotube transistors, the general conclusion should apply to other nanowire transistors with 1-D channels. The equilibrium band profile and charge density were obtained by solving the Poisson equation in cylindrical coordinates self-consistently with the equilibrium carrier statistics of the carbon nanotube. The charge density per unit length on the nanotube, $Q_L(z)$, is calculated by integrating the "universal" nanotube density-of-states (DOS) [7], $D(E)$, over all energies

$$Q_L(z) = (-e) \cdot \int_{-\infty}^{+\infty} dE \cdot \mathrm{sgn}(E) D(E) \times f(\mathrm{sgn}(E)[E - \tilde{E}_F(z)]) \quad (1)$$

where e is the electron charge, $\mathrm{sgn}(E)$ is the sign function, and $\tilde{E}_F(z) = E_F - E_m(z)$ is the Fermi energy level minus the middle gap energy of the nanotube, $E_m(z)$. Since the source/drain electrodes are grounded, the Fermi level is set to zero, $E_F = 0$. The nanotube middle gap energy is computed from the electrostatic potential at the nanotube shell, $E_m(z) = -eV(z, r = r_{\mathrm{cnt}})$, where r_{cnt} is the nanotube radius. The electrostatic potential V satisfies the Poisson equation

$$\nabla^2 V(z, r) = -\frac{\rho}{\varepsilon} \quad (2)$$

where ρ is the charge density, ε is the dielectric constant. The following boundary conditions were used:

$V = (Eg/2 - \phi_{\mathrm{bn}})/e$ at the left metal contact;
$V = (E_g/2 - \phi_{\mathrm{bn}})/e$ at the right metal contact;
$V = V_G$ at the gate cylinder (the flat band voltage is assumed to be zero)

Also, E_g is the nanotube bandgap, ϕ_{bn} is the Schottky barrier height for electrons between the source/drain and the nanotube, and V_G is the gate voltage.

We numerically solved the Poisson equation by two methods: 1) the finite difference method and 2) the method of moments

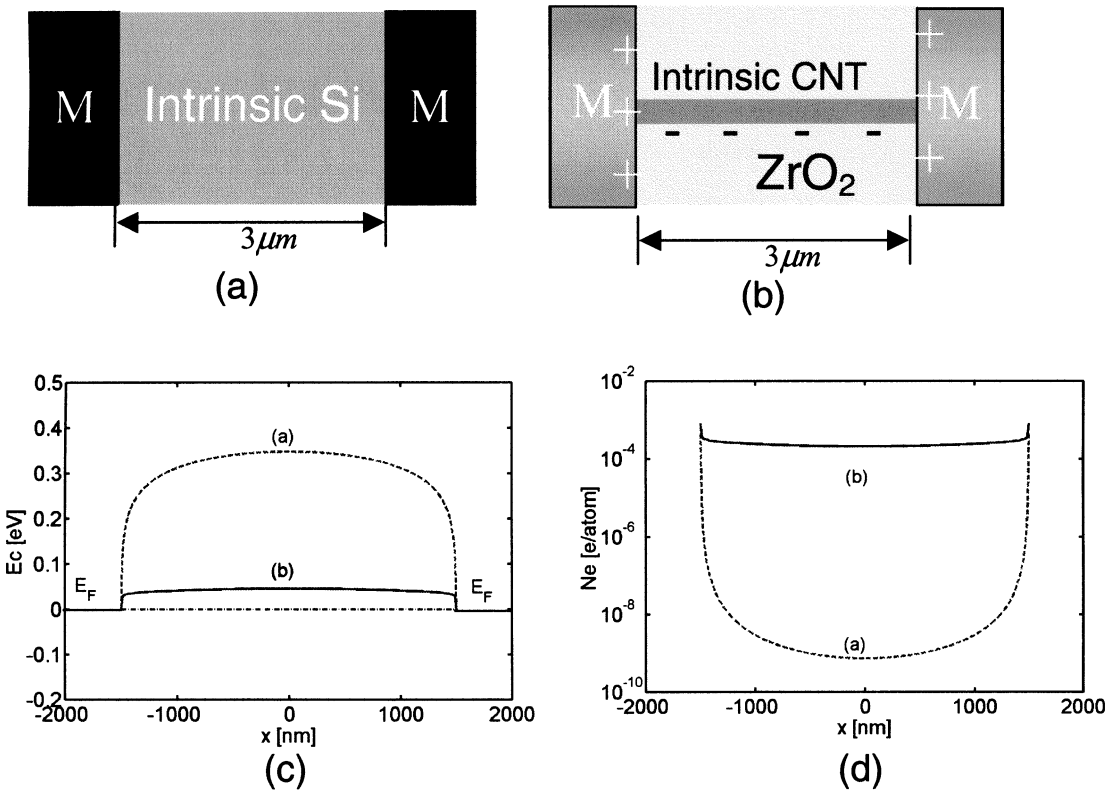

Fig. 2. Schematic plots for (a) a bulk Si structure where the cross-sectional area is assumed to be large and (b) a carbon nanotube channel between bulk metal electrodes. The Schottky barrier heights for electrons are zero. (c) The conduction band edge and (d) the electron density in the units of doping fraction. Results for the bulk Si structure are shown as dashed lines and for the nanotube as solid lines.

[8]. In order to improve the convergence when iteratively solving (1) and (2), the Netwton–Ralphson method (with details in [9]) was used. The results obtained by the finite difference method and by the method of moments agree well.

III. Results

We first compare the charge transfer from bulk contacts to the 1-D carbon nanotube to the charge transfer to a bulk silicon channel. We simulated two cases: 1) an intrinsic bulk Si channel sandwiched between two metal contacts as shown in Fig. 2(a) and 2) an intrinsic carbon nanotube channel between metal contacts as shown in Fig. 2(b). In both cases, the Schottky barrier heights between the metal contacts and the semiconductor channel are zero, which aligns the metal Fermi level of to the conduction band edge of the semiconductor. Electrons are transferred from metal contacts into the intrinsic channel due to the work function difference between the metal and the semiconductor. Fig. 2(c) plots the conduction bands, and Fig. 2(d) plots the charge densities in the unit of electron per atom for the bulk Si and nanotube channel. Compared to the bulk Si channel, the barrier in the nanotube is much lower, and the charge density is much higher. Although the nanotube is 3 μm long, the charge density at the center of the tube is still as high as 10^{-4}e/atom, about five orders of magnitude higher than that of the bulk Si in terms of electron fraction. As the result, the carbon nanotube channel is more conductive.

The charge transfer to the tube is significant because the charge on tube doesn't effectively screen the potential produced by the bulk contacts. Compared to the bulk channel, the charge element on the nanotube only changes potential locally. For example, in the bulk channel, the charge element is a two-dimensional sheet charge, which produces a constant field. The charge dipole formed by charge sheet in bulk Si and metal contacts shifts the potential far away. In contrast, for the nanowire channel, the charge element is a point charge, which produces a potential decaying with distance $\sim 1/r$ and has little effect far away (the potential of a point charge dipole decays even faster as $\sim 1/r^2$) [4]. As the result, for the 1-D channel, the potential produced by the bulk contacts is not screened by the charge on the nanotube near the metal/semiconductor interface. The bulk contacts tend to put the conduction band edge near the Fermi level over the whole 3-μm-long tube if the metal/CNT barrier height is zero.

We next estimate the charge density in the channel. The estimation provides a simple way to understand how the charge density of the tube varies with the contact and insulator properties. For the device structure shown in Fig. 2(b), if the metal contacts are grounded, and the metal/semiconductor work function difference is $U_0 = \phi_{\rm CNT} - \phi_M$, where $\phi_{\rm CNT}(\phi_M)$ is the nanotube (metal) work function, the electron density is

$$n(z) = \bar{D}(U_0 - U(z)) \tag{3}$$

where $U(z)$ is the electron potential energy produced by charge in the channel, and $\bar{D}$ is the average density-of-states for the

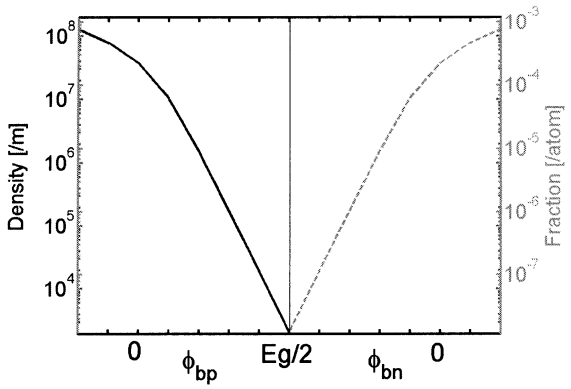

Fig. 3. Electron density (the dashed line) and hole density (the solid line) at the center of the 3-μm-long CNT [in Fig. 2(b)] versus the Schottky barrier height for electrons, $\phi_{\rm bn}$, and that for holes, $\phi_{\rm bp}$. The left axis shows the charge density in the unit of number of electrons (holes) per unit length and the right axis shows the same quantity in the unit of charge fraction.

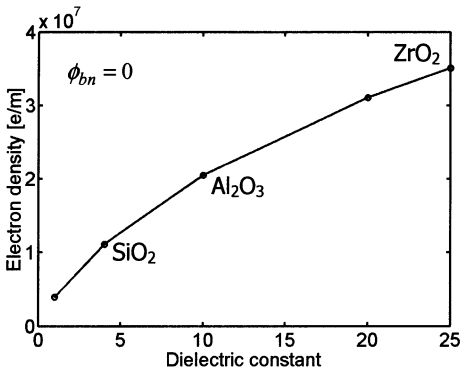

Fig. 4. Electron density at the center of the 3-μm-long tube [in Fig. 2(b)] versus the insulator dielectric constant. The Schottky barrier height for electrons, $\phi_{\rm bn}$, is zero.

energy between the nanotube middle gap energy and the Fermi level. The charge element in the 1-D channel only shifts the potential locally, we approximately relate the potential $U(x)$ to the electron density at the same position $n(z)$ as follows:

$$U(x) = e^2 n(z)/C_{\rm ins} \tag{4}$$

where $C_{\rm ins}$ is the electrostatic capacitance per unit length between the nanotube and the bulk contacts. The electron density due to the charge transfer from the bulk contacts can be obtained from (3) and (4) as

$$n(x) = \frac{U_0/e^2}{1/C_{\rm ins} + 1/\bar{C}_Q} \tag{5}$$

where the quantum capacitance [10], [11] is defined as $\bar{C}_Q = e^2\bar{D}$, which is proportional to the average DOS of the nanotube. Equation (5) can be interpreted in a simple way. The bulk electrodes modulate the charge density of the nanotube through an insulator capacitor, $C_{\rm ins}$, which is in series with the quantum capacitance of the nanotube.

We now examine how the charge transfer varies with the Schottky barrier height and the insulator dielectric constant. Fig. 3, which plots the charge density at the center of the tube as shown in Fig. 2(b) versus the barrier height, shows that when the barrier height decreases, the charge density first increases. Fig. 4, which plots the charge density at the center of the tube versus the insulator dielectric constant, shows that the charge density increases as the dielectric constant increases. The dependence of the charge density on the barrier height and the dielectric constant can be easily understood based on (5). Lowering the barrier height increases the metal/CNT work function difference, U_0, and increasing the insulator dielectric constant increases $C_{\rm ins}$, both of which increase the electron density, $n(x)$ (or hole density if the metal/semiconductor barrier height is lower for holes).

The importance of charge transfer into the carbon nanotube channel by one- dimensional metal contacts has been previously discussed in [4]. We, however, reached the same conclusion that charge transfer into the 1-D channel is significant for a different contact geometry (the bulk contacts). We also explored the 1-D contacts. In this case, the results are quite different from bulk contacts. The charge density of the nanotube channel is critically determined by the electrostatic environment (i.e., the potential and location of nearby bulk contacts) rather than the metal-contact properties, as will be discussed in detail next.

Fig. 5 illustrates the important role of the contact geometry. We simulated: 1) a CNT between grounded bulk contacts as shown in Fig. 5(a) and 2) a CNT between grounded wire contacts as shown in Fig. 5(b). In both cases, the tube length is 3 μm and a grounded, coaxial gate cylinder is far away with a radius of 30 μm. The S/D contacts have zero Schottky barrier heights for electrons thus tend to dope the tube n-type, while the gate has a high work function and zero barrier height for holes thus tends to modulate the tube to p-type. For the bulk contact case, the whole tube is doped to n-type by bulk contacts and the charge density on the tube is independent of the voltage on the gate cylinder. In contrast, for the wire contacts, the tube is lightly modulated to p-type and the charge density on the tube is very sensitive to the potential on the gate, although it is far away. The results shown in Fig. 5 can be explained as follows. For the bulk contacts, because the gate cylinder is far away, the bulk contacts at the ends collect all field lines and image all charge on the tube, as shown in Fig. 5(a). For the wire contacts, however, the potential produced by the charge on the 1-D wire decays rapidly with distance, thus several nanometer away from the metal/semiconductor interface, the wire contacts have little effects. On the other hand, the capacitance between the gate cylinder and the tube decays slowly (logarithmically) with the tube radius, thus several nanometer away from the metal/semiconductor interface, the charge on the tube images on the gate rather than the wire contacts nearby. As a result, the charge density is determined by the potential on the gate. The charge density on the nanotube channel is essentially determined by the electrostatic environment.

One consequence of the significant charge transfer is that nanowire transistors with large gate underlap can still operate. Fig. 6(a) shows a coaxially gated CNTFET with a 500-nm gate underlap and the bulk electrodes. Fig. 6(b) plots the conduction band profile at $V_G = 0$ and 0.3 V. In the OFF-state ($V_G = 0$ V), a large barrier is created in the channel and the transistor is turned off. In the ON-state ($V_G = 0.3$ V), the barrier under the gate is pushed down. Because the low dimensional charge

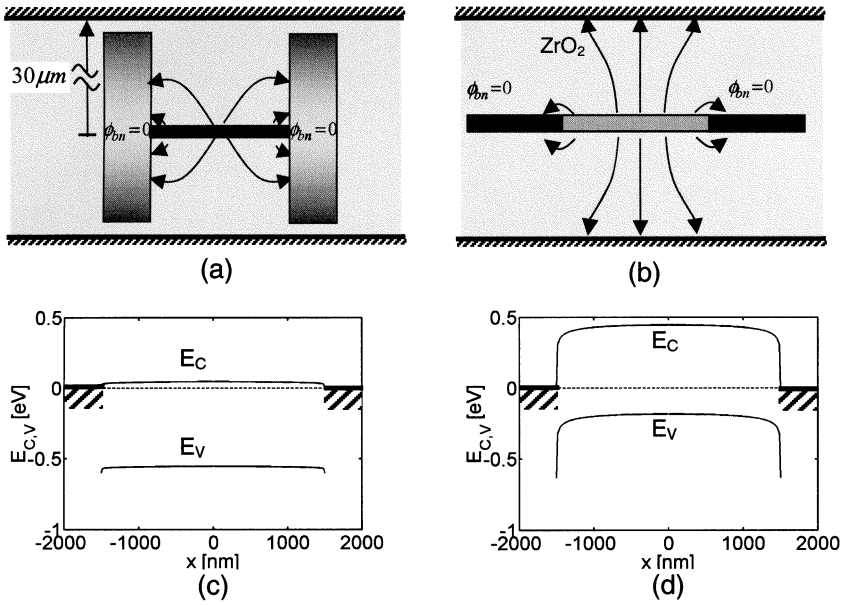

Fig. 5. Contact geometry. A 3-μm-long CNT between (a) the bulk contacts and (b) the 1-D wire contacts. The tube diameter is 1.4 nm. and Schottky barrier heights for electrons are zero. A coaxial gate far away with a 30-μm radius is grounded. The workfunction of the gate metal equals to the semiconductor affinity plus the band gap, so that the gate tends to dope the CNT to p-type. (c) The band profile for (a). (d) The band profile for (b).

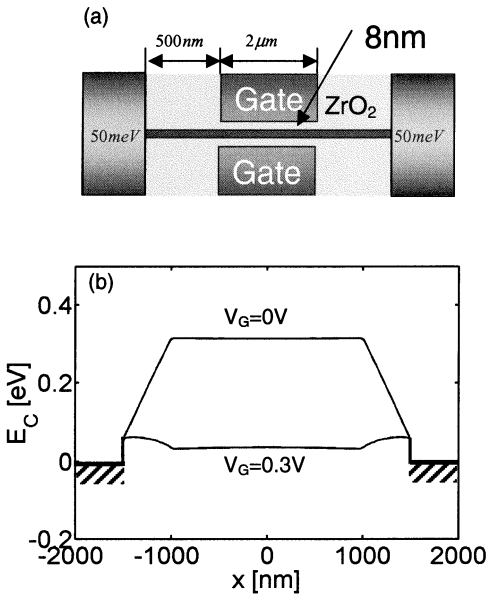

Fig. 6. (a) Coaxially gated CNTFET with bulk electrodes and a large gate underlap. (b) The conduction band profile at $V_G = 0$ V and 0.3 V. The metal/CNT barrier height for electrons is 50 meV, the ZrO_2 gate oxide thickness is 8 nm, the tube diameter is 1.4 nm, the gate length is 2 μm, and the gate underlap is 500 nm.

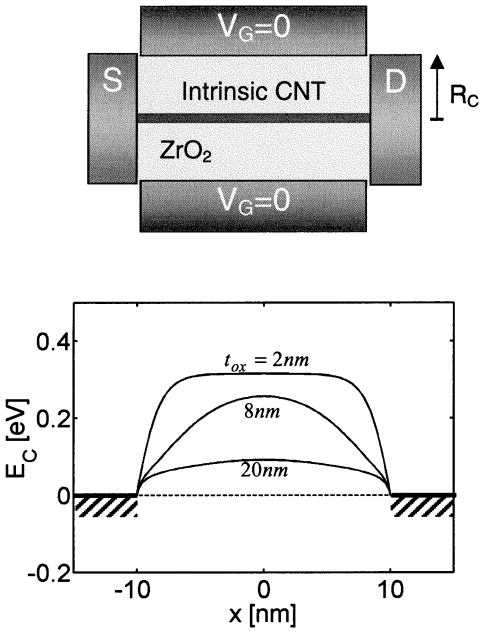

Fig. 7. (a) A coaxially gated CNTFET with a 20-nm-long, intrinsic channel. The source/drain radius, R_C, is equal to the oxide thickness. The metal/CNT barrier height for electrons is zero, the tube diameter is 1.4 nm and the dielectric constant of the gate insulator is $\varepsilon = 25$ (b) the equilibrium conduction band edge at $V_G = 0$ for the gate oxide thickness $t_{\rm ox}$ =2, 8, and 20 nm.

on the ungated nanotube does not effectively screen the potential produced by the gate and S/D electrodes, the potential at the ungated region is close to the Laplace potential produced by the source and gate electrodes. The conduction band edge is approximately linear in the ungated region. If the Schottky barrier height between S/D and the channel is $\sim$50 meV, the barrier height at the ungated region at the ON-state is low enough to deliver an ON-current of $\sim$1 μA. This mechanism provides a possible explanation for the operation of the n-type CNTFET in a recent experiment by Javey *et al.* [12], in which an n-type CNTFET with large, intrinsic gate underlaps still had a good ON–OFF ratio.

One concern about the nanowire transistors with low meta/CNT Schottky barriers is that due to the significant charge transfer, it might be difficult to turn off the transistor. To examine this concern, we simulated the coaxially gated CNTFET as shown in Fig. 7(a) with different gate oxide thickness. Fig. 7(b), which plots the equilibrium band profile, shows that when the gate oxide thickness is the same as the channel length, the source/drain field penetrates into the channel the channel and the transistor cannot be turned off. When the gate oxide is thin, however, the gate still has very good control over the channel and the transistor is well turned off. By solving

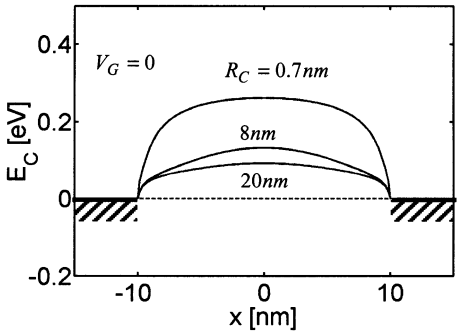

Fig. 8. Equilibrium conduction band edge at $V_G = 0$ for the CNTFET as shown in Fig. 7(a). The gate oxide thickness is kept constant at 20 nm and the source/drain contact radius is R_C =0.7, 8, and 20 nm.

the Poisson equation for the CNTFET in Fig. 7(a) [13], [14], the length by which the drain field penetrates into the channel (the scaling length [15]) is estimated to be the radius of the cylindrical gate, $\Lambda \sim R_G$. If the ratio between the channel length and the gate oxide thickness is large, the transistor can be well turned off.

Another way to reduce the penetration of the lateral field is to reduce the size of the source/drain contact. Fig. 8, which plots the equilibrium band profile for the CNTFET (in Fig. 7(a)) with 20-nm-thick gate oxide and different contact radius, shows that the screening length for lateral fields from S/D contacts decreases when the contact radius decreases. In the limit when the source/drain electrodes are reduced to wires with the same radius as the tube, the transistor can be well turned off, although the oxide thickness is large. As discussed earlier, the reason it that the potential produced by wire contacts decays rapidly with distance. Improving transistor performance by engineering contacts has been discussed by Heinze *et al.*, when they study the Schottky barrier CNTFETs. Smaller contacts produce thinner Schottky barriers and improve the transistor performance [2].

IV. Conclusion

The electrostatics of nanowire transistors were explored by self-consistently solving the Poisson equation with the equilibrium carrier statistics. For an intrinsic nanowire attached to bulk contacts, charge transfer is significant if the metal/semiconductor barrier height is low and the insulator dielectric constant is high. The contact geometry also plays an important role. If the contacts are metal wires rather than bulk contacts, the charge density of the nanowire channel is essentially determined by the electrostatic environment rather than the contact properties. The penetration distance of the source/drain field can be engineered by the gate oxide thickness and the contact size, which may provide ways to suppress the electrostatic short-channel effects.

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References

[1] A. Javey, J. Guo, Q. Wang, M. Lundstrom, and H. Dai, "Ballistic carbon nanotube field-effect transistors," *Nature*, vol. 424, pp. 654–657, 2003.
[2] S. Heinze, J. Tersoff, R. Martel, V. Derycke, J. Appenzeller, and Ph. Avouris, "Carbon nanotubes as schottky barrier transistors," *Phys. Rev. Lett.*, vol. 89, no. 10, p. 106 801, 2002.
[3] Y. Cui, Z. Zhong, D. Wang, W. Wang, and M. Lieber, "High performance silicon nanowire field effect transistors," *Nano Lett.*, vol. 3, pp. 149–152, 2003.
[4] F. Leonard and J. Tersoff, "Novel length scales in nanotube devices," *Phys. Rev. Lett.*, vol. 83, pp. 5174–5177, 1999.
[5] A. Odintsov, "Schottky barriers in carbon nanotube heterojunctions," *Phys. Rev. Lett*, vol. 85, pp. 150–153, 2000.
[6] F. Leonard and J. Tersoff, "Role of fermi-level pinning in nanotube schottky diodes," *Phys. Rev. Lett.*, vol. 84, pp. 4693–4696, 2000.
[7] J. W. Mintmire and C. T. White, "Universal density of states for carbon nanotubes," *Phys. Rev. Lett.*, vol. 81, pp. 2506–2509, 1998.
[8] S. Ramo, J. R. Whinnery, and T. V. Duzer, *Field and Waves in Communication Electronics*. New York: Wiley, 1994.
[9] Z. Ren, "Nanoscale MOSFET: Physics simulation and design," Ph.D. dissertation, Purdue University, West Lafayette, IN, 2001.
[10] S. Luryi, "Quantum capacitance devices," *Appl. Phys. Lett.*, vol. 52, pp. 501–503, 1988.
[11] J. Guo *et al.*, "Assessment of silicon MOS and carbon nanotube FET performance limitsusing a general theory of ballistic transistors," in *IEDM Tech. Dig.*, 2002, pp. 711–714.
[12] A. Javey *et al.*, "High dielectrics for advanced carbon nanotube transistors and logic," *Nature Materials*, vol. 1, pp. 241–246, 2002.
[13] J. D. Jackson, *Classical Electrodynamics*. New York: Wiley, 1975.
[14] D. John, L. Castro, J. Clifford, and D. Pulfrey, "Electrostatics of coaxial schottky-barrier nanotube field-effect transistors," *IEEE Trans. Nanotechnol.*, vol. 2, pp. 175–180, 2003.
[15] D. Frank, Y. Taur, and H.-S. P. Wong, "Generalized scaling length for two-dimensional effects in MOSFETs," *IEEE Electron Device Lett.*, vol. 10, pp. 385–387, 1998.

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