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Electro-thermal Design of a Discrete GaN Based Converter for Integrated Modular Motor Drives

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***Abstract*—Integrated modular motor drives have a compact and high fault tolerant structure compared to their conventional counterparts. The most challenging issue in the implementation of these drives is the thermal management of the inverter modules due to the small space available for each module and its physical proximity to the machine windings with their high heat production. The electro-thermal design of a discrete half-bridge inverter module for a radially stator mounted axial flux integrated drive is introduced in this paper. The inverter modules are mounted on the stator, radially along the circumference. The converter is implemented using GaN technology and the size is optimized. The structure of the presented integration topology from the case of the switches to the cooling ambient is optimized from the thermal point of view. The converter is modelled using steady state and transient lumped parameter thermal networks to estimate the steady state and the instantaneous temperature of the switches. The converter parasitics are extracted using FEM simulations and their influence on the switch loss and temperature is evaluated. The lumped parameter modelling is validated with CFD simulations and experimental measurements.**

***Index Terms*—Integrated modular drives, Wide Bandgap converters, Parasitic inductance, Inverter thermal modelling, Converter parasitic extraction, CFD modelling.**

I. Introduction

Integrated modular motor drives (IMMDs) combine the benefits of the physical integration of the machine and its driving structure and the drive modularity [1]- [2]-[3]. The physical integration eliminates the connection cables between the driving inverter and the machine which reduces the electromagnetic interference (EMI) of the drive [4]. A single cooling loop and housing structure can be employed for both the machine and the converter eliminating the separate cooling and housing of the converter [5]. The elimination of such components reduces the weight, the volume and the cost of the drive [6]. The modularity of the converter enhances the fault tolerance of the drive and reduces the voltage and the thermal stresses on the inverter switches [2]-[7]. One more advantage of the modularity is the possibility to interleave the carrier waveforms of the different modules to reduce the current stress of the DC-link capacitors [8].

The most challenging aspect to meet in the design of the IMMDs is the thermal management of the inverter modules due to their close proximity to the heat sources in the machine and the small space available for each inverter module [9]-[10]. These challenges can be met by utilizing wideband gap devices (GaN, SiC) in the implementation of the inverter modules [11]-[12] thanks to their small package size for the same voltage and current rating and low losses [13].

IMMDs can be classified to axially stator iron mounted (ASM), radially stator iron mounted (RSM), axially housing mounted (AHM) and radially housing mounted (RHM) [6]. In the ASM and RSM, the inverter modules are mounted near to the back iron of the stator while in the AHM and RHM, the inverter modules are mounted in an extended part of the machine housing in the axial or the radial direction. The RSM and ASM provide a more compact integrated drive with higher cooling design challenges.

In [14], a modular ring shaped converter is designed with the focus on the influence of the DC-link connections on the DC-link parasitics and the electrical stresses on the switches. In [2], a converter is designed for integrated drives with focus on the influence of the module connections on the voltage stress of the inverter and interleaving on the current stress of the DC-link capacitors. In [15], the influence of the design parameters (i.e. switching frequency, modulation index, number of modules, aspect ratio) on the system efficiency and power density is studied. In [16], a six-phase modular inverter is designed for axial integration in electric vehicle drives as a separate subsystem with focus on minimization of the DC-link capacitors height. In [17], a high power density axially stator mounted modular integrated drive based on modular twelve half-bridge inverter is developed for Unmanned Aerial Vehicles.

In this paper, a discrete low form factor GaN based half-bridge inverter module is designed for a RSM integrated drive developed by the authors. The integration structure and the inverter module are optimized from the thermal point of view. The steady-state and transient thermal models of the inverter module are derived and validated by CFD models and experimental measurements. The parasitics of the inverter module are extracted using a FEM model for the inverter PCB and their influence on the power loss and the temperature of the switches is evaluated.

The paper is arranged as follows: section II provides a brief description of the RSM integrated drive for which the GaN inverter module is designed with an optimal size and thermal performance. Section III elaborates the design of the inverter module electrically and thermally. In section IV, the optimization of the thermal performance of the inverter module and the integrated structure is explained. In section V, the VA rating of the inverter module is evaluated based on

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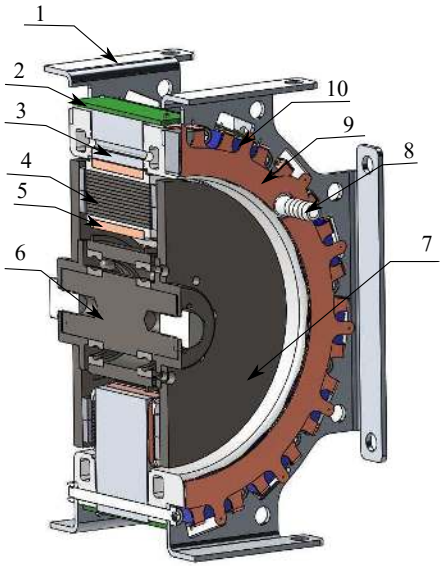


Fig. 1. A RSM integrated drive: (1) Mounting structure, (2) Converter module PCB, (3) Cooling channel, (4) Core, (5) Winding, (6) Shaft, (7) Rotor disc, (8) Cooling fluid fitting, (9) DC-link busbar, (10) DC-link capacitor

the maximum current that can be injected without violating the thermal limits. In section VI, the transient model of the converter is derived to evaluate the peak temperature of the switch to ensure reliable operation. Section VII explains the FEM model of the inverter PCB to extract the parasitics and explains the influence of them on the power loss and the temperature of the switch. In section VIII, the experimental setup and results are provided. Section IX gives the conclusion of the design and the results obtained in the paper.

II. Structure of the RSM integrated drive

Fig. 1 shows the construction of a fully integrated axial flux drive. The drive integrates the machine, the power converter modules and the DC-link structure together. The topology is capable of mechanically and thermally integrating the machine and the inverter modules without increasing the outer radius of the mechanical structure and cooling structure of the non-integrated machine. Adding the power electronic modules increase the outer diameter of the integrated machine by 7.25 mm which is the height of the gate drive power supplies, compared to the non-integrated machine. The key specifications of the drive are listed in Table I.

Fig. 2 illustrates how the inverter modules are integrated mechanically and thermally with the machine. The circular cross section of the ordinary housing shown in Fig. 2 (a) of the non-integrated machine has been replaced by its circumscribing polygon shown in Fig. 2 (b). In this way, a flat surface is created for mounting the inverter modules (mechanical integration).

The thermal management concept is illustrated by the cooling diagram in Fig. 3. The heat generated by the inverter switches and the machine stator components is decoupled by a cooling channel and dissipated in the cooling fluid pumped in the channel.

TABLE I
The key specifications of the integrated drive

Quantity	Value
Rated power (kW)	17
Rated speed (rpm)	2500
Rated rms current (A)	10
# pole pairs	8
# Slots	15
Axial stack length L_a (mm)	60
Outer diameter in Fig. 2 (a) D_o (mm)	190

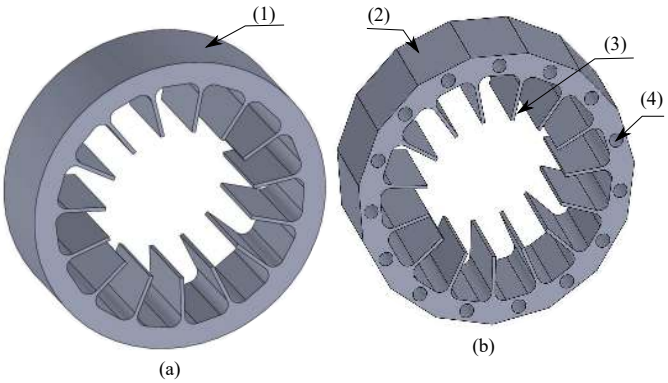


Fig. 2. Mechanical and thermal integration concept: (a) housing of the non-integrated machine, (b) integrated shared cooling structure, (1) cylindrical housing, (2) converter mounting surface, (3) radially inward stator heat extraction fins, (4) cooling channel

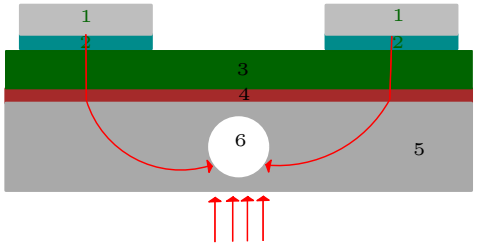


Fig. 3. The shared cooling concept with the arrows indicating the heat dissipation path: (1) the switch junction, (2) the thermal pad, (3) the PCB, (4) the thermal interface material, (5) the shared cooling structure, (6) the cooling channel

The outer diameter of the non-integrated machine is kept the same by designing and integrating the busbar structure shown in Fig. 4. The DC-link capacitors are arranged circumferentially with each capacitor pointing radially inward.

III. Inverter module design

The main challenge of the inverter module design for the integrated drive in Fig. 1 is the strictly defined module dimensions. The full half-bridge inverter module should be implemented within these dimensions and the thermal resistance from the switches to the ambient should be minimized for maximization of power output per module.

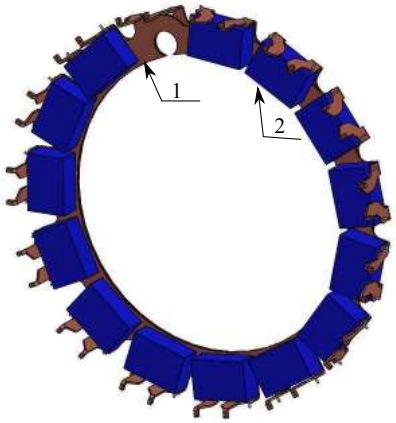


Fig. 4. The DC-link structure: (1) The busbar structure, (2) The DC-link capacitors

TABLE II
Key specifications of candidate inverter switches

Device	STW38N65M5	GS66508B	SCT3080ALHR
technology	Si	GaN	SiC
rated voltage (V)	650	650	650
rated current (A)	30	30	30
drain to source resistance R_{ds} (mΩ)	95	50	80
gate charge Q_g (nC)	71	5.8	48
reverse recovery charge Q_{rr} (nC)	6.6	0	53
reverse recovery time (t_{rr})	382	0	15
Figure of merit (FOM)	6745	290	3840
package size (mm^2)	306.7	60.4	327.6
case size	275.6	28.66	275.6

A. Inverter module dimensions

Each inverter module has one dimension in the axial direction of the machine and the other one in the circumferential direction. The dimension in the axial direction is the same as the axial length of the machine (L_a). The dimension in the circumferential direction (L_c) depends on the number of modules (n) and the outer diameter of the machine D_o. L_c can be calculated from (1). For the case study in Fig. 1, the resulted module dimensions are 60×40 mm^2.

$$L_c = D_o \tan(\frac{180}{n}) \tag{1}$$

B. Selection of inverter switches

Three candidate switches with the same voltage and current rating suitable for the application are compared for selection of the inverter module switches. Each switch belongs to a different power semiconductor technology in the market (Si, GaN, SiC). Table II contains the key specifications of the three switches.

Given the small space available for the inverter module, the two selection criteria for the inverter switches are the package size and the switch losses. From Table II, the GaN switch has the smallest package size.

The figure of merit (2) gives an indication for the total losses in the forward conduction path of the switch. The smaller the FOM, the smaller the losses.

$$FOM = R_{ds} * Q_g \tag{2}$$

The smaller the reverse recovery charge (Q_{rr}), the smaller the switching losses in the reverse conduction path of the switch. From Table II, the GaN switch achieves the lowest losses among the three technologies. Thus, the GaN switch GS66508B is selected for the converter implementation.

C. Switch cooling requirement

The cooling requirement of the switch can be represented by the maximum thermal resistance from the junction of the switch to the ambient which is the cooling fluid. The maximum thermal resistance from the junction of the switch to the ambient can be estimated from the switch total loss versus the junction temperature rise.

Both the conduction and the switching losses in the switch depend on the junction temperature due to the variation of the drain to source resistance, the voltage drop from the source to the drain and the output characteristic of the switch with the temperature. If the converter parasitics are neglected, the temperature dependant forward and reverse conduction paths losses in the switch can be calculated from (3)-(9). (3)-(9) are derived starting from the analytical loss equations given in [18] and [19] for the switches and the diodes.

$$P_{cons} = I_{srms}^2 R_{ds}(T) \tag{3}$$

$$P_{son} = V_{dc} f_o \sum_{n=1}^{n_{son}} (t_{on}(n,T) i_{on}(n) + Q_{rr}(n)) \tag{4}$$

$$P_{soff} = V_{dc} f_o \sum_{n=1}^{n_{soff}} (t_{off}(n,T) i_{off}(n)) \tag{5}$$

$$P_{st} = P_{cons} + P_{son} + P_{soff} \tag{6}$$

$$P_{cond} = f_o \int_t^{t+T_o} i_d(t) v_d(t,T) dt \tag{7}$$

$$P_{sd} = 0.25 V_{dc} f_o \sum_{n=1}^{n_{doff}} Q_{rr}(n) \tag{8}$$

$$P_{dt} = P_{cond} + P_{sd} \tag{9}$$

where, P_{cons},P_{son},P_{soff},P_{st} are the switch conduction, turn on, turn off and total losses respectively, V_{dc} is the DC link voltage, f_o is the fundamental frequency of the switch current waveform, n_{son} and n_{soff} are the number of turn-on and turn-off transitions of the switch in one fundamental cycle respectively, $t_{on}(n,T)$ and $t_{off}(n,T)$ are the turn-on and the turn-off time of the switch at the transition number n and temperature T, $i_{on}(n)$ and $i_{off}(n)$ are the switch current at the turn on and off instants respectively, $Q_{rr}(n)$ is the reverse recovery charge of the diode, $T_o = \frac{1}{f_o}$, $i_d(t)$ and $v_d(t,T)$ are the instantaneous current and voltage drop of the diode at temperature T, P_{cond}, P_{sd}, P_{dt} are the diode conduction, switching and total losses respectively.

Fig. 5 shows the variation of the switch power loss with the junction temperature rise at two switching frequencies (f_s)

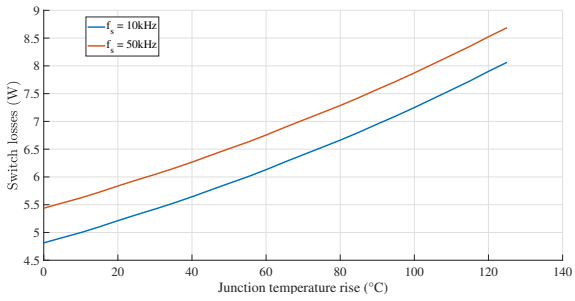


Fig. 5. Variation of switch losses with junction temperature for 10kHz and 50kHz switching frequencies

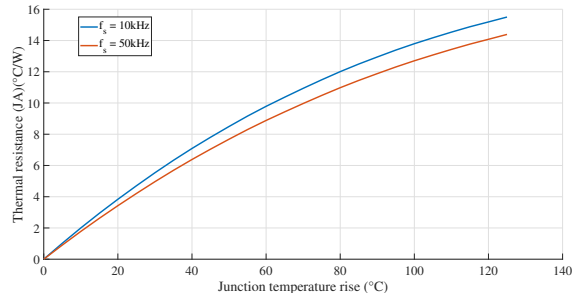


Fig. 6. Maximum junction to ambient thermal resistance versus the maximum allowable junction temperature rise for 10kHz and 50kHz switching frequencies

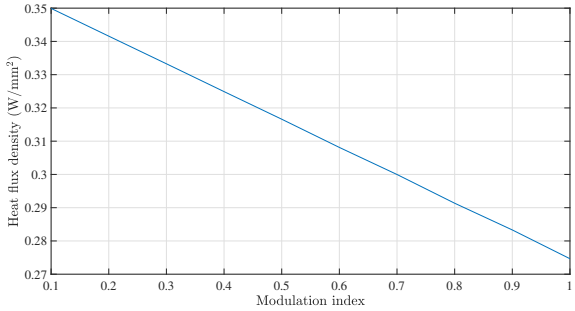


Fig. 7. Influence of the modulation index on the switch loss density

TABLE III
Key specifications of the (FB27A6J0335C) capacitor

Variable	Value
rated voltage (V)	550
rated rms ripple current (A)	5
capacitance (μF)	3.3
ESR (mΩ)	22
$\tan(\delta)$	2e-4
thermal resistance R_{th} (°C/W)	27.3
rated hotspot temperature (°C)	100
ESL (nH)	25

10kHz and 50kHz. The figures are generated considering the rated conditions of the drive in Table I assuming an ambient temperature of 25°C.

Depending on the maximum allowable junction temperature rise, the thermal resistance from the junction of the switch to the ambient can be obtained from the reciprocal of the slope of the curves in Fig. 5. Fig. 6 provides the maximum limit of the thermal resistance from junction to ambient for a given junction temperature rise limit for 10kHz and 50kHz switching frequencies.

As the targeted application is variable speed drive, the modulation index (M) is expected to be variable. The influence of M on the switch loss density is evaluated and reported in Fig. 7. it can be seen that the switch power loss decreases with M. This can be explained by the significance of the losses in the reverse conduction path compared to the forward one due to the high voltage drop on the reverse path compared to the forward path. As the modulation index increases, the forward conduction duration exceeds the reverse one which means lower reverse losses and hence total losses reduction with the modulation index.

D. DC-link capacitor selection

The two main capacitor selection criteria for the integrated drives are the DC-link voltage ripple and the rated hot spot temperature of the capacitor. The capacitor is selected to limit the DC-link voltage ripple to 1% of the DC-link voltage. Since, the ambient temperature of the integrated drives is expected to be high, the loss of the DC-link capacitor should be kept low to keep the hot spot of the capacitor within the rated value.

The analytical design approach developed in [20] is adopted. The value of the needed capacitance for the three phase operation of the drive is calculated to be 2μF and 1.92A capacitor rms current. Due to the longer life time, higher rated rms ripple current, smaller equivalent series resistance and lower losses compared to electrolytic capacitors [21] the film capacitor technology is chosen. The commercial film capacitor (FB27A6J0335C) with the specifications in Table III is chosen.

E. Inverter module PCB design

The design of the inverter PCB influences the thermal and the electromagnetic behaviour of the converter [22]. The PCB is designed as four layer board with the layer stack design shown in Fig. 8. The copper layers serve as a heat spreader for better heat transfer [23] and they are also used in effective magnetic field cancellation routing to reduce the parasitics of the converter.

Two main loops should be carefully routed for proper operation of the inverter module: the power commutation loop and the gate drive loop [24]. The area of both loops should be minimized for reduction of the commutation loop inductance and the gate loop inductance. Ceramic decoupling capacitors of 0.01 μF each are used in parallel with the main DC-link capacitors and routed in top and bottom layers as shown in Fig. 9.

Thanks to the small equivalent series inductance (ESL) of the decoupling capacitors compared to the main capacitor, the

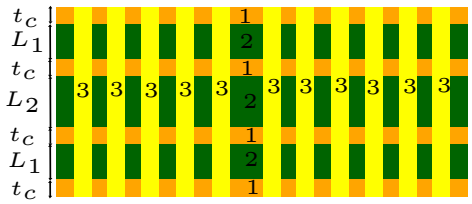


Fig. 8. The layer stack design of the inverter module PCB: (1) copper layers, (2) PCB laminate, (3) thermal vias. L_1= 0.36mm, L_2= 0.71mm, t_c= 0.07mm

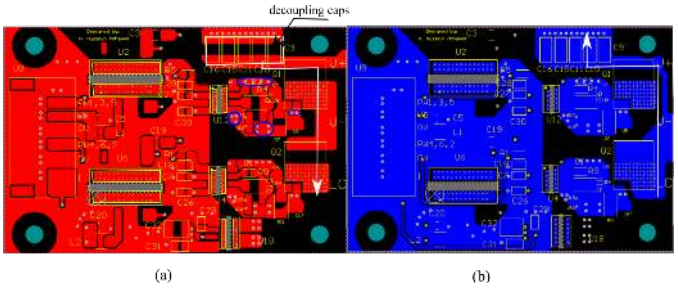


Fig. 9. PCB copper plot on the top layer (a) and the bottom layer (b)

current flows through them rather than the main capacitor during the commutation period. The commutation loop is routed so that, the current during the commutation period flows as indicated by the white arrows in Fig. 9. In this way, the current flows from the decoupling capacitors through the upper and the lower switches on the top layer and then returns back as a mirror on the bottom layer to cancel the magnetic field and hence reduce the parasitic inductance.

The isolated gate drive IC SI8271GB-IS with the main specifications in Table IV from SILICON LABS is used for driving the switches. It has a small propagation delay, an under voltage lockdown (UVLO) of 3V suitable for the driving voltage (V_{gon}) of the switch of 6V and a suitable source/sink current of 4A. The external turn on gate resistance (R_{gon}) and turn off resistance (R_{goff}) should be selected to satisfy the inequalities in (10) and (11), other wise the turn on/off speed of the switch will be limited by the current limit of the driving IC. Any value greater than or equal to zero for R_{gon} and R_{goff} would satisfy the inequalities.

$$R_{gon} \geq \frac{V_{gon}}{I_{on}} - (R_{gint} + R_{pu}) \tag{10}$$

$$R_{goff} \geq \frac{V_{gon}}{I_{off}} - (R_{gint} + R_{pd}) \tag{11}$$

where, I_{on}, I_{off} and R_{gint} are the sink current, the source current of the driving IC and the internal gate resistance of the switch.

One more inequality that should be satisfied by the selected gate resistances (R_{gon}) and (R_{goff}) is given in (12). The satisfaction of this inequality makes sure that the switches don't turn on spuriously by the miller current during the commutation of the switches.

TABLE IV
Gate drive IC main specifications

property	value
source/sink current (A)	4
$\frac{dv}{dt}$ immunity	200 kV/μs
maximum propagation delay (ns)	60
under voltage lockdown (UVLO) (V)	3
pull up resistance (R_{pu}) (Ω)	2.7
pull down resistance (R_{pd}) (Ω)	1
rated junction temperature ($^\circ C$)	125
junction to ambient thermal resistance ($^\circ C$/W)	115

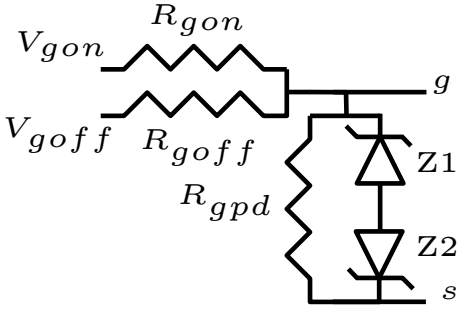


Fig. 10. Gate protection circuit

$$(\frac{V_{gon} - V_{plat}}{R_{gon} + R_{gint} + R_{pu}}) \times (R_{goff} + R_{gint} + R_{pd}) < V_{th} \tag{12}$$

where, V_{plat} is the plateau voltage of the switch, V_{th} is the threshold voltage of the switch.

The values selected for the R_{gon} and R_{goff} are 10 Ω and 1 Ω respectively.

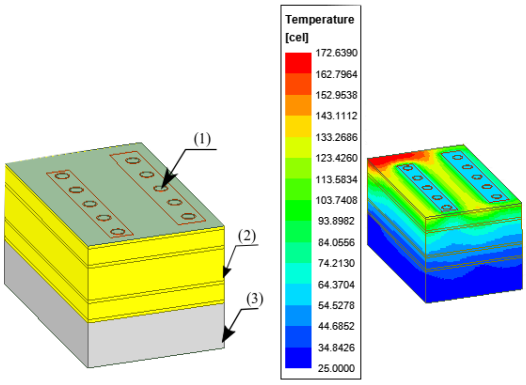
For extra protection of the switch against spurious turn on, a pull down resistor (R_{gpd}) of 10 kΩ and two back to back zener diodes (BZT52C6V8S-7-F) of 6.8V zener voltage are connected between the gate and the source of the switch as shown in Fig. 10. The pull down resistor shunts the miller current and makes sure that the switch voltage doesn't reach the threshold voltage during turn off period. The zener diodes clamp the gate voltage to its rated value.

The gate drive components are closed as close as possible to the gate of the switch and the same routing method used with the power commutation loop is used. The gate current leaves the gate drive IC to the gate of the switch on the top layer and mirrors back on the below layers in order to minimize the loop area and the gate parasitic inductance. The parasitics of the power loop and the gate loop are calculated in section VII and their influence on the thermal and the electrical performance of the converter is evaluated.

To make sure that the temperature of the driving IC stays below the rated value, the power loss of the IC P_{Dic} is calculated [25] (16). The IC power loss consists of three terms: the bias loss P_{D1}, the parasitic switching loss P_{D2} and the input/output resistance loss P_{D3}. P_{Dic} is calculated at the operating conditions in Table V and the value is 100.57 mW. A

TABLE V
Gate drive loss calculation parameters

parameter	value
V_{DDI} (V)	5
I_{DDI} (mA)	10
V_{DDx} (V)	6
I_{DDx} (mA)	4
Q_g (nC)	5.8
f_s (kHz)	50



(a) (b)

Fig. 11. Driving IC thermal model (a) geometry: (1) thermal vias, (2) PCB, (3) TIM, (b) temperature distribution at 1W loss top surface and 25°C bottom temperature

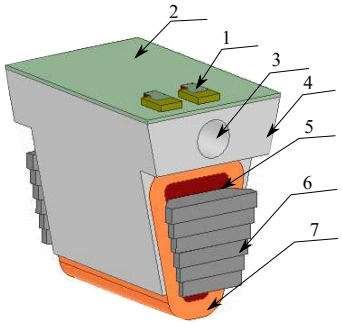
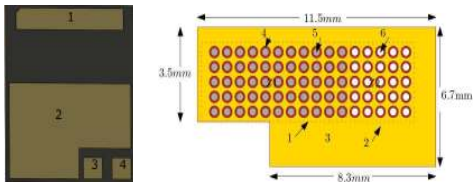


Fig. 12. One integrated module geometry: (1) the module PCB, (2) the thermal interface material (TIM), (3) the cooling channel, (4) the shared cooling structure, (5) the impregnation epoxy resin, (6) the core laminations, (7) the windings



(a) (b)

Fig. 13. Selected switch package and thermal vias pattern (a) switch package: (1) drain, (2) case (source), (3) gate, (4) source sense (b) thermal vias pattern: (1) inner thermal vias beneath the switch, (2) outer zone vias, (3) copper plot, (4) via plating copper, (5) via filling solder, (6) air

thermal model from the case of the IC to the cooling ambient Fig.11 (a) is developed to evaluate the thermal performance of the IC. A 1W loss is imposed on the top surface and constant 25°C on the bottom surface and all other surfaces are adiabatic. The peak top surface temperature is 172.6 °C as shown in Fig. 11 (b) and the thermal resistance from the case of the IC to the ambient (R_{caic}) is 147°C/W. for proper thermal operation of the IC, the junction to case thermal resistance should be less than 847°C/W. Since, the junction to case thermal resistance is less than 115°C/W then, no thermal problem is expected.

$$P_{D1} = V_{DDI} I_{DDI} + 2 V_{DDx} I_{DDX} \quad (13)$$

$$P_{D2} = 2 f_s C_{int} V_{DDx}^2 \quad (14)$$

$$P_{D3} = f_s Q_g V_{DDx} [\frac{R_{pu}}{R_{pu} + R_{gon}} + \frac{R_{pd}}{R_{pd} + R_{goff}}] \quad (15)$$

$$P_{Dic} = P_{D1} + P_{D2} + P_{D3} \quad (16)$$

where, V_{DDI}, I_{DDI}, V_{DDx}, I_{DDx} are the input bias voltage, input bias current, the output voltage and the output bias current, Q_g is the gate charge.

IV. Thermal Design of Integrated Drive Module

Fig. 12 shows the detailed construction of one module of the integrated drive in Fig. 1. The cooling structure is capable of extracting heat from both the machine stator and the inverter switches. The heat flow path from the junction of the switch to the ambient includes the junction to case thermal resistance (R_{JC}), the case to the PCB bottom thermal resistance (R_{CP}), the PCB to ambient thermal resistance (R_{PA}). These thermal resistances should be minimized for optimal thermal performance. The R_{JC} is defined by the internal structure of the switch and can be extracted from the datasheet. The R_{JC} for the selected switch is 0.5°C/W.

A. Case to PCB thermal resistance

The case to PCB thermal resistance depends on the geometry of the switch case, the layer stack design, and the thermal vias pattern beneath the case. The selected GaN switch package and the thermal vias pattern populated beneath the switch case and beyond are shown in Fig. 13. The thermal vias reduce the thermal resistance from the switch case to the bottom layer of the PCB extensively.

Thermal vias have a heterogeneous structure. Each via consists of a via barrel plated with copper and filled with a solder. This barrel is drilled through the layer stack structure. So, each via is composed of the following materials: copper, PCB laminate (FR4) and the filling solder (SnAgCu). For faster thermal simulations and easier thermal resistance calculations, the PCB part with thermal vias in Fig. 13 (b) is homogenized using 3-D thermal FEM simulations.

Th homogenization process involves the calculation of an equivalent thermal conductivity in each direction (k_{xe}, k_{ye}, k_{ze}), an equivalent mass density (ρ_e) and specific

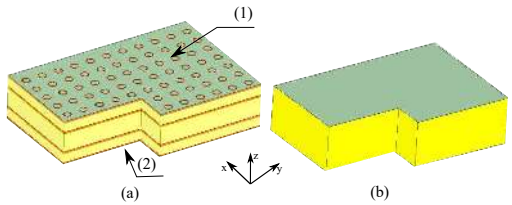


Fig. 14. PCB homogenization illustration (a) non-homogeneous PCB: (1) PCB top surface, (2) PCB bottom surface (b) homogenized PCB

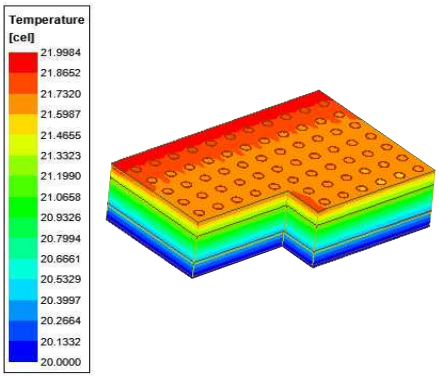


Fig. 15. PCB temperature distribution for 1W top surface loss, 20°C bottom surface temperature and all other surfaces are adiabatic

heat capacity (C_{pe}) for the PCB. Fig. 14 illustrates the homogenization method of the inner zone (see Fig. 13 (b)) for calculation of k_{ze}. A 1W loss (P_{loss}) is imposed on the top surface of the PCB and the temperature of the bottom surface (T_b) is kept constant at 20°C while all other surfaces are adiabatic. The thermal simulation is performed and the maximum temperature of the top surface is calculated (T_t). Fig. 15 shows the resulted temperature distribution with maximum temperature of 21.9984 °C for the top surface of the PCB. The thermal resistance and the equivalent thermal conductivity in the Z direction can be calculated from (17).

$$\begin{cases} R_z &= \frac{T_t - T_b}{P_{loss}} \\ k_{ze} &= \frac{L_z}{R_z A_z} \end{cases} \tag{17}$$

where, L_Z is the PCB thickness, A_z is the area of the top or the bottom surface.

The homogenization is done in a similar way for the x and y directions. The equivalent mass density (ρ_e) and specific heat capacity (C_{pe}) are calculated using the volumetric ratio of each material with respect to the total volume of the PCB part under homogenization. C_{pe} and ρ_e can be calculated from (18) and (19) respectively.

$$C_{pe} = C_{pcu}\frac{v_{cu}}{v_t} + C_{pfr4}\frac{v_{fr4}}{v_t} + C_{psolder}\frac{v_{solder}}{v_t} \tag{18}$$

$$\rho_e = \rho_{cu}\frac{v_{cu}}{v_t} + \rho_{fr4}\frac{v_{fr4}}{v_t} + \rho_{solder}\frac{v_{solder}}{v_t} \tag{19}$$

where, C_{pcu}, C_{pfr4}, $C_{psolder}$ and ρ_{cu}, ρ_{fr4}, ρ_{solder} are the specific heat capacities and mass densities of the copper, FR4 and the solder respectively. v_{cu}, v_{fr4}, v_{solder} are the volumes of the copper, FR4 and the solder respectively and v_t is the PCB part total volume.

TABLE VI
Thermal properties of PCB materials

Material	Thermal conductivity (W/m.K)	Specific heat capacity (J/kg.k)	Mass density (kg/m^3)
Copper	385	392	8890
FR4	0.35	1300	1250
Solder (SnAgCu)	57.3	250	7500
Air	0.0261	1005	1.1614

TABLE VII
Equivalent thermal properties of the homogenized PCB

Zone	Property	Value
inner	k_{xe} (W/m.K)	5.8767
	k_{ye} (W/m.K)	7.7
	k_{ze} (W/m.K)	25.3476
	C_{pe} (J/kg.K)	1017.7
	ρ_{pe} (kg/m^3)	3345
outer	k_{xe} (W/m.K)	5.4
	k_{ye} (W/m.K)	6.4
	k_{ze} (W/m.K)	1.3638
	C_{pe} (J/kg.K)	1127
	ρ_{pe} (kg/m^3)	2523.3

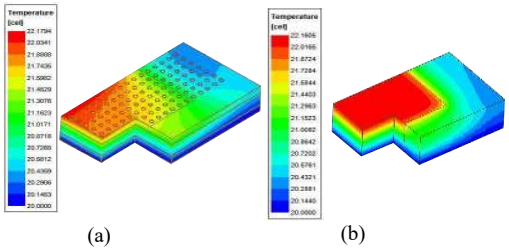


Fig. 16. PCB temperature distribution for 1W switch loss, 20°C bottom surface temperature, other surfaces are adiabatic (a) non-homogeneous model (b) homogenized model

The thermal properties of the materials used in the simulations are in Table VI. The equivalent thermal properties of the homogenized PCB are in Table VII.

Fig. 16 shows the PCB temperature distribution using the non-homogeneous and the homogenized models. The simulations are done using 1W loss over the inner zone top surface (the switch case) and 20°C constant temperature on the bottom surface. The non-homogeneous model takes 22 minutes to solve while the homogenized one takes only 2 minutes. Fig. 17 shows the error in temperature estimation due to homogenization versus the switch power loss. As the switch loss is not expected to be higher than 10W, the error in the temperature estimation using the fast homogenized model will not exceed 3.7%. From Fig. 16, the R_{CP} = 2.2°C/W.

B. PCB to ambient thermal resistance

From Fig. 3, the R_{PA} has three components, two conduction components through the thermal interface material (TIM) and the aluminium shared cooling structure and one convection

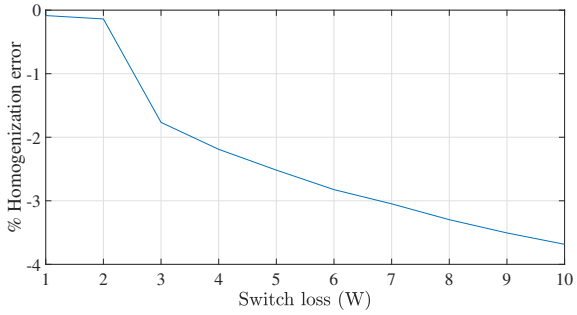


Fig. 17. PCB temperature estimation error due to homogenization

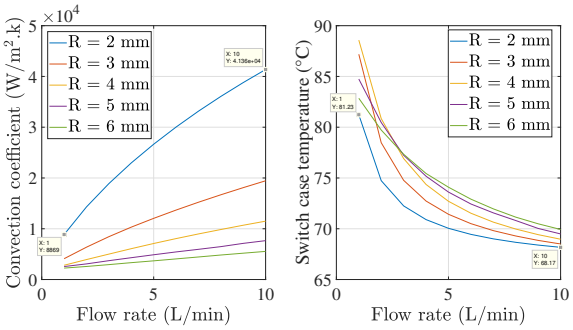


Fig. 18. Effect of the channel radius and flow rate on the convection coefficient (left) and the switch case temperature (right)

component through the cooling fluid. Although the calculation of the R_{PA} is sufficient for the steady state cooling performance analysis, the breakdown of this resistance into its components gives an insight into the heat transfer from the bottom of the PCB to the cooling fluid and makes it possible to model the transient temperature accurately.

The values of the three components of R_{PA} depend on the radius of the cooling channel and the flow rate. The bigger the radius, the bigger the channel area through which the heat transfer takes place which enhances the heat transfer but, at the same time, the coolant speed reduces for a given flow rate which in turn reduces the convection coefficient and hence the heat transfer rate. Therefore, the cooling channel radius should be optimized.

A CFD model is built for the integrated module in Fig. 12 to calculate the convection coefficient and the case temperature of the switches at different radii and flow rates. The simulation is performed considering a 5W loss in each switch and a 50W loss in the windings and the core. Fig. 18 shows the resulted channel convection coefficient and the switch case temperature for the radii from 2mm to 6mm and flow rates from 1 L/min to 10 L/min. The 2mm channel radius achieves the highest global convection coefficient and the lowest global switch case temperature. Therefore, the selected channel radius is 2mm. The switch case temperature decreases by 16% at the flow rate of 10 L/min compared to 1 L/min at 2mm channel radius.

For calculation of the R_{PA} and its three constituting components, the three curves in Fig. 19 are generated using CFD

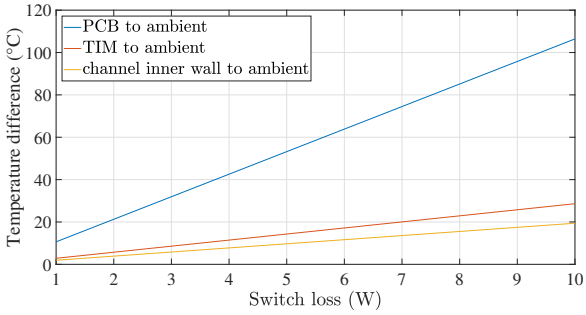


Fig. 19. The variation of the temperature difference from the PCB bottom surface to ambient, the TIM to ambient, the channel inner wall to ambient considering both switch and machine losses

TABLE VIII
PCB to ambient resistance and its components

Thermal resistance (°C/W)	Value
R_{PA}	10.6396
R_{TIM}	7.7783
R_{AL}	0.9226
R_{conv}	1.9387

simulations at 1 L/min flow rate, 22.5°C water inlet temperature and 2mm channel radius. The machine components loss set from 10W to 100W is considered with the switch loss set from 1W to 10W to account for the coupling resistance from the machine to the switches. The three curves represent the temperature difference between the PCB bottom surface and the ambient, the TIM bottom surface and the ambient, the inner wall of the cooling channel and the ambient at different switch losses. The slopes of these curves give the R_{PA}, the TIM to ambient thermal resistance R_{TA} and the convection resistance of the channel inner wall R_{conv}. The TIM thermal resistance R_{TIM} and the aluminium shared cooling structure resistance R_{AL} can be calculated from (20).

$$\begin{cases} R_{TIM} & = R_{PA} - R_{TA} \\ R_{AL} & = R_{TA} - R_{conv} \end{cases} \tag{20}$$

The value of R_{PA} and its components are given in Table VIII. The R_{TIM} constitutes 73.1% of R_{PA} due to its small thermal conductivity.

C. Steady state thermal model

Fig. 20 shows the detailed steady state thermal model from the junction of the switch to the ambient. The total resistance from junction to ambient R_{JA} is 13.3396 °C/W. From Fig. 6 and the calculated R_{JA}, the junction temperature rise at rated operating conditions and 25°C cooling fluid temperature would be 100°C.

The accuracy of the steady state thermal model is assessed by running CFD simulations at two different operating conditions. The first one is 25°C water inlet temperature, 1 L/min flow rate, 2W switch loss and 20W machine module loss. The

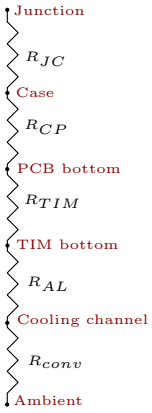
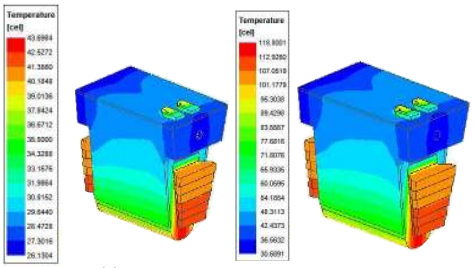


Fig. 20. The steady state thermal model from the inverter switch junction to the ambient (cooling fluid)



(a) (b)

Fig. 21. The CFD simulation results at (a) 1 L/min flow rate, 25°C water temperature, 2W switch loss and 20W machine loss (b)1 L/min flow rate, 25°C water temperature, 10W switch loss and 100W machine loss

second one is 25°C water inlet temperature, 1 L/min flow rate, 10W switch loss and 100W machine module loss. Fig. 21 (a) and Fig. 21 (b) show the temperature distribution of one integrated module for the first and the second operating conditions respectively. For the first case, the simulated and the steady state model calculated junction temperature is 39.3°C and 38.8°C respectively. For the second case, the temperature is 94.1°C from the simulations and 91.7°C from the lumped parameter model. A good correspondence between the model and the CFD simulations results. It worth mentioning that the CFD model takes 15 min to solve for the switch case temperature while the lumped parameter model requires the solution of the simple equation in (21).

$$T_J = T_A + P_{sw} R_{JA} \tag{21}$$

where, T_J is the switch junction temperature, T_A is the ambient temperature, P_{sw} is the switch loss.

V. VA RATING OF THE GAN MODULE

The steady state average switch loss at 14A peak line current (10A rms), 400V DC-link voltage and 50kHz switching frequency is 8.5W. The switch junction temperature from the steady state thermal model is 138.5°C which is less than the rated junction temperature of 150°C. The resulted VA rating of the 60×40 mm^2 inverter module is 5600VA. Fig. 22 shows

Fig. 22. The implemented GaN based half-bridge inverter module

the half-bridge inverter module implemented for the integrated drive.

VI. TRANSIENT ANALYSIS

The fast switching speed of the GaN switches can cause a high voltage spike over the switch due to the parasitic inductance of the circuit. This voltage spike can cause avalanche breakdown of the switch. This avalanche breakdown can only be avoided if the energy content of the voltage spike is below the avalanche energy and the peak instantaneous junction temperature is below the rated value [26]. Depending on the thermal capacitance from the junction of the switch to the ambient, the peak instantaneous temperature of the junction can be considerably higher than the average value estimated from the average switch losses and the steady state thermal model developed in the previous sections. So, an estimation for the peak junction temperature is crucial. The calculation of such a transient temperature variation requires a model for the instantaneous switch loss and a transient thermal model from the junction to the ambient.

A. Instantaneous switch loss

Both the conduction and the switching losses in the forward and the reverse paths of the switch vary with the time and the junction temperature. The variation with time results from the variation of the switch current with time while the variation with temperature results from the dependence of the drain to source resistance, the threshold voltage and the output characteristics of the switch on the junction temperature.

1) instantaneous conduction loss: The temperature dependant instantaneous conduction loss in the forward conduction path of the selected switch GS66508B is calculated from (22). The time dependence is handled by considering the instantaneous switch current $i_s(t)$ in the forward direction. The temperature dependence is handled by fitting the R_{ds} versus temperature curve with the polynomial in (22). The instantaneous conduction losses in the reverse conduction path is calculated from the reverse output charactereistcs by multiplying the reverse current by the corresponding voltage drop to get a curve for the instantaneous loss $P_{cond}(t)$ versus the reverse current $i_d(t)$ and then a fitting is done. $P_{cond}(t)$ is fitted by the polynomial in (23). The instantaneous reverse conduction loss of the selected switch doesn't show a significant dependence on the temperature. Fig. 23 (left) shows the datasheet and the fitted R_{ds} while Fig. 23 (right) shows the

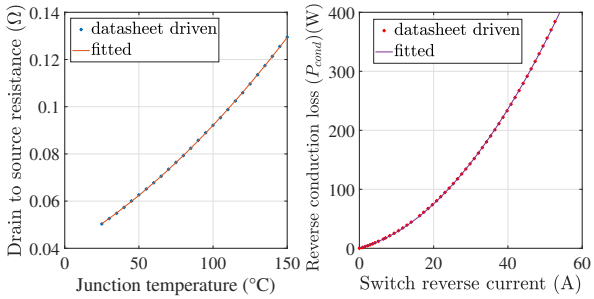


Fig. 23. The datasheet driven and the fitted drain to source resistance (R_{ds}) (left) and conduction loss in the reverse direction (right)

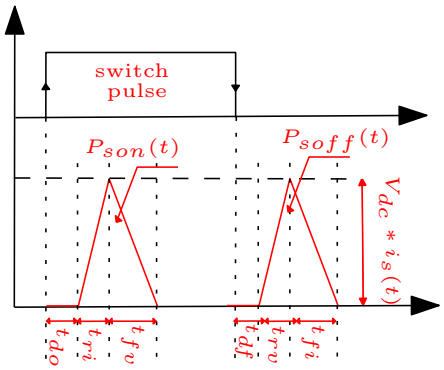


Fig. 24. The instantaneous turn on and turn off losses of the switch

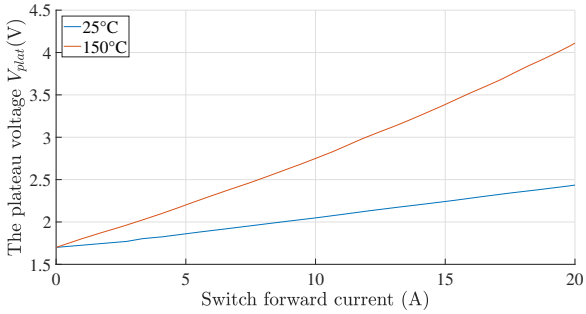


Fig. 25. The plateau voltage of the switch GS66508B versus the forward current at 25°C and 150°C junction temperatures

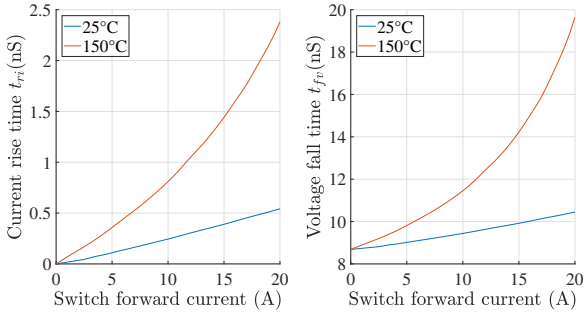


Fig. 26. The duration of the instantaneous turn on loss pulse versus the switch forward current at 25°C and 150°C and the parameters in Table IX

datasheet driven and the fitted loss in the reverse conduction path.

$$\begin{cases} P_{cons}(t) & = i_s^2(t) R_{ds}(T) \\ R_{ds}(T) & = K_1 T^2 + K_2 T + K_3 \end{cases} \tag{22}$$

where, K_1 = 1.5×10^{-6}, K_2 = 3.67× 10^{-4}, K_3 = 0.04.

$$P_{cond}(t) = K_4 i_d^2(t) + K_5 i_d(t) + K_6 \tag{23}$$

where, K_4 = 0.1, K_5 = 1.6, K_6 = 1.

2) instantaneous switching loss: The instantaneous turn on $P_{son}(t)$ and turn off $P_{soff}(t)$ power loss can be approximated by the energy pulses occurring at the turn on and turn off transition instants shown in Fig. 24. The peak of the pulse equals $V_{dc} \times i_s(t)$. The duration of the turn on and the turn off pulses defined by the current rise time t_{ri} and the voltage fall time t_{fv} for the turn on pulse and the voltage rise time t_{rv} and the current fall time t_{fi} for the turn off pulse can be calculated from (24).

$$\begin{cases} t_{ri} & = R_{gon} C_{iss} \ln \frac{V_{gon} - V_{th}}{V_{gon} - V_{plat}} \\ t_{fv} & = \frac{(V_{dc} - R_{ds} i_s(t)) R_{gon} C_{rss}}{V_{gon} - V_{plat}} \\ t_{rv} & = \frac{(V_{dc} - R_{ds} i_s(t)) R_{goff} C_{rss}}{V_{plat} - V_{goff}} \\ t_{fi} & = R_{goff} C_{iss} \ln \frac{V_{plat} - V_{goff}}{V_{th} - V_{goff}} \end{cases} \tag{24}$$

where, R_{gon}, R_{goff} are the turn on and the turn off external gate resistances respectively, V_{gon}, V_{goff} are the turn on and the turn off gate drive voltages respectively, C_{iss}, C_{rss} are the input capacitance and the miller capacitance of the switch respectively, V_{th}, V_{plat} are the threshold and the plateau voltage of the switch respectively.

Due to the increase of the R_{ds} (see Fig. 23 (left)), and V_{plat} (see Fig. 25) with temperature, the duration of the instantaneous switching loss pulses changes with the junction temperature. Normally, V_{th} decreases with the temperature, but for the selected switch GS66508B, V_{th} doesn't show significant change with temperature.

The durations of the turn on pulse (Fig. 26) and the turn off pulse (Fig. 27) are evaluated versus the switch forward current at the junction temperatures 25°C and 150°C at the parameters and the operating conditions in Table IX. Here, R_{gint} is the internal gate resistance of the switch. At the same forward current, all the durations of the turn on and the turn off loss pulses increase with temperature except t_{rv} because of the higher rate of change of R_{ds} with temperature than V_{plat}. The switching loss in the reverse conduction path is zero. So, it can be concluded that the instantaneous switching loss of the switch can be calculated from the instantaneous forward current and the junction temperature. The total instantaneous switch loss $P_s(t)$ can be calculated from (25) [27].

$$P_s(t) = P_{cons}(t) + P_{cond}(t) + P_{son}(t) + P_{soff}(t) \tag{25}$$

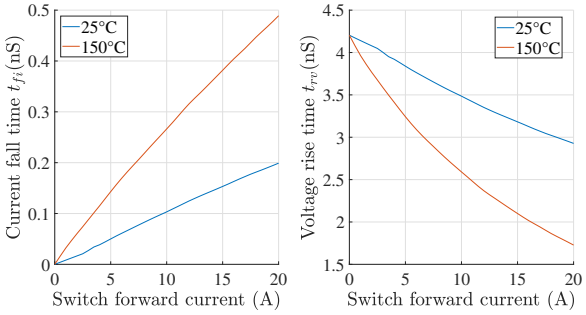


Fig. 27. The duration of the instantaneous turn off loss pulse versus the switch forward current at 25°C and 150°C and the parameters in Table IX

TABLE IX
Gate drive parameters and operating conditions

Parameter	Value
V_{dc} (V)	400
C_{iss} (PF)	260
C_{rss} (PF)	8.4
V_{th} (V)	1.7
R_{gon} (Ω)	10
R_{goff} (Ω)	1
R_{gint} (Ω)	1.13
V_{gon} (V)	6
V_{goff} (V)	0

B. Transient thermal model

The transient thermal model from the junction of the switch to the ambient is developed in this part.

1) Junction to case transient model: The junction to case thermal model of the switch can be represented by either Foster or Cauer networks [28]. Cauer network is chosen for the switch thermal model as it reflects the actual physical construction of the switch [29] and can be extended with the thermal models of parts from case to ambient. The Cauer network parameters can be fitted from the thermal impedance curve given in the datasheet or it can be extracted directly from the datasheet if it given. For the selected switch, the Cauer network is extracted directly form the datasheet.

2) Case to ambient transient model: The case to ambient model includes the PCB, the TIM, the aluminium shared cooling structure and the convection in the cooling fluid. Each of these components is represented by a first order RC network. The R part is the same as the values in Fig. 20. The thermal capacitance of each part C_{eq} is calculated from (26). Due to the localised heat generated by the switches, the thermal capacitance of each part is calculated from the equivalent heat transfer volume V_{eq} of the part which is calculated from the distance travelled by the heat through the part L_{eq}, the thermal conductivity of the part K_{eq} and the thermal resistance of the part R_{eq}. The transient thermal model from junction to the ambient is shown in Fig. 28. The parameters of the transient thermal model are calculated and

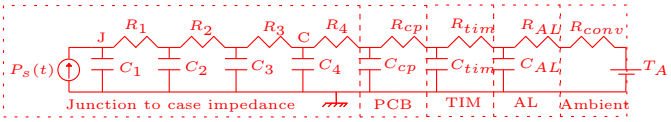


Fig. 28. The transient thermal model from the junction to the ambient

TABLE X
Transient thermal model parameters

Parameter	Value
R_1 (°C/W)	0.015
R_2 (°C/W)	0.23
R_3 (°C/W)	0.24
R_4 (°C/W)	0.015
C_1 (J/°C)	8 $\times 10^{-5}$
C_2 (J/°C)	7.4 $\times 10^{-4}$
C_3 (J/°C)	6.5 $\times 10^{-3}$
C_4 (J/°C)	2 $\times 10^{-3}$
The PCB (C_{cp}) (J/°C)	0.3095
The TIM (C_{TIM}) (J/°C)	0.0761
The Aluminium (C_{AL}) (J/°C)	0.8871

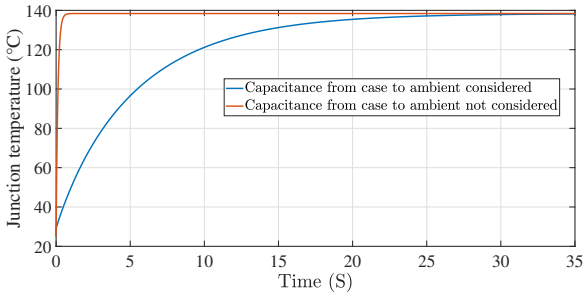


Fig. 29. The step response of the junction to ambient transient thermal model with and without the capacitance from the case to the ambient

listed in Table X.

$$\begin{cases} C_{eq} &= \rho_{eq} V_{eq} C_p \\ V_{eq} &= \frac{L_{eq}^2}{R_{eq} K_{eq}} \end{cases} \tag{26}$$

where, ρ_{eq} and C_p are the equivalent mass density and specific heat capacity of the part.

Fig. 29 shows the step response of the transient thermal model from the junction to the case with and without consideration of the capacitance of the case to the ambient components. The step amplitude is 8.5W and the ambient temperature is 25°C. The thermal time constant is 5.03s and 0.12s with and without the case to ambient capacitance. The influence of the capacitance from the case to the ambient would be a smoother junction temperature and a smaller difference between the peak and the average junction temperature.

Fig. 30 (left) shows the instantaneous switch loss resulting at the operating conditions in Table I. The large height needles correspond to the turn on and the turn off switching loss.

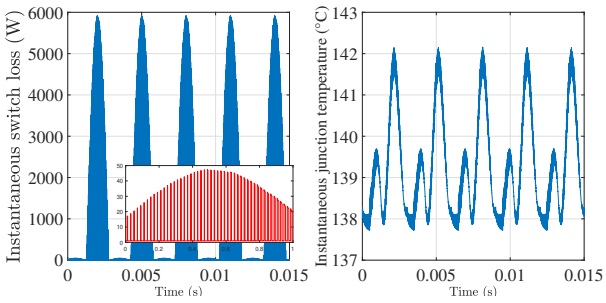


Fig. 30. The instantaneous switch loss (left) and junction temperature (right) at rated operating conditions with the loss in the reverse conduction path zoomed

The average value of the loss waveform is 8.5W which corresponds to the value calculated from (6) and (9). The instantaneous loss in the reverse conduction path is zoomed on the figure for comparison of instantaneous loss amplitudes. The instantaneous junction temperature is shown in Fig. 30 (right). The average temperaure is 138.3°C and the peak value is 142.5°C. A difference of 4.5°C between the peak and the average value results mainly due to the large switching loss needles at the transition moments of the switch.

VII. Influence of the Parasitics

Fig. 31 shows the half-bridge inverter module with the different parasitics that influence the switching loss of the switches namely the gate drive loop inductance L_g, the common source inductance L_{cs} and the commutation loop inductance L_{loop}. The L_{loop} can be calculated from (27).

$$\begin{cases} L_{dclink} &= ESL + L_+ + L_- \\ L_{comm} &= L_{d1} + L_{cs1} + L_{s1} + L_{d2} + L_{cs2} + L_{s2} \\ L_{loop} &= L_{dclink} + L_{comm} \end{cases} \quad (27)$$

where, ESL, L_+, L_-, L_{d1}, L_{s1}, L_{d2}, L_{s2} are the equivalent series inductance of the DC-link capacitors, the inductance of the DC-link busbar positive plate, the inductance of the DC-link busbar negative plate, the drain and the source inductances of the upper and the lower switches respectively, L_{dclink} is the total DC-link inductance.

The L_g reduces the rate of rise/fall of the gate current during the turn on/off transition of the switch. This rate reduction results in a longer turn on/off transition duration and hence a higher switching loss. Thanks to the additional source sense pin in the selected switch (pin 2 in Fig. 13 (a)), the L_{cs} is negligible. The L_{loop} has two components: L_{dclink} which represents the parasitic inductance of the DC-link capacitors and busbar, L_{comm} which represents the parasitic inductance of the switches and the inverter module PCB. The decoupling capacitors C_{d1}, C_{d2}, C_{d3} in Fig. 31 compensate the effect of the L_{dclink}. The L_{comm} causes a voltage dip/spike in V_{ds} during the turn on/off transition of the switch causing a decrease/increase in the turn on/off switching loss. V_{ds} during turn on/off transition of the switch can be calculated from (28).

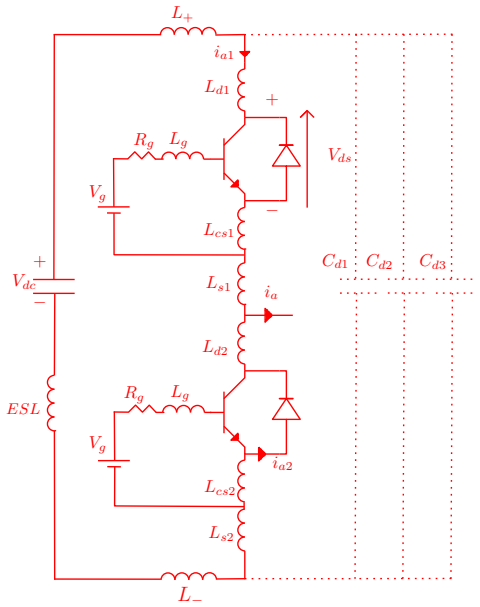


Fig. 31. The half-bridge inverter module with the parasitics that influence the switching loss of the switches

Fig. 32. FEM model of the half-bridge inverter module PCB

$$V_{ds} = V_{dc} \mp L_{comm} \frac{di_{a1}}{dt} \quad (28)$$

where, V_{dc} is the DC-link voltage, i_{a1} is the upper switch current during transition.

The L_g and the L_{comm} are computed at different frequencies using electromagnetic finite element (FEM) simulation for the inverter module PCB model shown in Fig. 32. Fig. 33 shows the variation of the L_g and L_{comm} with the frequency. It can be seen that the inductance decreases with frequency until 50MHz and then it plateaus. From Fig. 26, the maximum turn on time of the switch occurs at the rated current and mounts to 15.5 ns, the corresponding frequency is 64.5 MHz. From Fig. 27, the maximum turn off time is 4.2 ns and the corresponding frequency is 0.23 GHz. The frequency corresponding to the turn on/off moments is beyond the plateau frequency. Therefore, from Fig. 33, the values of L_{comm} and L_g are 9.22 nH and 3.08 nH respectively.

The turn on/off transition time delay resulting from the L_g is calculated by simulating the circuit in Fig. 34 (a)/(b) with the switch s off/on. The resulted turn on/off delay from L_g is 0.055 ns.

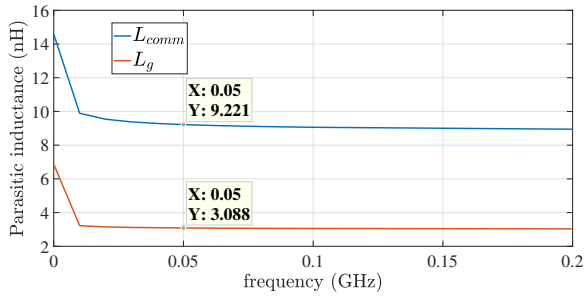


Fig. 33. The variation of L_{loop} and L_g with frequency

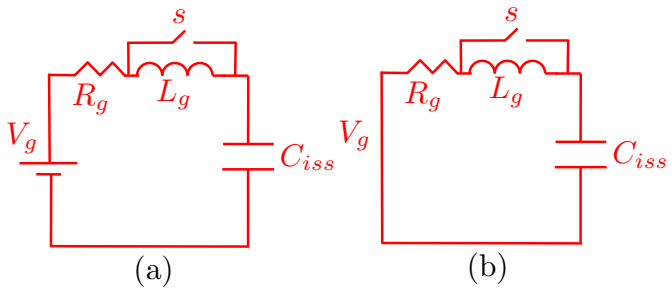


Fig. 34. The L_g turn on/off delay calculation circuits (a) turn on transition delay, (b) turn off delay.

The voltage spike resulting from the L_{comm} during the turn off transition at the rated current is $L_{comm}\frac{di_{a1}}{dt}$ and amounts to 37.5V. The voltage dip at the turn on time is 8.5V. The peak value of the turn on energy pulse and the turn off energy pulse is modified to $(V_{dc} - 8.5)\ i_s(t)$ and $(V_{dc} + 37.5)\ i_s(t)$ respectively. The resulted peak temperature is the same as the one without consideration of the parasitics as the increase in the turn off energy loss compensated the decrease in the turn on energy loss and the delay in the turn on/off transition time due to the L_g is small.

VIII. Experimental Results

The three teeth integrated setup in Fig. 35 is built to validate the converter modelling. The setup consists of three stator teeth, three half-bridge inverter modules, a DC-link PCB and an R = 8 Ω, L = 3 mH load. A 3D CAD model for the experimental setup is shown in Fig. 36 to further illustrate the detailed construction and the materials of the setup components. Table XI contains the materials and the geometrical parameters of the different parts in the setup.

TABLE XI
Material specifications of the experimental setup

part	specifications	
	material	geometry
winding	copper	round wire, 0.9 mm diameter, 90 turns
core	M100-23p	0.23 mm laminations
cooling structure	Aluminium	2 mm laminations

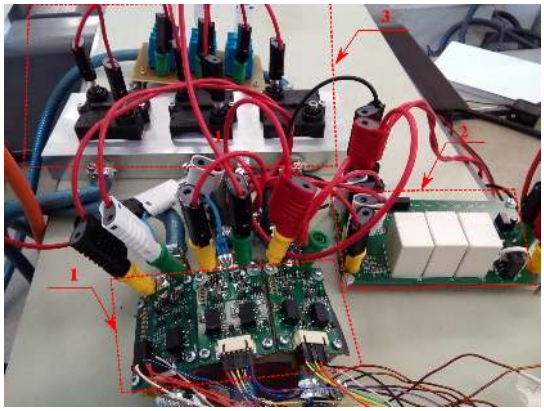


Fig. 35. Experimental setup: (1) The three teeth, (2) The DC link board, (3) The Load

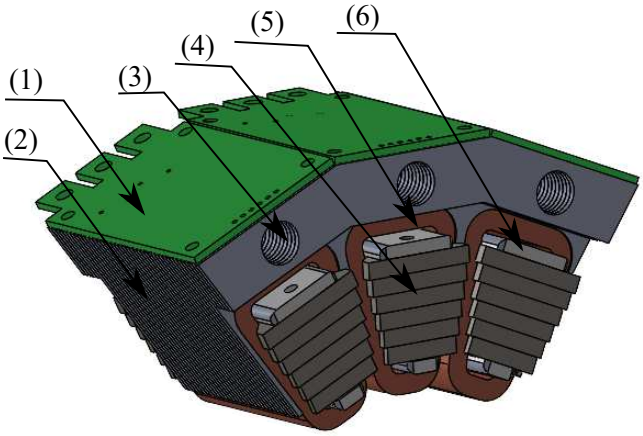


Fig. 36. 3D CAD model for the three teeth experimental setup: (1)inverter module PCB, (2) aluminium shared cooling structure, (3) cooling channel, (4) core, (5) winding, (6) epoxy infiltrated gap.

A. switch loss measurements

The switch conduction and switching losses are measured using one half-bridge module connected as shown in Fig. 37 (a) for the conduction loss measurements and Fig. 37 (b) for the switching loss measurement.

The two switches of the half-bridge in Fig. 37 (a) are turned on and a variable DC-voltage is applied between the drain of the upper switch and the source of the lower switch. At different voltages, the voltage is measured using the differential probe (RS 729-6677), the source current of the lower device is measured using the current probe (TCPA 300). All waveforms are visualized using a 1GHz scope. The junction temperature is measured using the thermal camera (GTC-400). The measurements are done at 1 LPM water flow rate and 25 °C inlet temperature. From these measurements, the measured drain to source resistance $R_{dsm}(T)$ of one device is calculated and plotted in Fig. 38. The conduction loss can be calculated at any junction temperature and switch current from (3).

Using the circuit shown in Fig.37 (b) with the upper transistor kept off and the lower transistor switched with f_s=10kHz,

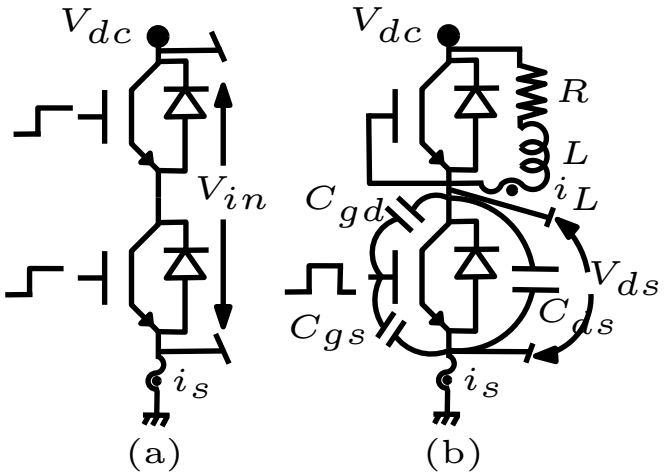


Fig. 37. The schematic diagram for the circuit used for (a) conduction loss measurements, (b) switching loss measurements

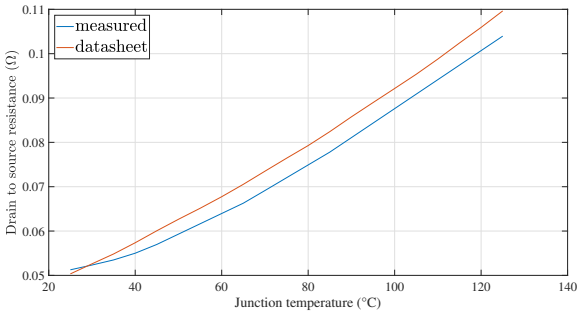


Fig. 38. Measured switch resistance R_{dsm} versus junction temperature

the loss of the lower device is measured and compared to the values calculated from (3)-(9). The measurements are performed at 175V DC-link voltage, 8.4A switch current and different junction temperatures. Fig. 39 shows V_{ds}, i_s, V_{gs} of the lower switch and i_L as well at 51°C junction temperature. The ringing that can be noticed in the current waveform results from the discharge of the output capacitance during the turn on transient of the switch. The total switch loss is calculated from (29) using the math mode of the scope, the conduction loss is calculated using R_{dsm} and the rms value of the current calculated by the scope and the switching loss is calculated from the difference. Fig. 40 shows the total loss, the conduction loss, and the switching loss at different junction temperatures measured and calculated. It can be noticed that the analytically calculated overestimates the conduction loss a bit and underestimates the switching loss a bit but the total loss is in a good agreement with the measurements.

$$P_{swtm} = \int_0^{T_s} V_{ds}(t) i_s(t) dt \tag{29}$$

where, P_{swtm} is the total switch loss, $T_s = \frac{1}{f_s}$.

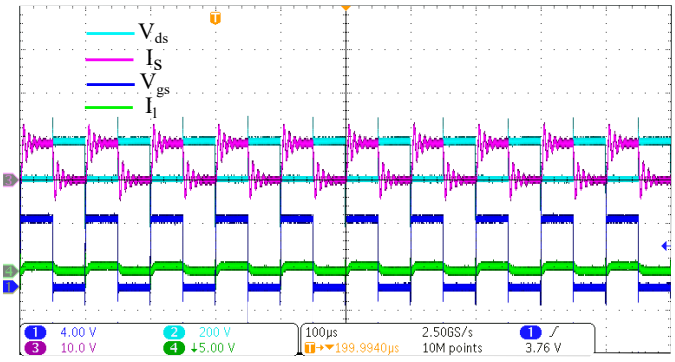


Fig. 39. Switch loss measurements waveforms measured at 175V DC-link voltage, 8.4A switch current and 51°C junction temperature

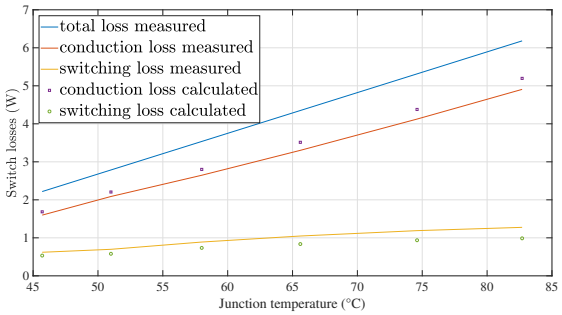


Fig. 40. Switch loss measurements measured at 175V DC-link voltage, 8.4A switch current and different junction temperatures

B. Modelling validation

The thermal model is validated by heating the windings and the switches by a well-defined conduction loss. The switches of the inverter modules are connected as shown in Fig. 41 (left) and supplied from a DC-source. The coils are connected in series and supplied from a different DC-source as shown in Fig. 41 (right). The DC-source of the three coils is adjusted until 75 W total loss is obtained. At different values of the inverter DC-voltage, the power loss is recorded and the temperature of the switch junction is measured by a thermal camera and recorded. The operating conditions of the experiment are listed in Table. XII.

Fig. 42 shows the measured switch junction temperature rise at different switch losses. The slope of Fig. 42 gives the junction to the cooling ambient thermal resistance and amounts to 13.498 °C/W an indication for a good correspondence with the CFD simulations.

TABLE XII
experimental operating conditions

Variable	Value
per coil loss (W)	25
inlet water temperature (°C)	25
flow rate (L/min)	1

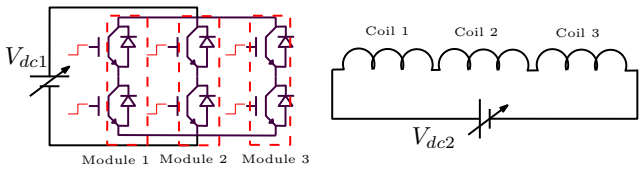


Fig. 41. The connection of the inverter modules (left) used to generate Fig. 42 and the coils connection used to generate 75 W total loss in the three coils (right)

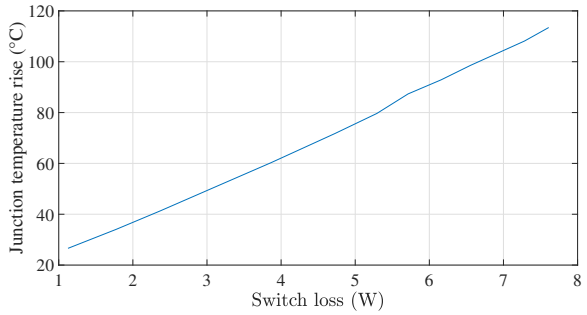


Fig. 42. The measured junction temperature rise versus the switch loss at the operating conditions in Table XII

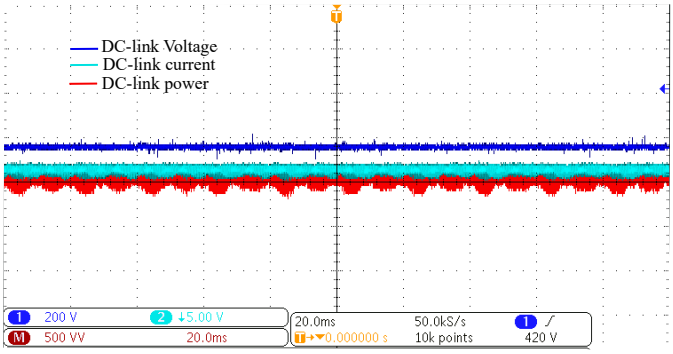


Fig. 43. The DC-link voltage, current and power measured at $V_{dc} = 175$V. The input voltage in blue and the output power in red

The three inverter modules are operated as three phase inverter and the switch loss is computed from the input/output power measurement and from the temperature measurement and the thermal resistance estimated from Fig. 42 . The PWM technique used is the sinusoidal PWM. The PWM pulses of frequency of 10kHz are generated using the MicroLabBox dSPACE. The measurements are carried out at a DC-link voltage of 175V. The line currents are measured with the on-board sensor ACHS7123 and the DC-link current is measured using the current probe TCPA300 from Tektronix. The waveforms are visualized using a 1GHz Tektronix scope. The DC-link current, voltage and input power are shown in Fig. 43. The average input power is 1115W. The output current of 9.5A peak value, voltage and power per phase are shown in Fig. 44. The average output power is 1094.5 W. The total power loss of the three inverter modules is 20.5W and the loss per switch is 3.41W.

The temperature of the switches is measured and the temperature distribution of the inverter module is visualized using a thermal camera. Fig. 45 shows the temperature distribution over one inverter module. The junction temperature is 67.9°C. The estimated switch loss is 3.2W, which is in good correspondence with the electrically estimated one, an indication of the validity of the thermal model introduced in section IV with PWM operating conditions. Note that the temperature of the low power components on the inverter module remains low. The efficiency of the three inverter modules is 98.2 %.

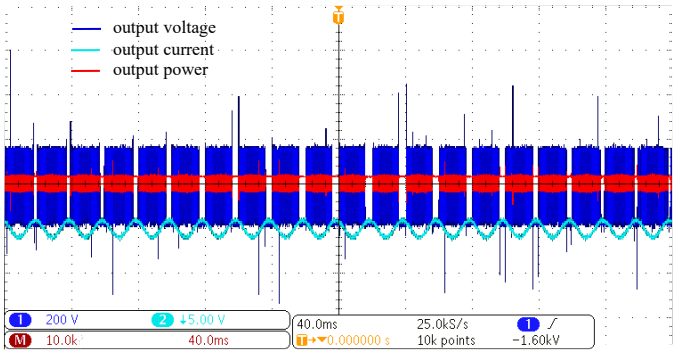


Fig. 44. The output current, voltage and power per phase measured at 9.5A peak phase current. The output voltage in blue and the output power in red

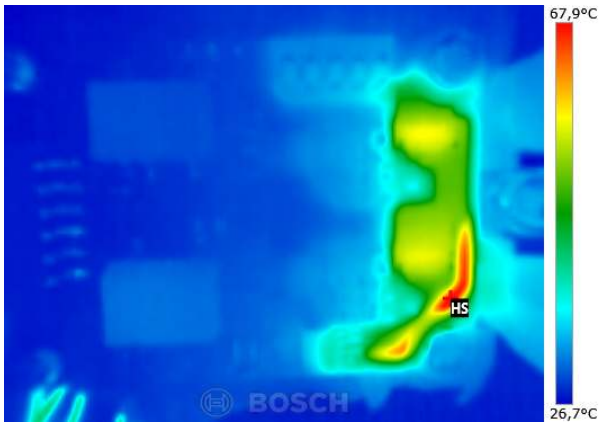


Fig. 45. The inverter module measured temperature distribution at 175V DC-link voltage, 9.5A peak line current

The temperature of the stator elements (core and windings) is also measured with a thermal camera and a PT100 RTD temperature sensor placed on the bottom end winding. Fig. 46 shows the core temperature of the three teeth and amounts to 54 °C. Fig. 47 shows the bottom end winding temperature of the three teeth and amounts to 58.7°C. The transient bottom end winding temperature is measured with the PT100 sensor and shown in Fig. 48. The temperature measured with the thermal camera is in good agreement with the value measured by the PT100 RTD.

To validate the accuracy of the CFD model introduced in section IV in predicting the stator elements temperature, the simulation is performed at the operating conditions of the experiments (Table XII) to compare the results with the measurements in Fig. 46 and Fig. 47. Fig. 49 shows the simulation results with core temperature of 52.58 °C

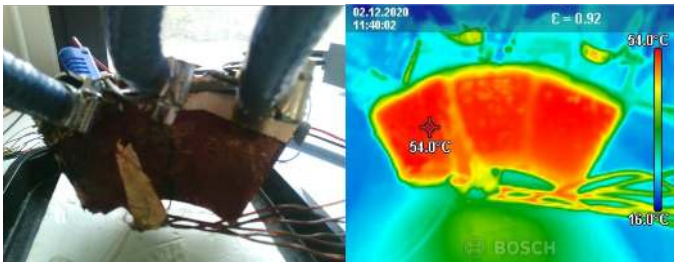


Fig. 46. The measured temperature distribution over the core of the three teeth at the operating conditions in Table XII

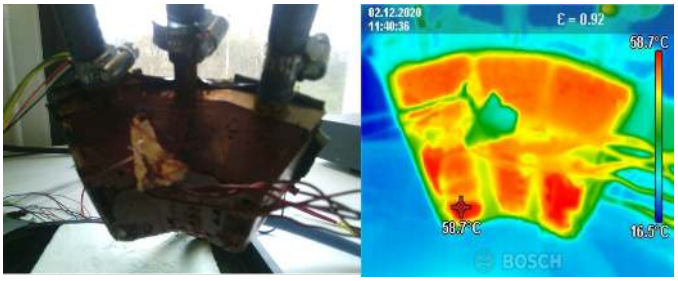


Fig. 47. The measured temperature distribution over the bottom end winding of the three teeth at the operating conditions in Table XII

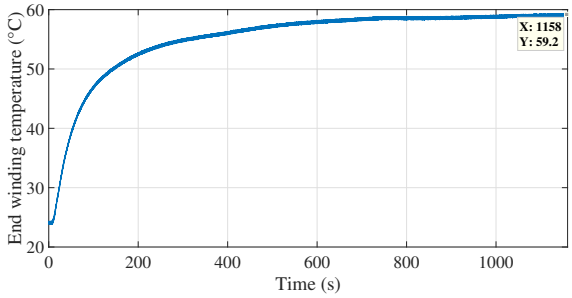


Fig. 48. The measured transient temperature of the bottom end winding measured with PT100 RTD sensor at the operating conditions in Table XII

and winding hot spot temperature of 57.77°C an indication of a good correspondence between the simulation and the measurements.

IX. Conclusion

A discrete GaN based inverter module is designed for a radially stator mounted (RSM) integrated drive topology for axial flux machines and its size and thermal performance are optimized. The inverter is modelled using steady-state and transient lumped parameter networks.

The VA rating of the 60×40 mm^2 inverter module designed for the case study axial flux machine considered in the paper is 5600VA.

The gate and the commutation loop inductances of the designed inverter module are extracted and resulted in 9.22 nH and 3.08 nH respectively and their influence on the loss and the peak temperature of the inverter switches is proven to be minor.

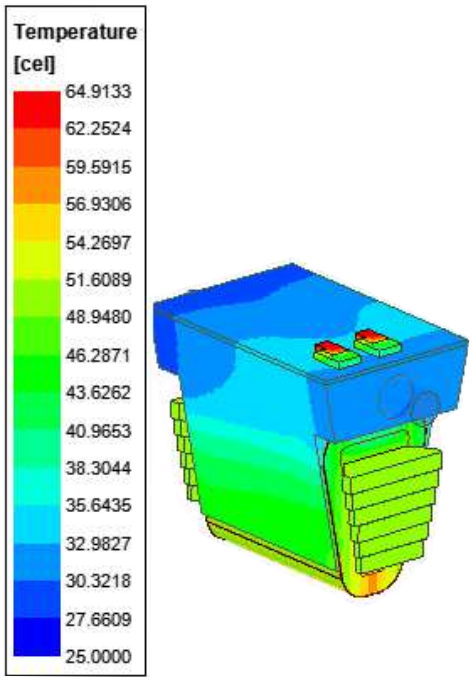


Fig. 49. The simulated temperature distribution at 3.42W switch loss, 25W winding loss and 1 LPM flow rate

The modelling is validated using CFD simulations and experimental measurements. The experimental measurements are performed using well-defined conduction losses and real PWM waveforms.

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