Elimination of Non-Simultaneous Triggering Effects in Finger-type ESD Protection Transistors Using Heterojunction Buried Layer

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Abstract

This paper presents a novel technique to eliminate non-simultaneous triggering effects in finger-type ESD protection transistor using SiGe heterojunction buried layer structures. It is confirmed that lower snapback voltage and maximum lattice temperature are obtainable in the new structure based on device simulation. As a result, current localization and lattice overheating of a finger-type protection transistor caused by process variations can be avoided in this structure.

1. Introduction

A thin oxide NMOS transistor is the common ESD protection device in CMOS VLSI, as shown in Fig. 1, where a parasitic npn bipolar transistor action shunts high-level current. When positive transient pulses are forced to the drain with the gate and the source connected to ground, the n^+/p diode at the drain is in reverse bias until avalanche breakdown occurs. However, this configuration suffers from poor performance for ESD as modern devices employ shallow junctions, silicided contacts, higher well doping, thinner gate oxides and more compact layouts.

A proposed new NMOS protection transistor that includes a buried SiGe narrow-bandgap layer, as shown in Fig. 2. Since the bandgap of the germanium is narrower than that of the silicon, a discontinuity in the valence band is created in the Si/SiGe heterostructure, which can be effectively used to confine the mobile holes in the SiGe channel. The main idea of the proposed ESD protection structure is to improve the current gain using the SiGe layer as in the case of HBTs, since protection transistors turn on due to bipolar transistor action under ESD stress. Furthermore, because the layer is formed far below the silicon surface, the device operates as a normal NMOS transistor during standard circuit operation. Therefore, we can use the advantages of both BJTs and MOSFETs by using a SiGe NMOS transistor as an ESD protection device. As a result, the BJT can suppress local overheating on the silicon surface by providing faster turn-on and more uniform current distribution [1].

Current gain (β) of the SiGe layer is shown to be higher exponentially by a factor $\exp(\Delta E_V/\mathrm{kT})$, as reflected in the energy band diagram of Fig. 3. This in turn affects the current gain as follows:

$$\beta \cong \frac{N_E D_{nB} W_E}{N_B D_{pE} W_B} e^{\Delta E_V / kT} \tag{1}$$

where

$$\begin{aligned} \Delta E_{V(Si/SiGe)} &= \Delta E_C - (\Delta Eg_{(Si)} - \Delta Eg_{(SiGe)}) \\ &\cong -(\Delta Eg_{(Si)} - \Delta Eg_{(SiGe)}) \\ &= -\Delta Eg_{(Si/SiGe)} \end{aligned} \tag{2}$$

In addition, since the main current path can form along the buried layer, the local overheating of the silicon surface can be avoided in this new structure.

2. Phenomena and Simulation

Excellent ESD protection of NMOS transistors can be achieved by using sufficiently large devices — finger or ladder structures as illustrated in Fig. 4 [2]. According to experiments, however, the total active width of a 4 × 100 μm (W = 400 μm) four-gate multi-finger transistor is only 200 μm, which implies only half the fingers are effective during the snapback operation owing to the non-uniform current distribution and non-simultaneous triggering of the four gates [3]. The discretization of threshold in multi-finger structures is caused by both asymmetries between fingers due to substrate resistance and process variations of effective gate length and the doping profiles. This in turn produces RC delays for triggering of the adjacent fingers. Moreover, bus connections, complex bussing, parasitic resistance, inadequate contacts, and vias, are known as the common errors that cause ESD failures. In order to avoid these problems, the protection transistor must be capable of shunting a high level current during fast ESD transients, while maintaining low voltage and power consumption for a uniform current distribution.

This work presents results for the new structure that improves the protection performance ; results are validated using thermal modeling, mixed circuit-device analysis and heterostructure device structures [4]. The characteristics of the SiGe heterojunction are analyzed using a heterojunction analysis module, which handle the properties of materials for the heterojunction such as energy bandgap, electron affinity, density of states, as well as various transport parameters used in describing recombination and mobility.

3. Analysis and Results

A multi-finger transistor with two gates is constructed based on two-dimensional process simulation [5], as shown in Fig. 5. The transistor exploits an n^+ polysilicon gate and retrograde well technology with the gate oxide thickness of 80 Å. The gate lengths are 0.50 μm and 0.55 μm for Tr.1 and Tr.2, respectively, assuming that the length difference is caused by process variations. The gate width of both transistors is 85 μm.

Also, the same multi-finger transistor structure with SiGe buried layers is constructed with a Ge mole fraction of 0.2. In reality, the layer can be realized after the Vth channel implantation. Ge ions are implanted into the active area of the protection transistor with a peak dopant concentration that occurs around 1400 Å below the silicon surface. Using the Machine-Model (MM) with 300 V, applied to the protection

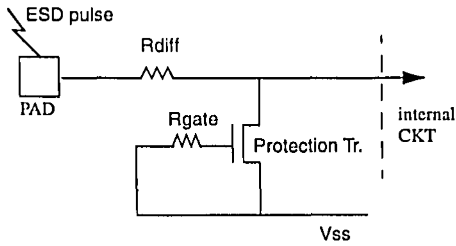


Fig. 1. ESD protection circuit in a CMOS technology.

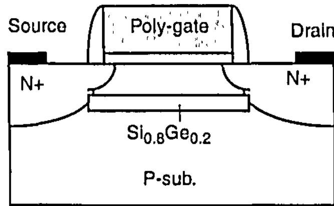


Fig. 2. New ESD protection NMOS Tr. with a buried layer.

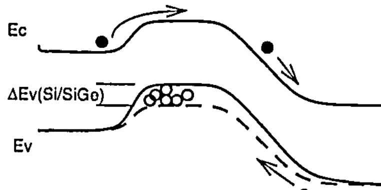


Fig. 3. Energy diagrams of n+/p/n+ (dot line) and n+/p-SiGe/n+ (solid line).

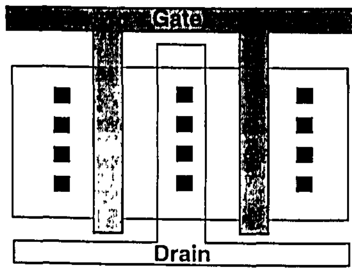


Fig. 4. A simple layout of finger NMOS Tr.

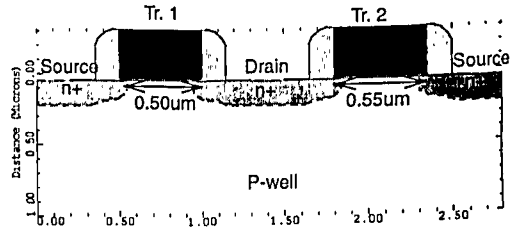


Fig. 5. ESD simulation structure for a finger NMOS Tr.

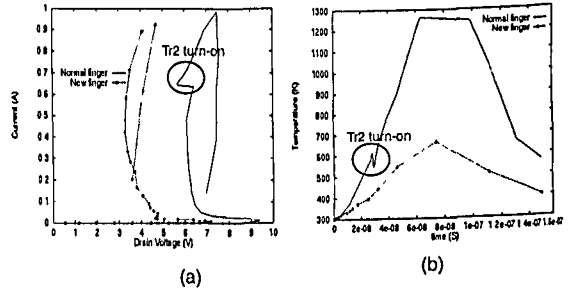
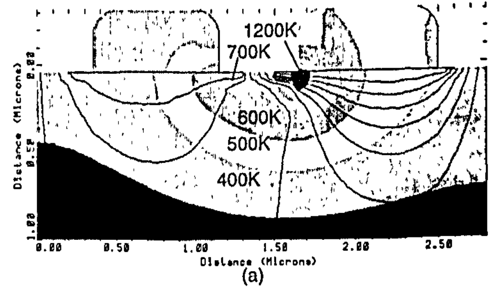


Fig. 6. ESD simulation results against MM 300V. (a) Vds-Ids, (b) Time-Temperature.



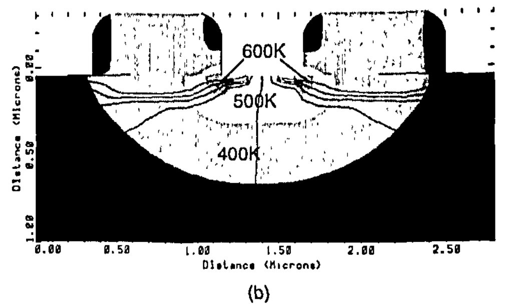


Fig. 7. Distributions of maxinum temperature and current flow at t=60ns. (a) Normal finger Tr., (b) New finger Tr.

circuit as shown in Fig. 1, the internal device characteristics and thermal variations are investigated as a function of time.

The simulated snapback voltages are 6.5 and 4.5 V for normal and new transistor structures, respectively, as shown in Fig. 6 (a). Higher snapback voltage implies that the device is clamped by the higher drain voltage, resulting in high power generation and lattice temperature [6]. Also, second breakdown occurs in the normal finger structure as denoted with circles. In addition, we can see that Tr. 1 and Tr. 2 do not turn-on at the same time from the circles of Fig. 6 (b) for the normal transistor configuration, where Tr. 2 turns on after 30 ns. (Tr. 1 turns on at 1ns). Thus, its effective width is only 85 μm, not 2 × 85μm before 30 ns, which causes current localization to Tr. 1. Once Tr. 2 turns on, however, the current localization moves to Tr. 2. As a result, the maximum lattice temperature rises by as much as 1230 °K at t = 60 ns, as shown in Fig. 7 (a).

Meanwhile, for the new structure, Trs. 1 and 2 turn on simultaneously at the initial stage because the collection for ionized holes by the buried layer is effective despite Tr. 2's relative larger channel length. Thus, the effective device width becomes 2 × 85 μm as expected. As time goes on, almost the same amount of current flows to each device so that much lower maximum temperatures (600 °K) are generated at t = 60 ns, as shown in Fig. 7 (b). Therefore, the current localization and lattice overheating can be avoided in the new finger transistor configuration.

4. Conclusions

ESD performance of a SiGe protection transistor is studied and compared to a normal NMOS finger-type protection transistor. Bandgap engineering with SiGe heterojunction layers is shown to be efficient in eliminating the non-simultaneous triggering effects in finger-type ESD devices. This device is a good candidate as future generation ESD protection in RF and ultra high density VLSI circuits.

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