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Elucidating 1S1R operation to reduce the read voltage margin variability by stack and programming conditions optimization

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***Abstract*—1S1R operation behavior and read margin variability are elucidated for the first time to our knowledge. To this aim, an extensive experimental study is performed on HfO_2 OxRAM technology co-integrated with GSSN-based Ovonic Threshold Selector (OTS) in 4kb memory arrays, supported by deep theoretical analysis. A semi-analytical dynamic model is developed for selector operation, describing OTS switching variability. The voltage repartition in the 1S1R stack during the switching operation is clarified. The 1S1R read voltage margin is quantified statistically, based on OTS switching voltage dispersion, OxRAM variability and margin degradation during endurance. Based on this theoretical and experimental study, 1S1R figures of merit (overall functionality, reliability, and maximum bank size) are optimized based on OTS and OxRAM devices' features and programming conditions.**

***Index Terms*--chalcogenide, crossbar, OTS, operation variability, resistive RAM**

I. Introduction

Resistive Random-Access Memory (RRAM) is one of the most promising candidates for high-density crossbar architectures [1-2] targeting memory and neuromorphic circuit applications [3]. In this aim, OxRAM co-integration with Ovonic Threshold Switching (OTS) back-end selector is one of the most competitive approaches for the sneak-path current reduction in a high-density crossbar array. In previous works, OTS (1S) was successfully co-integrated with HfO_2 based OxRAM (1R) [4-5], demonstrating promising functionality for large crossbar arrays. However, among the various device parameters, read voltage margin was identified as one of the most critical feature for 1S1R stack. Beyond device functionality, it is thus mandatory to deeply analyze and understand how both OxRAM and OTS affect the reading window. In this work, we present a theoretical and experimental statistical study of the 1S1R read voltage margin and propose to reduce its variability through device lifetime, by optimizing the stack and programming conditions. Moreover, knowing optimized stack and programming conditions, we provide general guidelines to guarantee the overall functionality and reliability of crossbar arrays depending on their size.

II. Technological Details

OxRAM is co-integrated with OTS back-end selector in 4kb 1S1R matrix configuration. A transistor is used as current limiter. Magnetron sputtered Ge-Se-Sb-N (GSSN) alloy is used as OTS, sandwiched between two Carbon electrodes to improve endurance [6]. 5nm-thick ALD HfO_2 is integrated with a 5nm PVD Ti scavenging layer for the OxRAM device [7]. Showed in **Fig.1 (a)**, **(b)** and **(c)**, SEM top view, TEM cross section and EDX image of the stack demonstrate the consistent co-integration of all deposited layers.

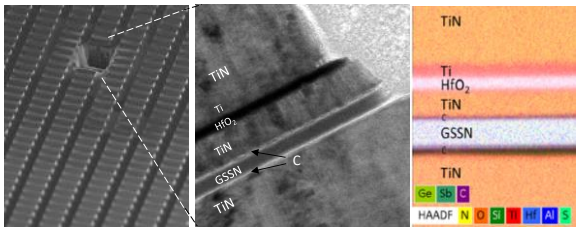

Fig. 1. (a) SEM top view of 4kb 1S1R array composed of HfO_2 based OxRAM and GeSeSbN (GSSN) based OTS. (b) TEM cross section of a 1S1R stack. (c) EDX image of the 1S1R stack showing the elements constituting the layers.

III. Results and Discussion

A. OTS and OxRAM switching characteristics

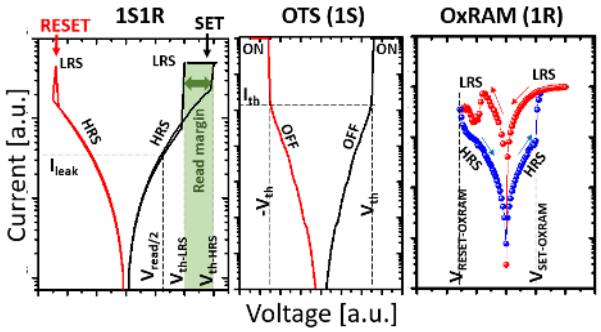

Fig. 2. IV of 1S1R, 1S (GSSN OTS) and 1R (OxRAM, blue for HRS, red for LRS) devices showing the device's key electrical parameters used in this work.

Fig.2 shows typical IV switching characteristics of our 1S1R, 1R and 1S devices together with the key electrical parameters used in this work. In particular, the reading voltage should be comprised between $V_{th\text{-}LRS}$ and $V_{th\text{-}HRS}$ (respectively the 1S1R switching voltages in low and high resistive states) defining the read margin.

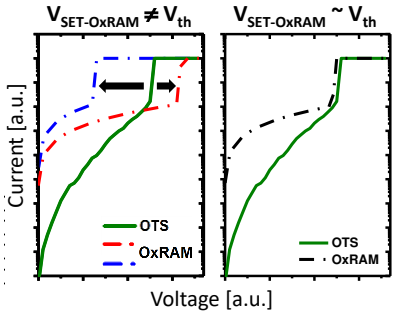

Fig. 3. IV SET switching characteristics of 1S and 1R devices. While preserving satisfactory device insulating properties, switching voltages for memory and selector devices should be of the same order to avoid voltage stress in the stack.

Fig.3 plots the IV SET characteristics of 1R and 1S devices. The OTS switching voltage V_{th} being linked to its isolating properties [6], 1S1R optimization strategies must engineer both OTS and OxRAM switching voltages without compromising OTS insulating properties.

B. Semi-analytical model for OTS switching

Semi-analytical simulations of 1S devices' operations are developed based on filamentary field-driven switching theory [8, 4]. OTS switching is described by the successive nucleation of metastable domains within the GSSN chalcogenide layer. OFF-to-ON switching (*resp.* ON-to-OFF relaxation) through filament nucleation (*resp.* dissolution), together with the main equations implemented in the model, are detailed in **Fig.4** and **Fig.5**. After firing, once the OTS returns to the OFF state, a residual filament remains.

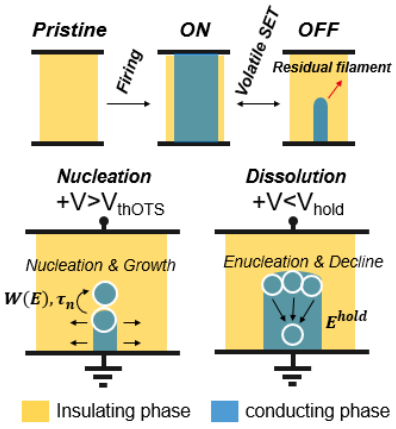

Fig. 4. Description of the semi-analytical model used to simulate the switching dynamics of the OTS: schematics of the simulated OTS material in pristine, ON and OFF states. The conductive state being insured by the growth of a conductive filament, filament dynamics for device switch to ON state (nucleation) and relaxation to OFF state (dissolution) are presented.

Height nucleation barrier (free energy maximum)

$$W(E) = \frac{W_{0\_height}}{\left(1 + \frac{H^3}{8 * W_{0\_height}} \epsilon_r E^2\right)^2}$$

Holding activation energy

$$E^{hold} = \frac{E_0^{hold}}{1 + \exp\left(-\frac{V - V_{hold}}{\sigma_{V_{hold}}}\right)}$$

Radius nucleation barrier (free energy maximum)

$$W(E) = \frac{W_{0\_height} * k}{\left(1 + \frac{R^3}{8 * W_{0\_height} * k} \epsilon_r E^2\right)^2}$$

Nucleation time

$$\tau_n = \frac{1}{\upsilon} * \exp\left(-\frac{W(E)}{k_b * T}\right)$$

E=electric field [V/m]
$W_{0\_height} = E_0^{hold}$ *= zero field nucleation barrier* = 2.75eV
k *= depolarizing factor influence* = 1.1
H *= domain critical height* = 6nm
R *= domain critical radius* = 3nm
ϵ_r *= relative permittivity* = 10 $\sigma_{V_{hold}}$=0.9V

Fig.5. Description of the semi-analytical model used to simulate the switching dynamics of the OTS: equations implemented in the model.

Fig.6 shows experimental and simulated OTS firing and threshold voltage evolution with GSSN thickness. A residual filament of ~44% of the GSSN thickness after firing process is used for OTS threshold V_{th} simulation, satisfactorily capturing experimental results. Assuming a standard deviation of 0.15eV for holding activation energy (E^{hold}), 10nm-thick GSSN-based experimental and simulated OTS holding voltage (V_{hold}) distributions are presented in **Fig.7 (a)** with a median of 0.9V. V_{hold} is a key parameter quantifying the voltage that drops on the selector in the ON state. Moreover, both experimental and simulated OTS switching voltage V_{th} evolution with voltage sweep rate are presented in **Fig.7 (b)**. All in all, successful agreement between experimental and simulated data is evidenced for pristine, ON and OFF cell resistive states (**Fig.4**) in quasi-static and dynamic regimes.

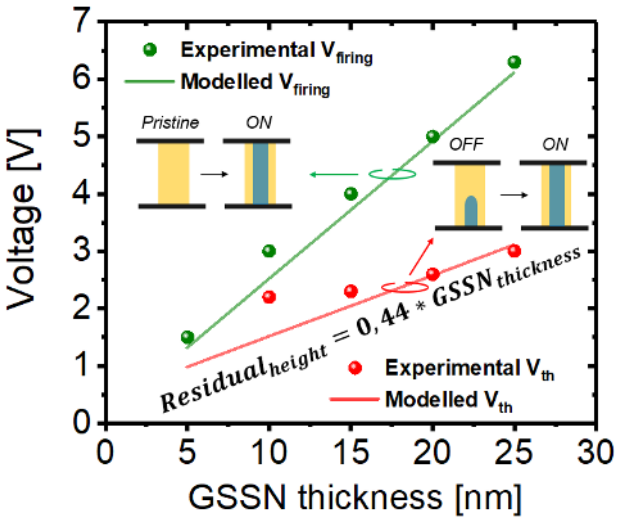

Fig. 6. Experimental and simulated selector firing and threshold voltage as function of GSSN thickness (considering a residual filament of ~44% of the GSSN thickness after relaxation to OFF state).

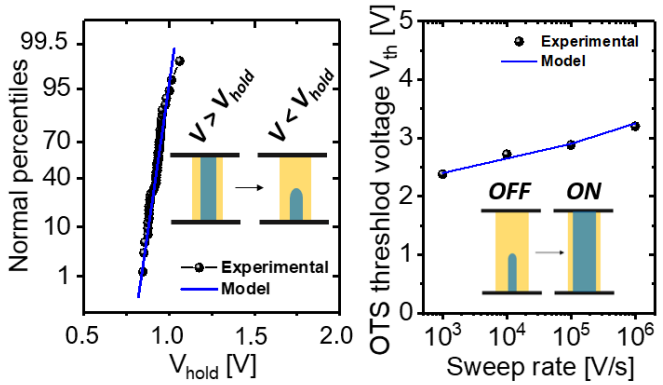

Fig. 7. (a) Experimental and simulated distribution of the OTS holding voltage for 10nm GSSN. 0.15eV of holding activation energy (E^{hold}) dispersion is considered for the simulation. (b) Experimental and simulated OTS switching voltage (V_{th}) as function of voltage sweep rate. Faster ramps lead to higher switching voltages.

C. *OxRAM+OTS read voltage margin variability reduction*

a. *1S1R programming conditions impact on read voltage margin*

Fig.8 shows experimental and simulated V_{firing}, $V_{th\text{-}HRS}$ (high resistive state) and $V_{th\text{-}LRS}$ (low resistive state) 1S1R switching voltages. $V_{th\text{-}HRS}$ > $V_{th\text{-}LRS}$ when the OxRAM is in HRS due to the additional voltage that drops on the OxRAM. The higher R_{HRS}, the higher $V_{th\text{-}HRS}$ switching values and so the larger the 1S1R read voltage margin ($V_{th\text{-}HRS}$-$V_{th\text{-}LRS}$). Particularly, the 1S1R reading voltage is comprised within the read voltage margin. $V_{th\text{-}HRS}$ distributions, using OTS modelling (previous section) and OxRAM (Poole Frenkel mechanism) conduction characteristics, are calculated for various R_{HRS} (blue discontinuous lines in **Fig.8**).

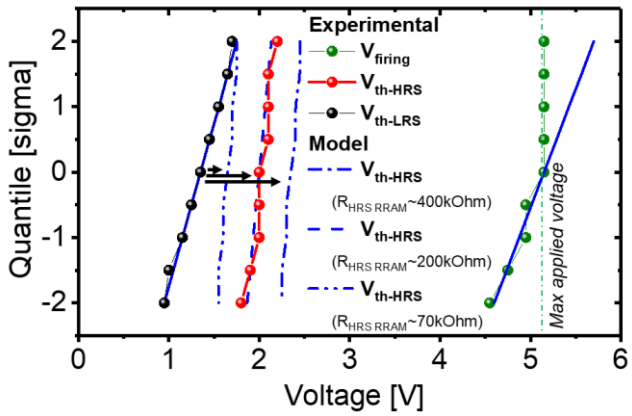

Fig. 8. Distribution of experimental and simulated 1S1R threshold voltages for 10nm GSSN and 10nm HfO_2. $V_{th\text{-}LRS}$ (resp. $V_{th\text{-}HRS}$) is measured for the OxRAM in the LRS (resp. HRS). For V_{firing}>5.2V, longer pulse time at fixed voltage is applied to form the 1S1R. Calculated $V_{th\text{-}HRS}$ distributions take into account OxRAM R_{HRS}.

Moreover, OxRAM R_{HRS} variability leads to read voltage margin reduction due to the resulting $V_{th\text{-}HRS}$ switching voltage dispersion (**Fig.8**), which requires SET and RESET optimization to maximize $V_{th\text{-}HRS}$ and reduce its dispersion over lifetime.

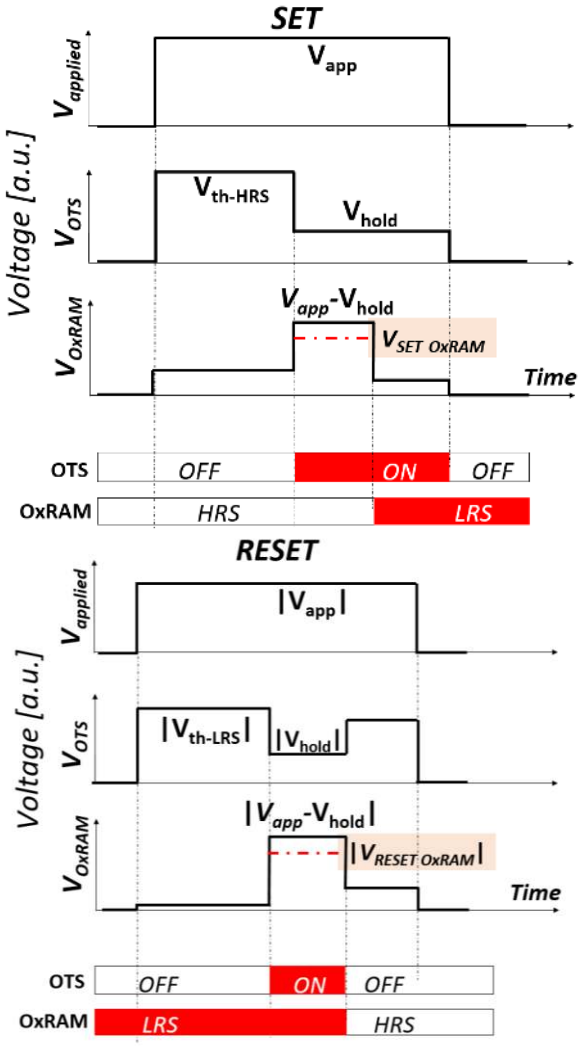

Fig.9. Voltage repartition in 1S1R structures during programming and respective states of OTS and OxRAM during SET and RESET

Once the OTS becomes conductive, V_{hold} drops on the OTS and V_{app}-V_{hold} on the OxRAM (**Fig.9**). It is thus important to control the stack features and programming voltages, so that V_{app}>$V_{th\text{-}HRS}$ and V_{app}>$V_{th\text{-}LRS}$ to efficiently open the OTS, while V_{app}-V_{hold} (voltage that drops on the OxRAM) has to be compatible with a functional operation of the OxRAM: sufficient for a proper programming operation but not too high to prevent device early degradation. **Fig.10 (a)** shows how V_{RESET} seen by the OxRAM (which is a function of V_{app}) affects 1S1R window margin (see **Fig.10 (b)**) and reading yield (probability that $V_{th\text{-}HRS}$>$V_{th\text{-}LRS}$ on the array) at 10^4 operating cycles. In particular, a minimum voltage seen by OxRAM ensures a 1S1R window margin of ~1V while a too high voltage seen by OxRAM device is detrimental for the reading yield.

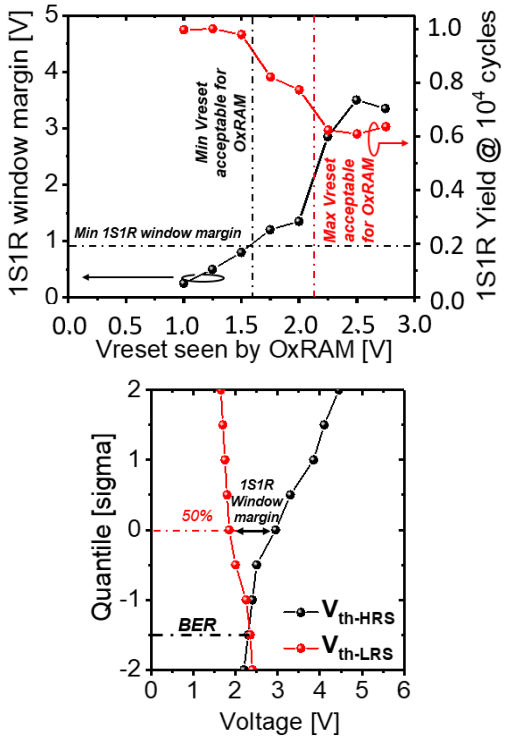

Fig. 10. (a) Calculated 1S1R window margin and reading yield at 10^4 operating cycles' evolution with voltage seen by OxRAM for RESET operation. Reading yield is defined as the probability for V_{th-HRS} and V_{th-LRS} to be distinct so that the resistive state of the device can be read. (b) Illustrative V_{th-HRS} and V_{th-LRS} 1S1R distributions (with intentional poor performances), detailing window margin and BER (=1-yield).

Fig.11 concretizes the tradeoff between 1S1R read margin (calculated from 1R window margin) and maximum measured endurance (with stable window). Up to ~4V 1S1R read voltage margin values can be reached if only 10^3 cycles are needed, and up to 10^7 cycles can be achieved if ~500mV read margin is tolerated.

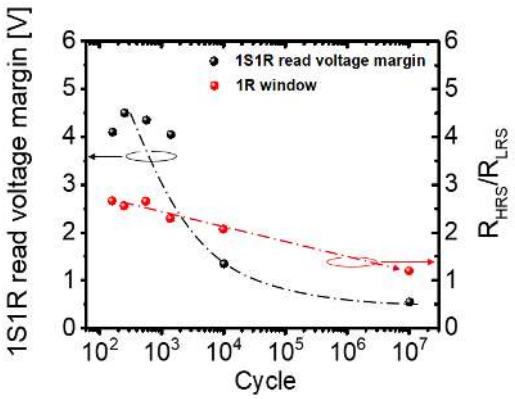

Fig. 11. Evolution of experimental OxRAM window margin (red symbols) as function of maximum number of cycles insuring stable window, and corresponding calculated 1S1R mean read voltage margin (black symbols).

b. 1S and 1R stack influence on read voltage margin

Based on OxRAM endurance, V_{th-HRS} and V_{th-LRS} distributions are calculated from OxRAM R_{HRS} and R_{LRS} statistics for a wide range of V_{SET} and V_{RESET} conditions, allowing to extract 1S1R read margin and BER heatmaps (**Fig.12**). While strong V_{RESET} enlarges 1S1R read window margin, poor endurance with high BER is obtained due to OxRAM early degradation. White dots indicate the voltages the OxRAM undergoes after OTS switching during 1S1R operation for various GSSN thicknesses. Therefore, 10nm and 15nm-thick GSSN co-integration with 5nm-thick HfO_2 ensures reliable read window margin features with no early degradation. Indeed, for >15nm GSSN, BER dramatically increases due to the strong voltage required to open the OTS that degrades the OxRAM after cycling.

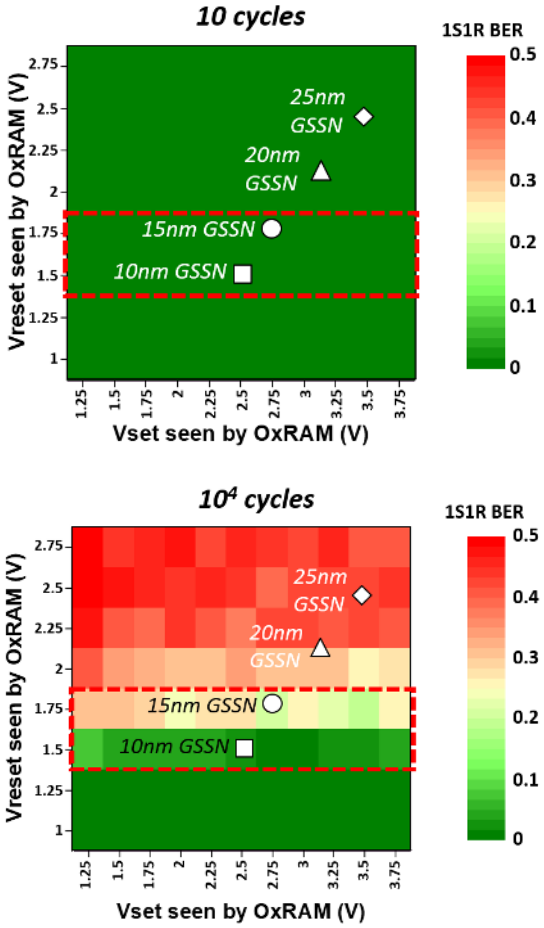

Fig. 12. 1S1R BER evaluation based on SET and RESET programming strategies through cycling (for 100ns pulses). Aggressive RESET strategies lead to excessive voltage drop to OxRAM devices, inducing 1S1R BER early degradation. Fail occurs when V_{th-HRS} <V_{th-LRS}. Symbols illustrate the voltages the OxRAM undergoes after GSSN switches to the ON state, for various selector thicknesses.

c. 1S1R figures of merit on read voltage margin

Based on these analyses, 1S1R figures of merit are proposed. **Fig.13** illustrates the functional SET and RESET operating regions, both to open the OTS and program the OxRAM without degradation (**fig.12**), allowing to adjust GSSN thickness. 10-15nm GSSN appears here to be the functional working range.

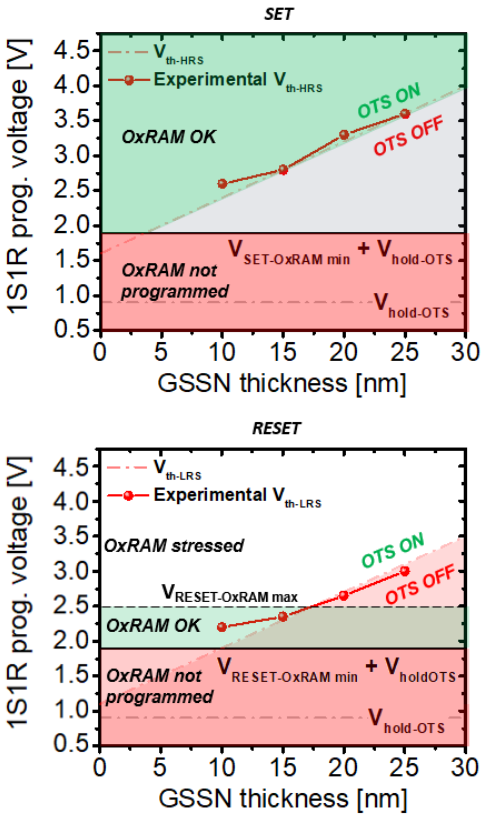

Fig. 13. 1S1R simulated and experimental switching voltage ($V_{th\text{-}HRS}$ and $V_{th\text{-}LRS}$) during SET and RESET. Functional operating regions are highligted where sufficient voltage is provided to both open the OTS and program the OxRAM.

Then, the impact of programming conditions on reading margin is evaluated for 15nm GSSN (**Fig.14-15**). Functional behavior with a stable read margin is achieved for adapted SET and RESET conditions, allowing to reach 10^7 cycles for optimized SET and RESET conditions and optimized GSSN thickness.

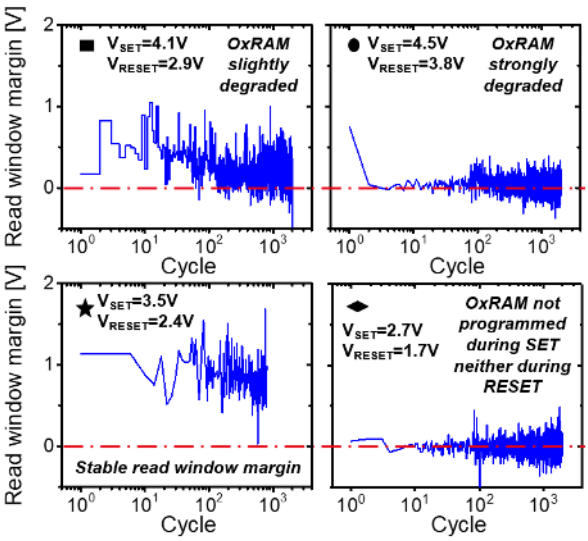

Fig. 14. Evolution of 1S1R read voltage margin over cycling for various programming conditions.

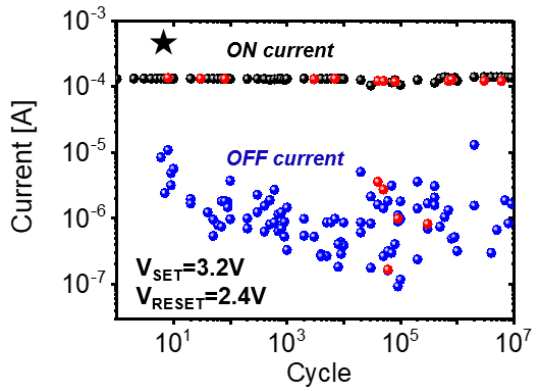

Fig. 15. 1S1R endurance characteristics for adapted programming condition (star condition Fig. 13). Fails are indicated in red.

Fig.16 generalizes the trend and links the programming voltages with 1S1R functionality as a function of OTS V_{th}, based on the minimum and maximum voltages the OxRAM can sustain. Experimental cycling results (from **Fig.14**) are indicated on the graph, confirming the calculated optimized SET and RESET voltages. OTS V_{th} and leakage current being linked [4], the maximum bank size of the 1S1R can also be estimated, as reported on top of the graph.

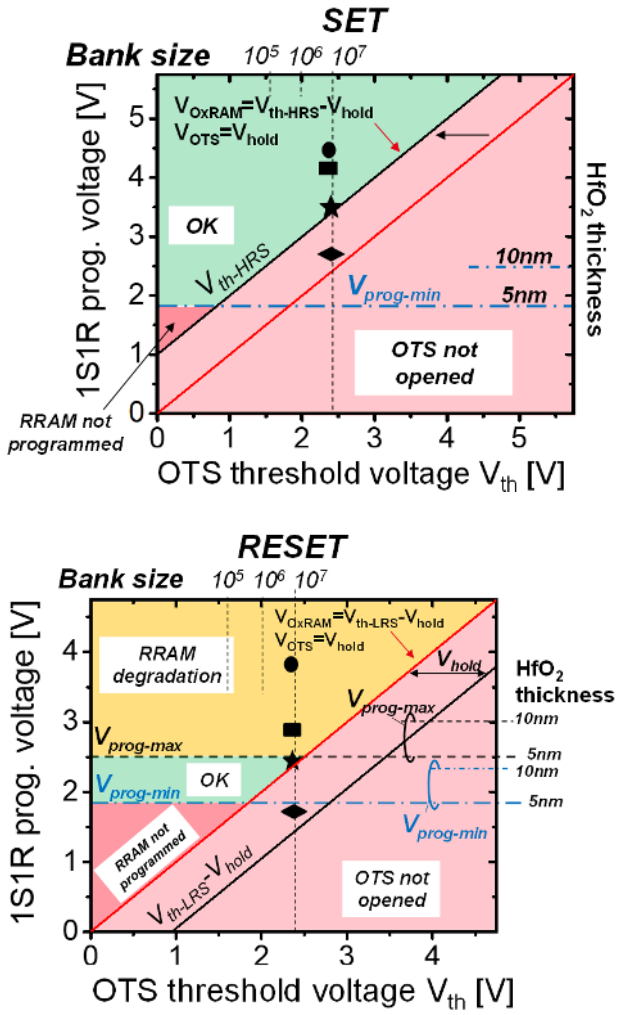

Fig. 16. Functional 1S1R SET and RESET voltages operating regions as function of OTS V_{th}. Functionality ensures OTS opening and sufficient voltage to program the OxRAM preventing device degradation. Symbols correspond to illustrative experimental cases showed in Fig.13.

Finally, **Fig.17** summarizes HfO_2 and GSSN thicknesses dependence to insure a reliable operating region and good overall 1S1R characteristics, including OxRAM integrity, large bank size and acceptable firing voltage.

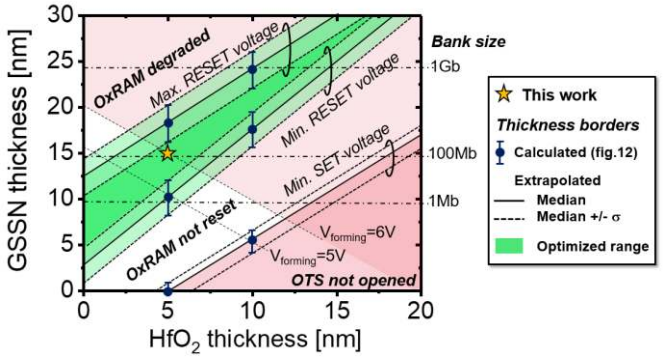

Fig. 17. 1S1R operating regions matching the 1S and 1R stacks, playing with GSSN and HfO_2 thicknesses. Good functionnality is insured when opening the OTS allows to program the OxRAM without degradation. $V_{th\text{-}LRS}$, V_{hold} (simulated, see section B), $V_{th\text{-}HRS}$ (calculated, see section C a)) are used to simulate the operating limits.

IV. Conclusions

1S1R switching operations are clarified by crossing numerical model and semi-analytical simulated results with experimental data. 1S1R dynamical voltage repartition and device degradation are elucidated. We provided general guidelines allowing to design 1S1R stack for optimized read window margin, large maximum array size and extended endurance. It appears that 10^7 programming cycles can be achieved for adjusted SET and RESET conditions and optimized thicknesses of GSSN OTS and HfO_2 OxRAM.

Acknowledgments:

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References:

[1] S. Yasuda et al., "A Cross Point Cu-ReRAM with a Novel OTS Selector for Storage Class Memory Applications," in *VLSI Tech. Dig. 2017, T30-31.*

[2] K. Ohba et al., "Cross Point Cu-ReRAM with BC-Doped Selector", in *Proc. 2018 IEEE IMW.*

[3] G. Molas et al., "Crosspoint Memory Arrays: Principle, Strengths and Challenges", *in Proc. of IMW 2020, pp.1-4.*

[4] D. Alfaro Robayo et al., IEDM 2019 Tech. Dig., pp. 35.3.1-35.3.4.

[5] J. Minguet Lopez et al., Optimization of RRAM and OTS selector for advanced Low voltage CMOS Compatibility", in *Proc. of IMW 2020, pp.1-4.*

[6] A. Verdy et al., "Optimized Reading Window for Crossbar Arrays Thanks to Ge-Se-Sb-N-based OTS Selectors", in *IEDM 2018 Tech. Dig., 37.4.*

[7] J. Sandrini et al., "OxRAM for embedded solutions on advanced node: scaling perspectives considering statistical reliability and design constraints", in *IEDM 2019 Tech. Dig., pp. 30.5.1-30.5.4.*

[8] V. G. Karpov et al., "Field-reduced nucleation in phase change memory", in *Phys. Rev. B 78, 052201 (2008).*