Embedded Decoupling Capacitor Performance in High Speed Circuits

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Abstract

Embedded decoupling is normally considered a better solution than surface mount decoupling for suppressing the switching noise of a high speed digital board/package because of its shorter leads that result in smaller parasitic inductance. This leads to lower impedance over a higher frequency band. It is presumably better in reliability and lowers the cost as well. Designers tend to use large value capacitors for efficient decoupling. Usually, to increase capacitance of an embedded capacitor, one can use a material with higher dielectric constant, design larger electrodes, and reduce the thickness of the dielectric. However, these strategies may sometimes lead to lower performance at high frequency band. This paper will discuss the pros and cons of different embedded capacitor approaches through simulation. As an application example, a typical power/ground network with an embedded capacitor will be compared with that of surface mount discrete capacitor.

1. Introduction

As ICs move towards higher speed/frequency bands, it is hard to design a decoupling network for the suppression of switching noise because most commercial surface mount capacitors work below a few hundreds of MHz. The reason these capacitors operate only at low frequencies is that the equivalent serial inductance (ESL) and resistance (ESR) are high. Usually, ESL is about hundreds of picohenry to nanohenry, which is too large to decouple noise at high frequency band. Embedded capacitors provide a better solution for noise decoupling in power/ground network by introducing small parasitic inductance. The inductances for buried capacitors vary from several to teens of pH depending on the capacitor structure and size. Since embedded capacitor has more advantages in saving room during layout, better reliability, and lower cost, it is being widely investigated by industry and academia [1-5]. Most researchers focus on the material and processing. Some researches explored the design and performance of embedded capacitors for certain applications [5-7]. Croswell [1] at al. reported that using embedded passive devices can reduce PCB area by 44%. However, they did not mention the performance change by replacing the surface-mount decoupling with embedded decoupling. Ulrich [7] et al. studied the embedded capacitors performance in a system through simulation of a equivalent circuit. Their assumptions do not capture the accurate inductance effect of a real embedded capacitor component. This paper will discuss the electric performance of embedded capacitors at system level.

In a PCB/package design, the questions a designer faces are:

1) *How much decoupling capacitance leads to ideal performance?* The value may come from target impedance calculation. Industry generally does not use the exact value from the calculation. For safety reasons, they usually use greater than ten times the capacitance obtained from the calculation. If embedded capacitors will be used, designers need to know how much capacitance does a system really need.

2) *Where should the capacitors be located?* Research shows that the capacitor should be located near the noise source. The closer the chip to the capacitors, the better is the decoupling. Naturally, the ideal location for the embedded capacitor is just underneath the chip.

3) *What is the performance of power/ground network with embedded decoupling capacitors?* The effect of decoupling capacitors in a power/ground network will depend on several factors. A complete system level simulation is needed to quantify this effect.

4) *How to design embedded capacitors in a PCB/package*: The size, shape, and via location strongly affect the embedded decoupling performance. Simulation for the power/ground network with embedded decoupling capacitors is necessary in a design. This paper will address some of these questions through simulation.

2. Simulation Methodology and Experimental Validation

The tool used for the simulation was developed by the author. Derived from Maxwell's equations, or from conventional one-dimensional transmission line equations, two 2-dimensional partial differential equations can be obtained [8]. Using FDFD (Finite Differential Frequency Domain) technique and CG (Conjugate Gradient) algorithm for solving the equations, a fast simulation tool was developed, which can numerically simulate impedance, voltage/current distribution on two-plane networks in any shape, with or without other devices connected. The embedded capacitor used in this study is a planar capacitor of 2×2 cm2 in area. Thicknesses of dielectric material and metal are 12 and 20 μm respectively. Loss tangent of the material is 0.0001. The reason for using lower dielectric loss is to reduce the calculation time. The conducting planes are made of copper with resistivity of 1.69×10-8 ohm m. Frequency region is from 100 KHz to 5 GHz. A 3-D structure of the capacitor is shown in Figure 1.

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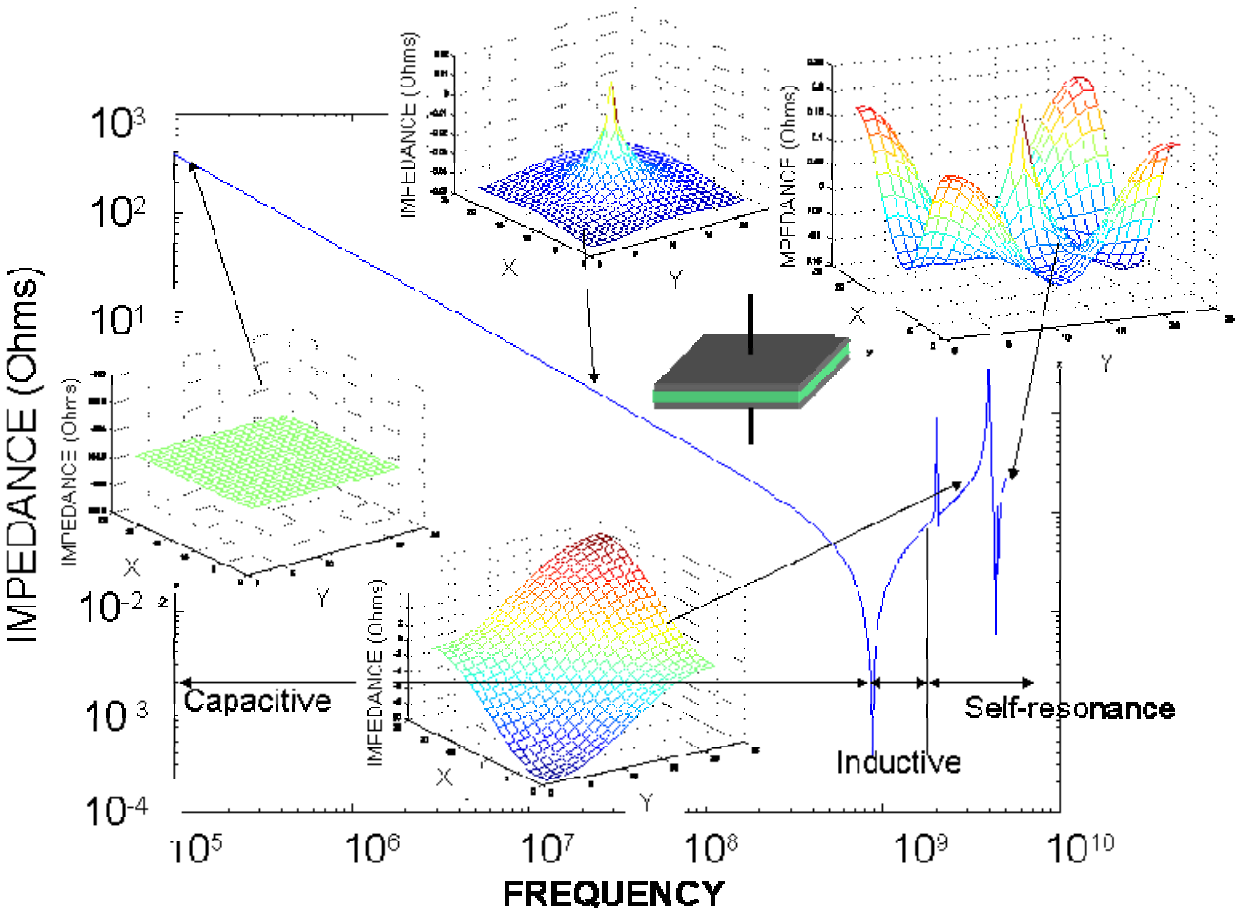


Figure 1: Impedance of a square embedded capacitor varies with frequency. Capacitor area is 2×2 cm^2, dielectric thickness is 12 μm, dielectric constant is 14. Loss tangent is 0.0001. Vias are connected to the center. The simulation neglects metal loss.

A typical embedded capacitor is made of two parallel planes. Between the planes there is a high dielectric constant material. Figure 1 shows a square embedded capacitor, its impedance varying with frequency, and several 3-D voltage distribution plots on the electrode at some particular frequencies. It is clear that the capacitor resonates at 850 MHz. Below the frequency, the impedance is capacitive and the embedded capacitor is an actual capacitor. Beyond the resonant frequency and within the first self-resonant frequency, the impedance becomes inductive. In this band, the embedded capacitor acts like an inductor. Above the first self-resonant frequency, the embedded capacitor acts like a resonator. The impedance could be either inductive or capacitive. Therefore, the first resonant frequency is the upper limit of frequency for the capacitor. Below the self-resonant frequency band, the planar embedded capacitor can be equivalent to an inductor and a capacitor connected in series. The resonant frequency can be calculated by $f_0 = \frac{1}{2\pi\sqrt{LC}}$. The capacitance can be evaluated by: $C = \varepsilon_r \varepsilon_0 \frac{A}{h}$, where A is the area of electrode and h is the thickness of the dielectric material. To obtain the inductance analytically is much tougher. The most common equation for estimating inductance is: $L = \mu_0 \frac{hl}{w}$, where l and w are the length and width of the plates, and h is the separation. It is incorrect to use this equation to evaluate the inductance of an embedded capacitor, because the equation assumes that current flow is uniform. Actually, the current is zero at the boundary of electrodes. The inductance of an embedded capacitor not only depends on the structure, geometry and size but also on the position of connection of via/though hole, as discussed in the later part of this paper. It is possible to estimate the impedance for a simple feature such as circular electrode. The impedance of a circular planar capacitor with center connection is:

$$Z = \frac{Z_0}{2\pi a\left[J_1(\gamma a)Y_1(\gamma b) - J_1(\gamma b)Y_1(\gamma a)\right]\left[J_0(\gamma a)Y_1(\gamma b) - J_1(\gamma b)Y_0(\gamma a)\right]} \quad (1)$$

where Z_0 is the characteristic impedance of the pair of conductor planes, a is a radius of center connect, b is the radius of circular plane, J and Y are the first and second kind of Bessel functions respectively, and γ is the constant of wave propagation in the dielectric material between the conductor planes.

3. Experimental validation

Figure 2 shows the results from above equation and measurement. A circular electrode embedded capacitor was made with a nanocomposite having a dielectric constant of 18, thickness of 12 µm, and electrode radius of 220 mils. 2-port measurements were used because they show very little error up to several GHz [9-10]. The results match well at low frequency band. However, the measured result has lower resonant frequency than the calculated result. The difference may come from: 1) The connection of the capacitor. The probe position is much different from the assumptions in the calculations. The probe is GS type, and the pitch is 1000 µm. The G tip touches the bottom electrode at the center while the S tip touches the top electrode at 1000 µm away from the center. On the other hand, the calculation assumes that both electrodes are connected to the center; 2) The improper calibration of probe. Standard calibration kit may cause incorrect compensation in the Vector Network Analyzer (VNA); 3) Other unknown inductance from non-plane contact of probe, and 4) Loss from dielectric material and metal. To obtain the impedance of embedded capacitors with other shapes, numerical method may be the only way.

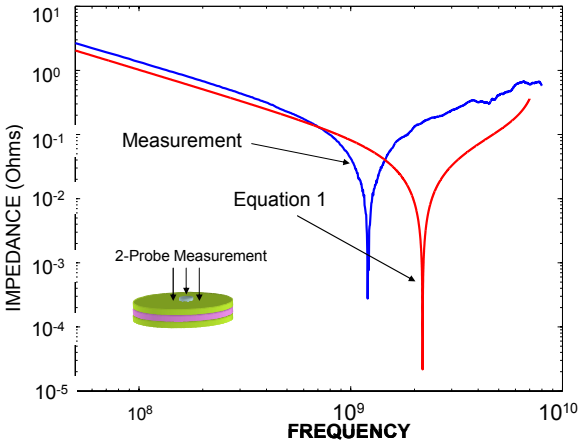


Figure 2: Impedance of a circular embedded capacitor. The electrode radius is 5.6 mm, connection radius is 0.53 mm, thickness of dielectric 12 µm and dielectric constant 18

4. Simulation Results and Discussion

The above discussed simulation tool will now be used for parametric studies. The important parameters a designer encounters in a power network design will be considered in these simulations.

Material dielectric constant

Using high dielectric constant material can reduce the impedance at low frequency while the resonant frequency shifts to low frequency band. Figure 3 shows the comparison of impedances of embedded capacitors with different dielectric constant. All geometry features of the capacitors are same. The parasitic inductance depends on the structure of the capacitor instead of the dielectric material. Therefore, the resonant frequency is only dominated by the capacitance. From this figure, it is obvious that reducing the impedance at low frequency by using high dielectric constant material will push the first resonant frequency to low frequency band. This will lead to performance loss at high frequency band. On the other hand, to increase high-frequency performance, reducing the inductance by reducing the size of electrode will decrease the capacitance which increases the impedance at low frequency and the loss of performance at low frequency band. Therefore, there is trade-off for embedded capacitors: it is either large capacitance working at low frequency band or small capacitance at high frequency band. It is hard to get them both.

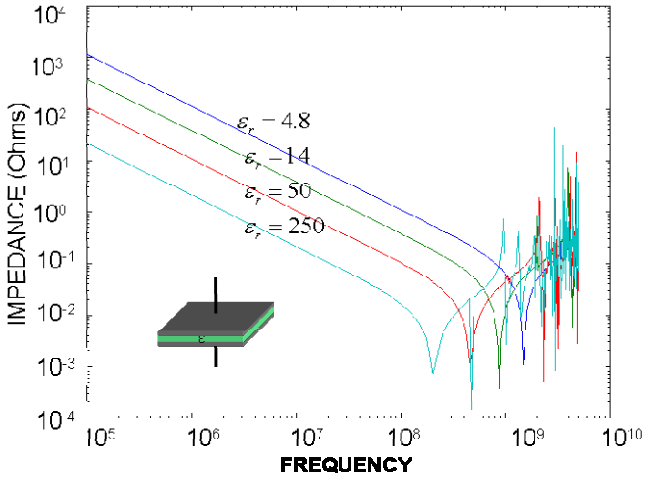


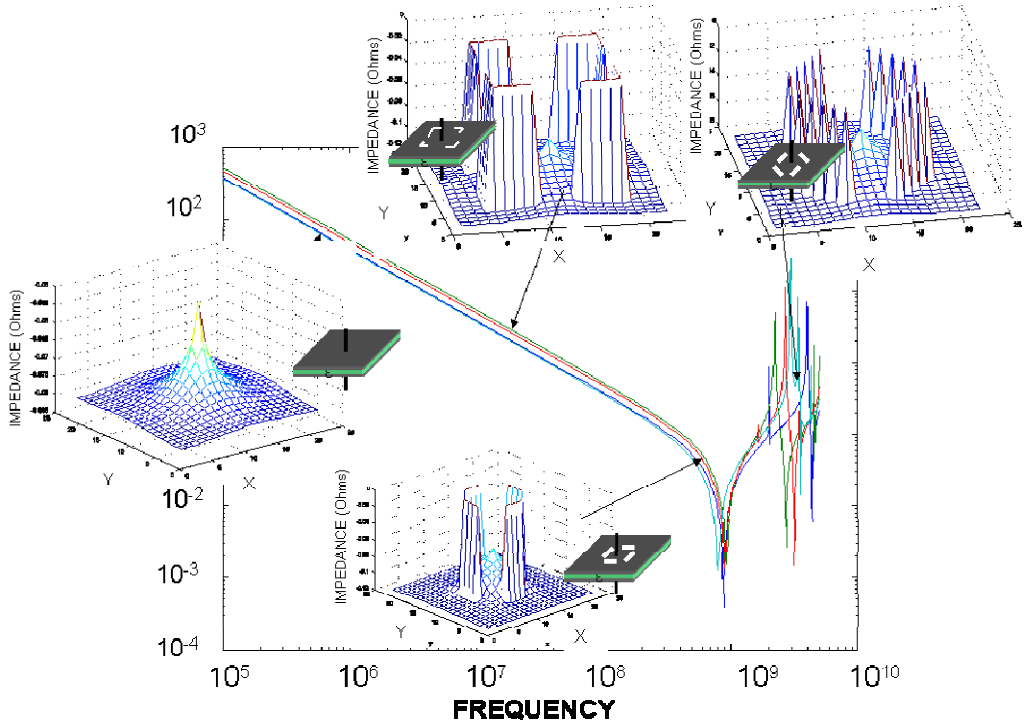
Figure 3: Impedance comparison for materials with different dielectric constants.

Electrode patterning

Cutting slots on electrode can change embedded capacitor property. Since the slots change the current path on the electrode, the parasitic inductance of the embedded capacitor will be changed. However, the slots can be so narrow that the capacitance does not change too much. Figure 4 shows simulated impedances of three embedded capacitors with differently patterned electrodes. A simulation of un-patterned capacitor and 2-D voltage distributions of the patterned electrodes for different designs (at 450 MHz) are also shown in the same figure. This can help to understand how the voltage/current distributes on the patterned electrode. From the figure, it is clear that cutting slots blocks a part of the current path, so that the current density on the un-blocked area is higher, which increases the voltage drop in the area. Patterning the electrode can slightly move the first resonant frequency to either higher or lower frequency depending on the slot design. Large impedance change occurs in the self-resonant region. The slot changes the boundary condition of electrode resulting in changes in the resonant mode.

Via location on the capacitor electrodes

To connect the embedded capacitors to a power/ground network, blind vias or through holes can be located on side, corner, or center of the planar electrode. Generally, the inductance of an embedded capacitor depends on the location of the connection. It is larger when the location is on corner or



. Figure 4: Patterned electrode can change the first resonant frequency slightly, and the self-resonant frequencies

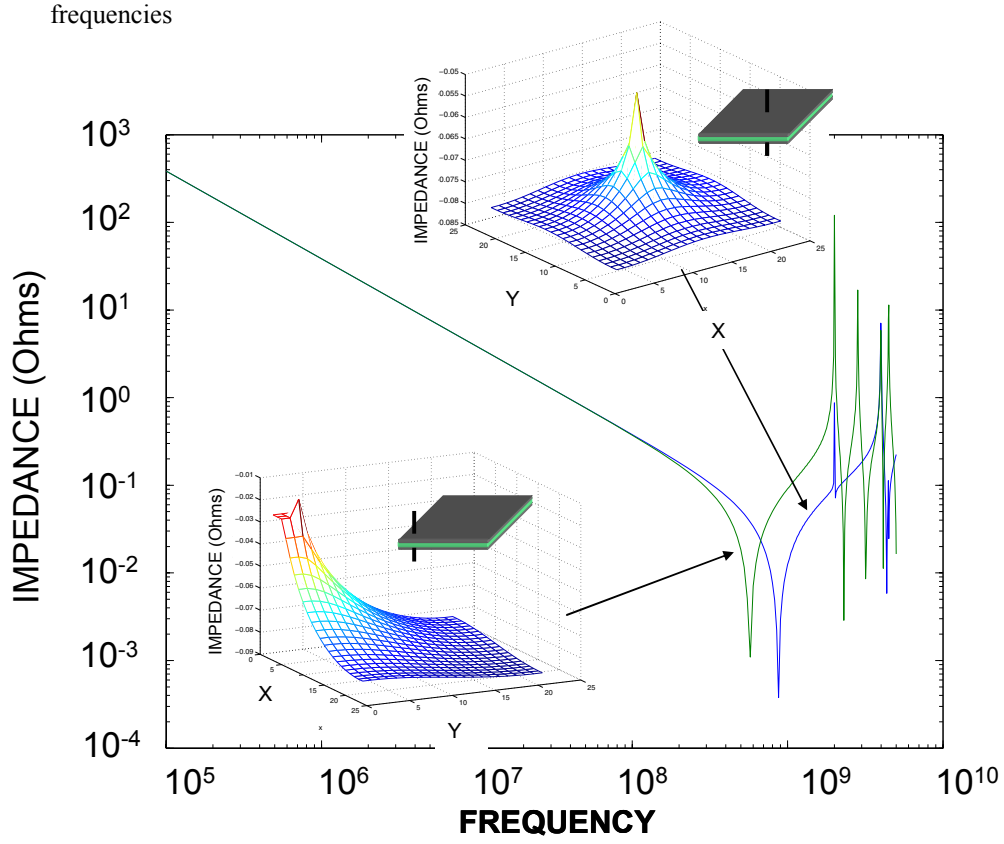


Figure 5: Impedance comparison of an embedded capacitor with connections at center (case 1) or corner (case 2).

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side than that on center. Figure 5 shows this comparison for a planar embedded capacitor. The resonant frequency of the capacitor with a corner connection is lower than that with a center connection. Since the capacitance of both connections is same, the inductance with corner connection is larger than that center connection. Beyond first resonant frequency point and below the self resonant frequency (in the inductive region), the measured slope is larger for the capacitor with corner via compared to that with center via. This also implies that the inductance of corner connected via is larger than that of center connected via. Two 2-D voltage distributions on the electrode are shown in the same figure. From this, a longer current path on the electrode with corner connected via can be observed. Longer current path leads to larger inductance within the structure which lowers the decoupling performance.

Comparison between embedded and SMT capacitor in a system

To compare the effect of embedded and SMT discrete decoupling capacitors, a power/ground network of a typical package is investigated. It has two 4×4 cm^2 solid planes with separation of 60 μm. The dielectric constant of the material between the planes is 4.8. A chip of 0.8×0.8 cm^2 is assumed on the center of the package with a connection to power/ground network at the center. In case 1 (embedded decoupling), four embedded capacitors are included in the package. The equivalent circuit of the capacitor has a capacitance of 1.2 nF and inductance of 0.21 nH including via's/through hole's inductance. They are located under the chip. For case 2 (surface mount decoupling), four surface mount capacitors of 0.01 μF, and 0.47 nH, including via/through hole's inductance, are assumed around the die. Power/ground network with no decoupling is simulated as a third case. The simulated results without any decoupling capacitors are also shown in Figure 6. Simulation show a resonant frequency around 1.48 GHz in the power/ground network. The figure shows that adding embedded capacitors or SMT capacitors result in the resonant frequency moving to lower frequency band. The curves show that surface mount capacitors have lower impedance at low frequency band. For the high frequency band, embedded capacitors achieve lower impedance than surface mount capacitors. A result of combination of both kinds of capacitors is shown in the figure as well. Combination of embedded and surface-mount decoupling takes advantages of both capacitors. It is interesting that if the package is designed to work around 1.48 GHz, no decoupling capacitors would be needed for this power-ground network. Since the impedance is lower than that with embedded/SMT capacitor connected, any extra decoupling capacitor would make the performance worse at this frequency region. However, if the package will work below 300 MHz, the decoupling capacitors should be introduced. To design a decoupling network, the power/ground network has to be taken into account, and the value of capacitors (no matter embedded or SMT) is not "the larger the better". It depends on the power/ground network, frequency band, current, voltage and noise tolerance.

5. Conclusions

Different embedded decoupling configurations were simulated using a novel method. The effect of the capacitor dielectric constant, via location and other design modifications were analyzed through the simulation. The conclusions from the analysis are:

- Like a normal capacitor, embedded capacitor can be equivalent to a L-C-R serial circuit in a certain frequency band. It may act as an inductor if frequency increases beyond the first resonant frequency. At higher frequencies, the embedded capacitor acts like a resonator. Depending on frequency, impedance can be either capacitive or inductive.

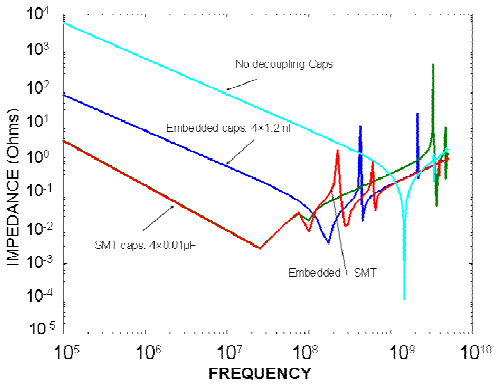

Figure 6: Performance comparison of embedded and surface mount capacitors. The figure also shows performance without decoupling and with both types of decoupling.

- Inductance of an embedded capacitor depends not only on the electrode geometry, size, feature, etc, but also on the connection of via/through hole. Corner or side connection on electrode will result in larger inductance than the center connection.
- High dielectric constant ε_r can reduce the impedance of embedded capacitor at low frequency band, while it shifts the first resonant frequency to low frequency band, and then lowers the performance at high frequency. It means, to decouple high frequency noise, small electrode and high ε_r should be used. Large area of electrode can increase both capacitance and inductance. It should not be used to decouple high frequency noise.
- Patterned electrode does not affect the impedance at low frequency band but affects the self-resonant region. It could be used for higher order harmonic frequency decoupling.
- From system point, embedded and surface mount capacitors can achieve low impedance in the low frequency band while pushing the first resonant frequency of the power/ground network to low frequency band. This will degrade the performance of the system at high frequency band. Increasing capacitance by using large ε_r material does not help to reduce the impedance at high frequency band unless appropriately designed. Power/Ground network plays a critical part on the high

frequency band. To design an efficient decoupling network, power/ground network, current, voltage, noise tolerance, connection position, and frequency have to be taken into account.

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