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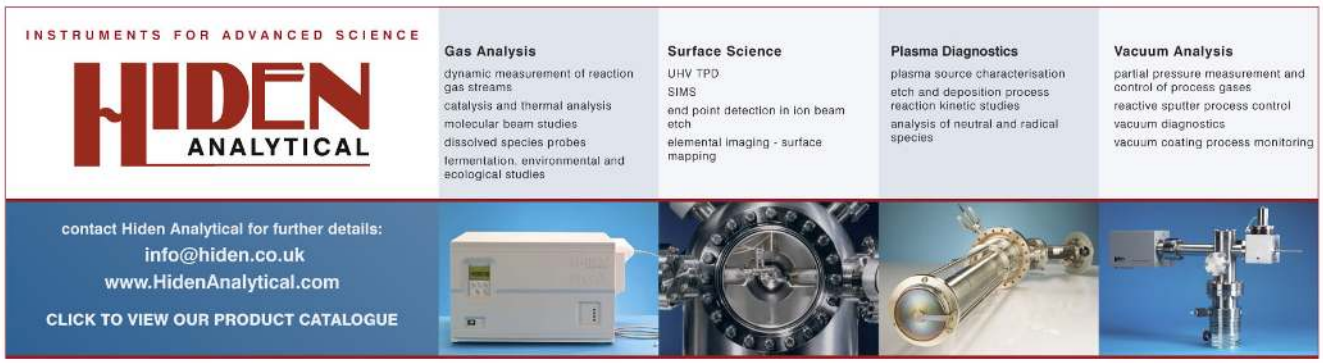

Embedded-gate graphene transistors for high-mobility detachable flexible nanoelectronics

Jongho Lee,[1] Li Tao,[1] Yufeng Hao,[2] Rodney S. Ruoff,[2] and Deji Akinwande[1,a)]
[1]*Electrical and Computer Engineering, The University of Texas, Austin, Texas 78758, USA*
[2]*Mechanical Engineering and the Materials Science and Engineering Program, The University of Texas, Austin, Texas 78758, USA*

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A high-mobility graphene field-effect transistor with embedded gate was fabricated on smooth spin-coated polyimide films. Electrostatic transport measurements reveal a maximum electron and hole mobility of 4930 $cm^2/V\,s$ and 1130 $cm^2/V\,s$, respectively. Temperature dependent measurements indicate that carrier transport is not limited by intrinsic mechanisms but by charged impurities, surface roughness, and defects, suggesting that further increases in mobility are possible. The measured carrier mobilities are the highest reported for graphene transistors on polymeric substrates and hence enable high-speed devices for flexible electronics from graphene grown by size-scalable chemical vapor deposition. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.3702570]

Very fast carrier transport is one of the main attributes of monolayer graphene field-effect transistors (GFETs), an enabling feature for high-speed nanoelectronics.[1] Intrinsically, carrier mobilities approaching 100 000 $cm^2/V\,s$ have been observed at room temperature on suspended devices.[2] The carrier mobility degrades on oxide supported GFETs, with values around 10 000 $cm^2/V\,s$ frequently measured on clean exfoliated graphene on SiO_2 in agreement with theoretical upper limits.[3–5] However, it is unclear how fast charge carriers can travel in monolayer graphene on polymeric substrates, an important substrate for flexible electronics. It has been suggested that remote phonon scattering from the broad continuum of modes from the polymer substrate should impact the carrier mobilities at a scale comparable to SiO_2.[6] As graphene holds great potential for fast flexible electronics,[7,8] it is imperative to experimentally access its fast carrier transport on polymer supports.

In this letter, we report embedded-gate graphene field-effect transistors (EGFETs) realized from chemical vapor deposited (CVD) graphene with maximum carrier mobilities of 4930 $cm^2/V\,s$ and 1130 $cm^2/V\,s$ for electrons and holes, respectively. The electron mobility is comparable to peak mobilities observed for CVD graphene devices on oxidized Si with high-k dielectrics,[9] indicating that the fast carrier transport observed on SiO_2 supports is also accessible on polymeric substrates. Temperature dependent measurements on the fabricated devices indicate that charge impurity or defect scattering limits carrier transport rather than phonon scattering from the substrate. Hence, further improvement in mobility should be possible on at least some polymeric substrates as the quality and transfer of CVD graphene continue to improve. The carrier mobilities reported here are the highest observed to date for organic and carbon based transistors on flexible substrates,[10,11] potentially enabling high-speed flexible nanoelectronics.

High quality monolayer graphene was synthesized by a low-pressure chemical vapor deposition (LPCVD) method on evaporated 500-nm thick copper film on a 285-nm thick thermal oxide grown on a single-crystal silicon substrate. LPCVD on Cu-coated substrates in a vertical cold-wall chamber with independent showerhead and substrate heaters yielded monolayer graphene. The sample was first annealed in a hydrogen environment for 5 min at 1000 °C, followed by exposure to methane at the same temperature. The ultra-high purity (99.999%) methane was typically flowed at 5–10 sccm for 5 min. After growth, the chamber was cooled below 180 °C before removal of the sample. Raman spectroscopy verified high-quality monolayer graphene with the following characteristics as shown in Fig. 1(a): (i) the full width at half maximum (FWHM) of the 2D-peak is $\sim 32\,cm^{-1}$, (ii) the 2D/G intensity ratio is 2.5–3, and (iii) the D-peak intensity is small or negligible. The conventional wet-transfer process with poly(methyl methacrylate) (PMMA) coated on graphene[12] was employed to transfer graphene from the Cu-coated substrate onto a polyimide (PI) coated substrate.

Liquid polyimide (PI-2574 from HD Microsystems) was spin-coated on a 50-nm thick plasma-enhanced chemical vapor deposited Si_3N_4 sacrificial layer on silicon. The 15 μm-thick spin-coated PI affords a smooth surface with root-mean-square (RMS) roughness of <1 nm as shown in Fig. 1(b). After device fabrication, the sacrificial layer is etched to release the free-standing flexible film. The PI coated film is soft-baked at 200 °C for 30 min and subsequently cured at 300 °C for 1 h under a nitrogen atmosphere. Its high glass transition temperature (>300 °C) and high chemical resistance make it a suitable material for flexible electronics and is compatible with standard microelectronic device fabrication.[13]

The device fabrication process is illustrated in Fig. 2(a). In brief, an array of gate electrodes were patterned on a PI-coated silicon substrate by electron-beam lithography, evaporation, and liftoff. A high-k dielectric of 20-nm thick Al_2O_3 is deposited by atomic layer deposition (ALD); the estimated

a)Author to whom correspondence should be addressed. Electronic mail: deji@ece.utexas.edu.

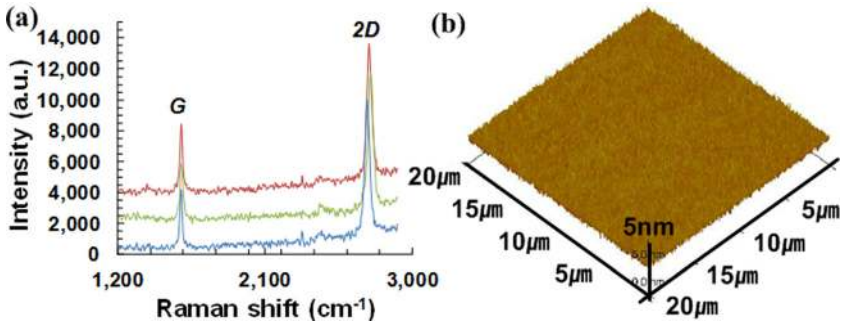

FIG. 1. (a) Representative Raman spectra of monolayer graphene used for device fabrication. Raman spectra were taken with a 442 nm blue laser at three locations of the synthesized graphene on evaporated Cu film directly before transfer. (b) 3D AFM image of cured polyimide surface with surface roughness <1 nm.

gate-oxide capacitance (C_{ALD}) measured from a test capacitor structure on the same substrate is about 179 nF/cm^2. A CVD grown graphene film from a Cu/SiO_2/Si growth substrate was then transferred via a conventional wet-transfer process using ammonia persulfate to etch the copper.[12] Oxygen plasma reactive-ion-etching (RIE) was used to pattern the active channel region while removing the superfluous graphene and ensuring channel isolation. Source and drain electrodes were defined to complete the device fabrication. The gate and source/drain metals are Ni/Au (10 nm/40 nm) and Ni (50 nm), respectively. Finally, buffered oxide etchant (BOE 6:1) was used to strip the Si_3N_4 sacrificial layer and release the flexible polyimide film from the underlying silicon substrate.

Atomic force microscope (AFM) images of the graphene area on the sample after complete device fabrication are shown in Fig. 3. The RMS surface roughness over the scanned area is 4.25 nm; the high peaks and roughness are the result of the residual resist during graphene transfer and film release. The highlighted rectangle in Fig. 3(a) is a relatively smooth local graphene area having a surface roughness of 1.9 nm. The complete removal of chemical residue is crucial for obtaining high performance transistors since the residue is detrimental to charge transport and motivates the need for cleaner transfer and fabrication methods, a pressing matter that is currently a focus of further research.[14,15]

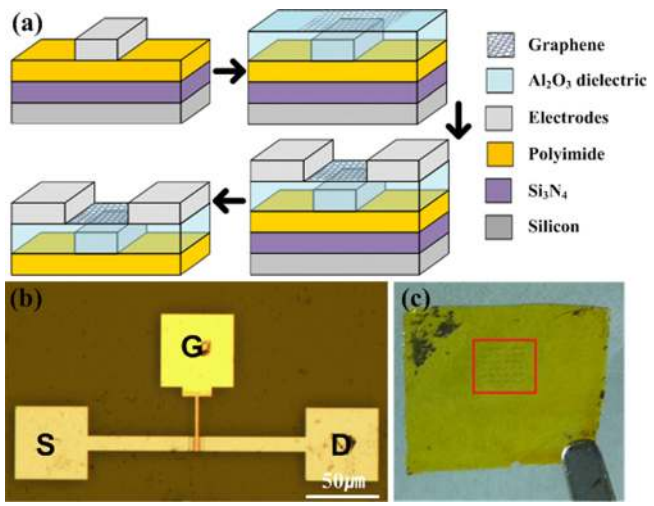

FIG. 2. (a) Illustration of the EGFET fabrication process on spin-coated PI on a Si_3N_4/Si substrate. (b) Optical image of a completed EGFET. The device length and width are 4 and 8 μm, respectively. (c) Photograph of the flexible substrate with an array of EGFETs. The highlighted square shows the array of devices.

Electrostatic measurements performed under ambient conditions are presented in Fig. 4. Unintentional charge doping of graphene during the wet-transfer process[14] and metal-induced doping from high work-function metals[16] are most likely responsible for the shift of the Dirac voltage to 2.7 V. A well accepted diffusive transport model[17] shows good agreement with the experimental data and is employed to extract key device parameters. From the data in Fig. 4, the extracted electron and hole mobilities are 4930 cm^2/V s and 1130 cm^2/V s, respectively. These values are significantly higher than the previously reported GFET mobilities on flexible substrates[7,8,18] and are comparable to the highest mobility values for CVD graphene on SiO_2/Si substrates.[9,19–21]

The temperature dependence of the EGFET device parameters is shown in Fig. 5. After the initial measurements, the Dirac point of the sample shifted to over 6 V due to prolonged exposure to the ambient. Before performing the temperature measurements, the sample was kept under ultra-high vacuum ($<10^{-8}$ Torr) for over 72 h in order to recover its initial Dirac point. Figure 5 shows the temperature dependence of the key parameters: impurity concentration, mobility, and contact resistance (R_c).

As shown in Fig. 5(a), the source-drain current slightly increases as the temperature more than tripled from 78 to 300 K. At the Dirac point, current is largely determined by the transport of the (voltage-independent) residual charge concentration consisting of (i) the intrinsic thermally generated carriers which scales quadratically with temperature[22] and (ii) the impurity carrier density from unintentional doping which is largely temperature independent in the thermal range of interest investigated here and corroborated by the experimental profile shown in Fig. 5(b). The weak temperature dependence (<15%) at the Dirac point indicates that the impurity carrier density is mostly responsible for charge transport at the Dirac point. Indeed, the extracted impurity density ($\sim 1.3 \times 10^{12}$ cm^{-2}) is almost an order of magnitude

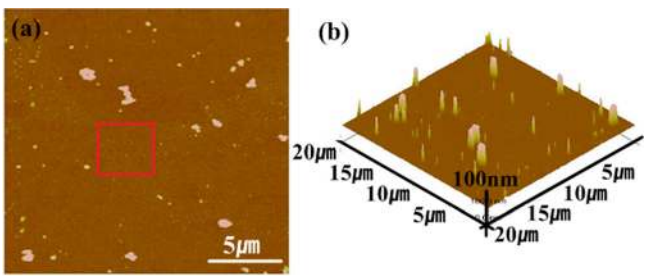

FIG. 3. AFM images of monolayer graphene after device fabrication. (a) 20 μm × 20 μm scan, and (b) 3D image of the scanned area. The surface roughness of the highlighted rectangle is 1.9 nm.

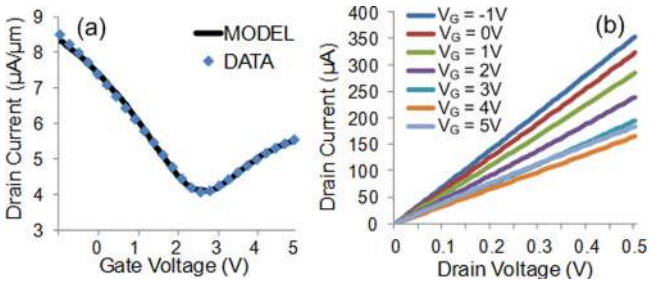

FIG. 4. Experimental current–voltage characteristics of the EGFET. (a) I_D-V_G profile with extracted electron and hole mobilities of 4930 cm^2/V s and 1130 cm^2/V s, respectively. $V_D = 100$ mV. (b) I_D-V_D curves showing linear relation.

larger than the intrinsic thermal carrier density ($\sim 1.6 \times 10^{11}\,cm^{-2}$) at 300 K, further supporting this assertion. The relatively high impurity density is an undesired outcome of unintentional doping from polymer residue during graphene transfer and device fabrication.[14,15] We are presently exploring several experimental routes for improved processing to overcome the high impurity doping that obscures the inherent graphene device physics.

The electron and hole carrier mobility show opposite dependence on temperature. The hole mobility can be interpreted as relatively flat or marginally decreasing with temperature. The weak dependence on temperature is a reflection of carrier scattering that is dominated by (charged or neutral) impurity scattering which is in contrast to phonon scattering that increases strongly with rising temperature and yields a proportional decrease in mobility. However, the electron mobility shows an increase with temperature particularly above 200 K, an unexpected result that has not been previously reported for GFETs. This is most likely due to Coulomb scattering from the large charge impurity density ($\sim 1.3 \times 10^{12}\,cm^{-2}$) that more strongly interacts with

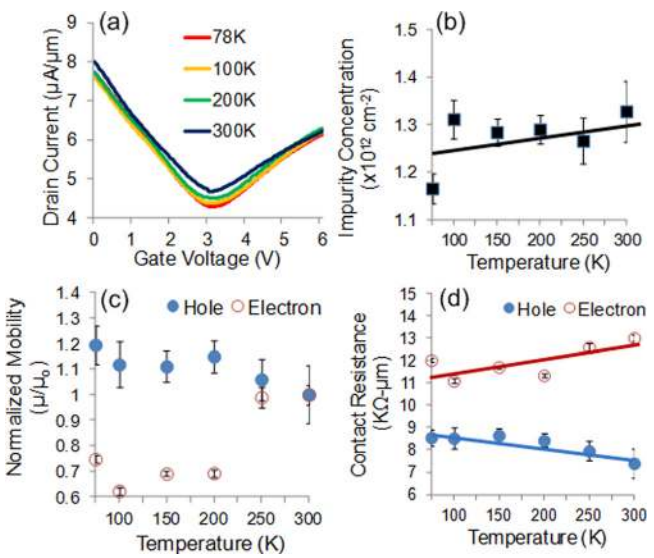

FIG. 5. Temperature-dependent device characteristics. (a) ID-VG response. The initial and final measurements at 300 K are identical indicating reliability of the measurements. (b) Charge impurity density, (c) mobility normalized to the 300 K value (μo), and (d) contact resistance dependence on temperature. The contact resistance reported here is the total contribution from the source and drain contacts. μo is the reference mobility at 300 K.

electron transport in graphene. Our hypothesis is in line with conventional semiconductor device physics where a mobility increase with temperature is observed for high doping densities and is understood to result from ionized impurity scattering that grows stronger with decreasing temperature owing to the decreased thermal velocities and screening effect.[23–25] The temperature dependency of the screening effect has previously been generally analyzed for graphene on SiO_2 substrates and shown to exhibit a complex behavior that impacts the carrier transport temperature profile.[23] Further detailed studies are needed to shed light on the interaction of the charged impurities with graphene electrons and the specific conditions that result in mobility increase with temperature for the device structure reported here (GFET on Al_2O_3/PI substrates). Nonetheless, we can conclude that the carrier mobility of the EGFET is not limited by the intrinsic phonon scattering suggesting that higher mobilities are possible for flexible nanoelectronics.

The high contact resistance (including both source and drain contact contributions) seen in Fig. 5(d) reflects the poor metal graphene interface that likely includes a thin polymer interface of ~1.9 nm, evidenced by the surface roughness in Fig. 3. The asymmetry in R_c is a result of the high work-function metal contact (Ni) which affords a more transparent interface (p-p) for hole transport in contrast to electron transport that involves a p-n junction interface, hence an additional contribution to the contact resistance.[26,27] Overall, drift-like behavior mostly accounts for electron transport at the metal-graphene interface resulting in the observed contact resistance increase with temperature (Fig. 5(d)). The ~13% increase in the electron R_c compares well with the ~20% increase reported for much lower contact resistance devices made from exfoliated graphene.[28] In contrast, the hole R_c exhibits a slight decrease with increasing temperature suggesting that thermionic or thermionic-field tunneling,[29] across a barrier (e.g., the thin polymer interface mentioned earlier) is a significant transport mechanism. However, the very weak temperature dependence (differences are within the measurement/extraction uncertainty) might be due to the near cancellation of the temperature dependence of two competing mechanisms including thermionic and drift-like transport, where the former and latter increase and decrease with temperature, respectively.

In conclusion, we have achieved record mobilities of 4930 cm^2/V s and 1130 cm^2/V s, respectively, for electron and hole transport in graphene transistors with high-k dielectrics on polyimide sheets. The device physics have been elucidated indicating further improvements in charge transport is achievable with better fabrication processes. Our work reveals that graphene electrical devices on polymeric substrates are promising for high-speed flexible electronics.

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