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# Embedded Micromechanical Devices for the Monolithic Integration of MEMS with CMOS

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Abstract

Recently, a great deal of interest has developed in manufacturing processes that allow the monolithic integration of microelectromechanical structures (MEMS) with driving, control, and signal processing electronics. This integration promises to improve the performance of micromechanical devices as well as the cost of manufacturing, packaging, and instrumenting these devices by combining the micromechanical devices with an electronic sub-system in the same manufacturing and packaging process. For example, Analog Devices has developed and marketed an accelerometer[1] which illustrates the viability and commercial potential of this integration. They accomplished this task by interleaving, combining, and customizing their manufacturing processes which produce the micromechanical devices with the processes that produce the electronics. Researchers at Berkeley[2] have developed a modular integrated approach in which the aluminum metallization of CMOS is replaced with tungsten to enable the CMOS to withstand subsequent micromechanical processing.

In order to maintain the modularity of the Berkeley approach but overcome some of the manufacturing challenges of their CMOS-first approach, we are developing a MEMS-first process. This process places the micromechanical devices in a shallow trench, planarizes the wafer, and seals the micromechanical devices in the trench. These wafers with the completed, planarized micromechanical devices are then used as starting material for a conventional CMOS process. At Sandia, both 2 μm and 0.5 μm CMOS technologies are available for integration; although, the 2 μm process is being used as the development vehicle for the integrated technology. Since this integration approach does not modify the CMOS processing flow, the wafers with the subsurface micromechanical devices can also be sent to a foundry for CMOS processing. Furthermore, the topology of multiple polysilicon layers does not complicate CMOS lithography.

Figure 1 is a schematic cross-section of our integrated technology. A shallow trench (~ 6 μm) is etched in (100) silicon wafers using a KOH etchant. A silicon nitride film is deposited to form a dielectric layer on the bottom of the trench. Sacrificial oxide and multiple layers of polysilicon are then deposited and patterned in a standard surface micromachining process. The shallow trenches are then filled with a series of oxide depositions and planarized with chemical-mechanical polishing (CMP). The entire structure is then annealed to relieve stress in the structural polysilicon and sealed with a silicon nitride cap. Conventional CMOS processing is performed. Additional masks are used at the end of the process to open the nitride cap over the micromechanical layer for metal contact to polysilicon studs and for release of the micromechanical structures.

Figure 2 shows a released accelerometer fabricated in a trench. Figure 3 is a close-up view of the polysilicon interconnects on the bottom of the trench leading to the polysilicon stud that connects to the CMOS metal. In order to provide contact between the micromechanical devices and the CMOS, the depth of the trench is sized so that the top of the polysilicon stud lies just below the top of the planarized trench. Figure 4 shows a cross-sectional view of a trench that has been refilled and planarized using CMP.

This integrated process is being evaluated using a mask set that contains accelerometers, combustible gas detectors, lateral resonators, test structures, and their CMOS drivers. The fabrication of devices using this process along with the performance of the CMOS driving electronics will be presented. Additionally, the results of three-level (plus ground plane) polysilicon structures built using this same trench technology will be presented.

References

[1] W. Kuehnel and S. Sherman, "A surface micromachined silicon accelerometer with on-chip detection circuitry", *Sensors and Actuators A*, vol. 45, no. 1, pp. 7-16 (1994).
[2] W. Yun, R. Howe, and P. Gray, "Surface micromachined, digitally force-balanced accelerometer with integrated CMOS detection circuitry", *Proc. of the IEEE Solid-State Sensor and Actuator Workshop '92*, p. 126 (1992).

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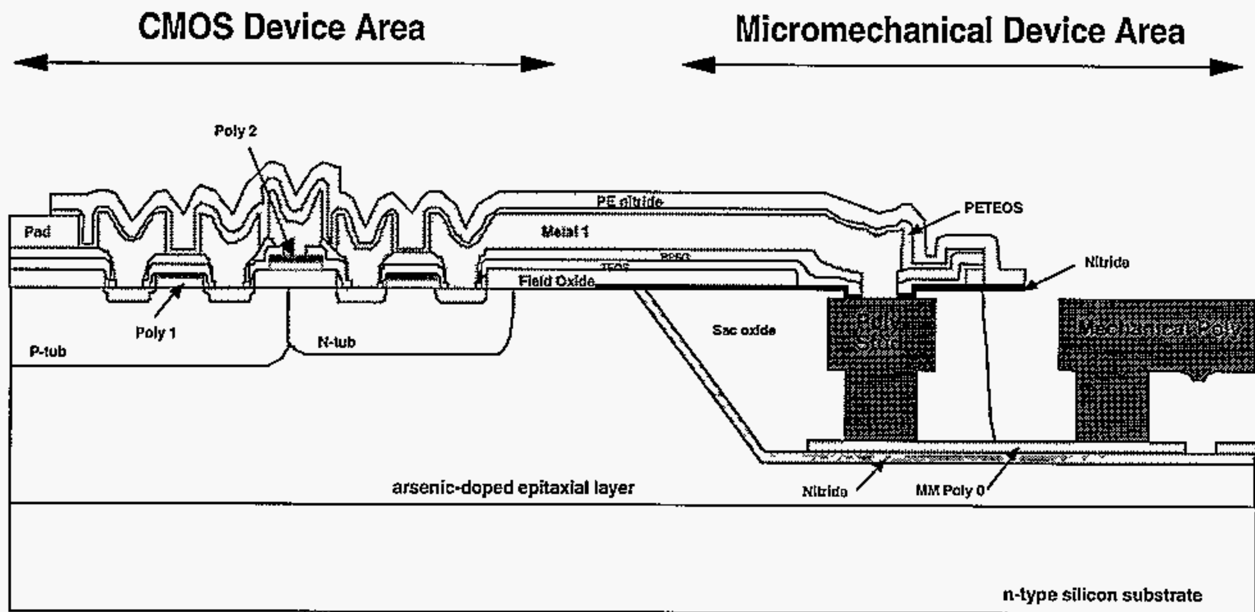


Figure 1. A cross-sectional schematic of the subsurface MEMS integrated technology.

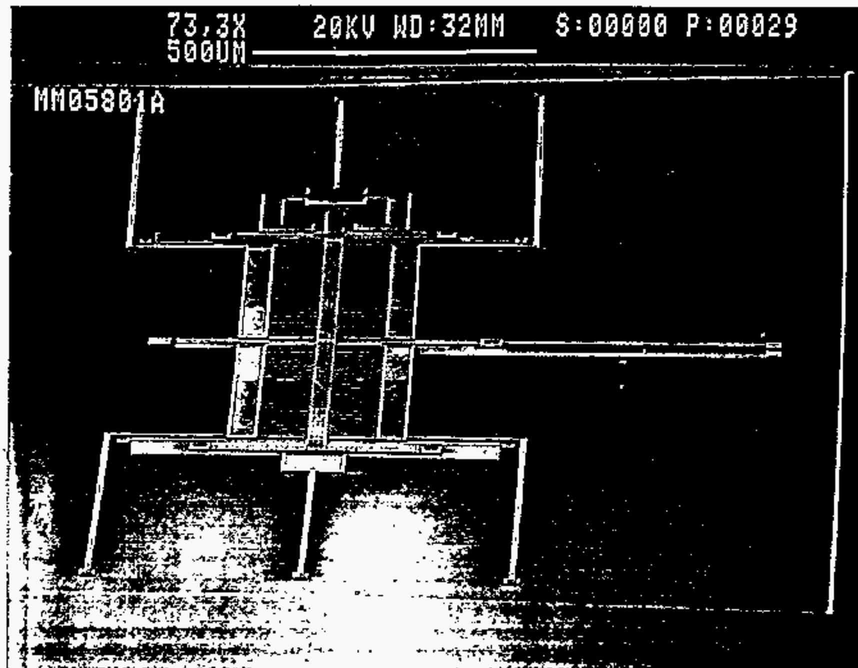


Figure 2. A surface-micromachined polysilicon accelerometer built in the bottom of a 6 μm trench.

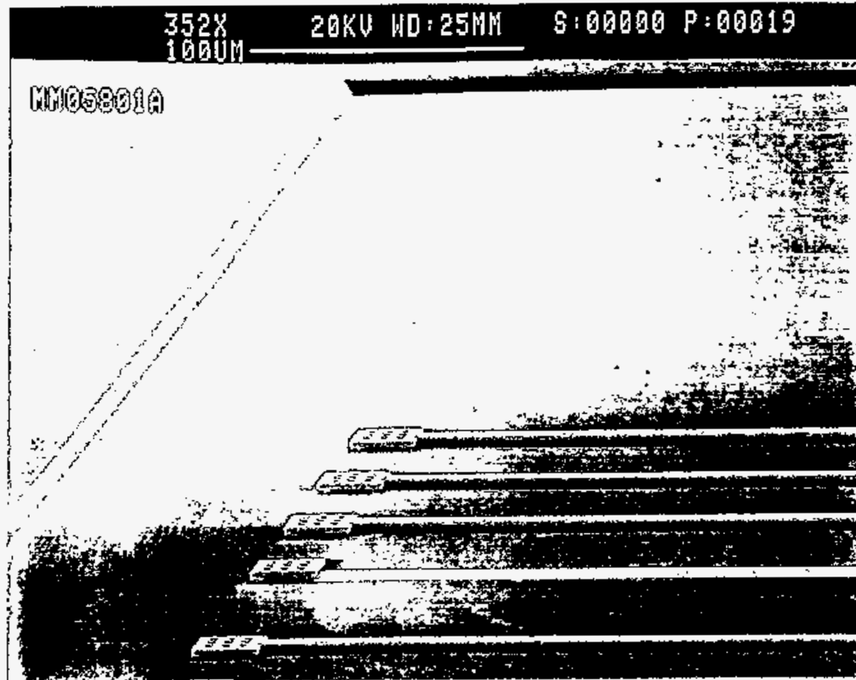


Figure 3. Interconnects leading to polysilicon studs for contact to CMOS metallization.

Figure 4. A cross-sectional view of a KOH-etched trench refilled with oxide and planarized using chemical-mechanical polishing. This planar structure is ready for standard CMOS processing.