Embedded Pitch Adapters: a High-Yield Interconnection Solution for Strip Sensors

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Abstract

A proposal to fabricate large area strip sensors with integrated, or embedded, pitch adapters is presented for the End-cap part of the Inner Tracker in the ATLAS experiment. To implement the embedded pitch adapters, a second metal layer is used in the sensor fabrication, for signal routing to the ASICs. Sensors with different embedded pitch adapters have been fabricated in order to optimize the design and technology. Inter-strip capacitance, noise, pick-up, cross-talk, signal efficiency, and fabrication yield have been taken into account in their design and fabrication. Inter-strip capacitance tests taking into account all channel neighbors reveal the important differences between the various designs considered. These tests have been correlated with noise figures obtained in full assembled modules, showing that the tests performed on the bare sensors are a valid tool to estimate the final noise in the full module. The full modules have been subjected to test beam experiments in order to evaluate the incidence of cross-talk, pick-up, and signal loss. The detailed analysis shows no indication of cross-talk or pick-up as no additional hits can be observed in any channel not being hit by the beam above 170 mV threshold, and the signal in those channels is always below 1% of the signal recorded in the channel being hit, above 100 mV threshold. First results on irradiated mini-sensors with embedded pitch adapters do not show any change in the interstrip capacitance measurements with only the first neighbors connected.

Keywords: Silicon radiation detectors; Strip sensors; HL-LHC; ATLAS Upgrade; ITk; Pitch adapters.

1. INTRODUCTION AND MOTIVATION

The interconnection of sensors and readout electronics is a subject of critical impact in the module design for High Energy Physics experiments, such as ATLAS. The sensors are made progressively larger, and the readout ASICs smaller, and both contain increasingly more channels. On the other hand, the pitch between bonding pads is usually very different between sensors and ASICs, which leads to unrealizable wire-bonding angles between them. With all this, the actual design of the electrical connection between sensors and ASICs is not trivial and it becomes a yield issue when the experiment contains tens or hundreds of millions of strip channels. The question is not anymore if the wire-bonding can be done, but if it can be done reliably enough to build a whole tracker in the required production time.

In the case of the current ATLAS experiment the interconnection was solved by adding external pitch adapters which facilitated the bonding at both sides, sensor and ASIC, and made the pitch adaptation by routing with metal tracks on a high-density metal-on-glass technology [1]. The downside of this solution is that, although the bonding is very much facilitated, the number of bonds is doubled. On top of that, an extra piece is added to the module, increasing the total mass, assembly complexity, and costs. The groups involved in the developments of the ATLAS Upgrade Inner Tracker (ITk) want to avoid this solution. Several studies have been made in order to identify the maximum angle that can be achieved by direct wire-bonding between detectors' and ASICs' bonding pads [2]. Angles below 20º are considered safe, which results in that direct wire-bonding can be used for the barrel design, but for the End-cap a solution might be needed due to the larger pitch variations in the 6 different sensor layouts [3].

In this paper, a proposal to fabricate large-area strip sensors with integrated, or embedded, pitch adapters is presented for the End-cap part of the Inner Tracker in the ATLAS experiment. To implement the embedded pitch adapters (EPA), a second metal layer is used at the end of the sensor fabrication in order to form additional metal tracks which contact the top metal of the strip's coupling capacitor (where the standard AC pad is) with an "embedded pad" that is placed on the

sensor right in front of the corresponding ASIC pad. In this way, the routing for the pitch adaptation from sensor to ASIC is done on the sensor itself, and direct bonding from sensor to ASIC is facilitated without the need to double the number of wire-bonds, making the wire-bonding faster and more reliable.

Nevertheless, there are some possible effects that have to be taken into account in the evaluation and use of the EPA:

Inter-strip Capacitance: An increase of the inter-strip capacitance can be expected from the increase of the total metal length and from the additional coupling of the second-metal tracks with each other and with the first-metal tracks, especially taking into account that the second-metal tracks have to cross over several first-metal tracks. This increase in the inter-strip capacitance implies an increase in the overall *noise*, thus the sensor channels with EPA will show more noise than the standard one-metal channels. Also, as the inter-strip capacitance in the EPA will depend strongly on the particular design, the noise can also vary from channel to channel, resulting in larger *noise variability* through the sensor.

Cross-talk: Signal transmitted between first-metal tracks (standard detector strip metal) and second-metal tracks (EPA metal) due to the coupling between them. This can result in spurious signals in not hit channels and in loss of signal (*efficiency*) for the hit channel.

Pick-up: Charge that can be induced in the second-metal tracks directly from the bulk when a particle crosses the sensor and charge is created in the bulk. This can also induce spurious signals in channels that are away from the actual hit channel and in loss of signal (*efficiency*) for the hit channel.

Yield: From a technological point of view, as there is an increase of the number and length of tracks plus the addition of an extra photolithographic step with the EPA, this could increase the probability of a short-circuit between channels, or an open circuit in a channel during the processing. This means a possible reduction in the number of good channels per sensor, and consequently also a possible reduction of the number of good sensors in a whole production.

The EPA have been implemented on the sensors fabricated for the prototype of the End-cap part of the ATLAS Upgrade Inner Tracker (ITk), the "petalet" [4][5]. Initial results on these sensors, which had first-generation layout designs, have shown no indication of cross-talk or pick-up from laser tests [6]. Nevertheless an increase in noise and noise variability has been observed in the first modules fabricated with those sensors as can be seen in Fig 1, where the noise results for petalet modules made with and without the first designs of EPA are shown. These tests were taken using threshold scans on a digital readout system to determine the noise level in electron noise equivalent. Fig 1 shows the noise per channel comparing typical sensors of "One metal" and "Embedded" designs. The electrical noise stemming from the readout system alone (without the sensors) is 380 +/- 10 ENC and has not been subtracted in the figure. For a typical one-metal sensor, the ENC noise is 550 with a deviation of at most 50 ENC. Six sensors with EPA have been built into modules and showed consistent behavior as seen in Fig. 1

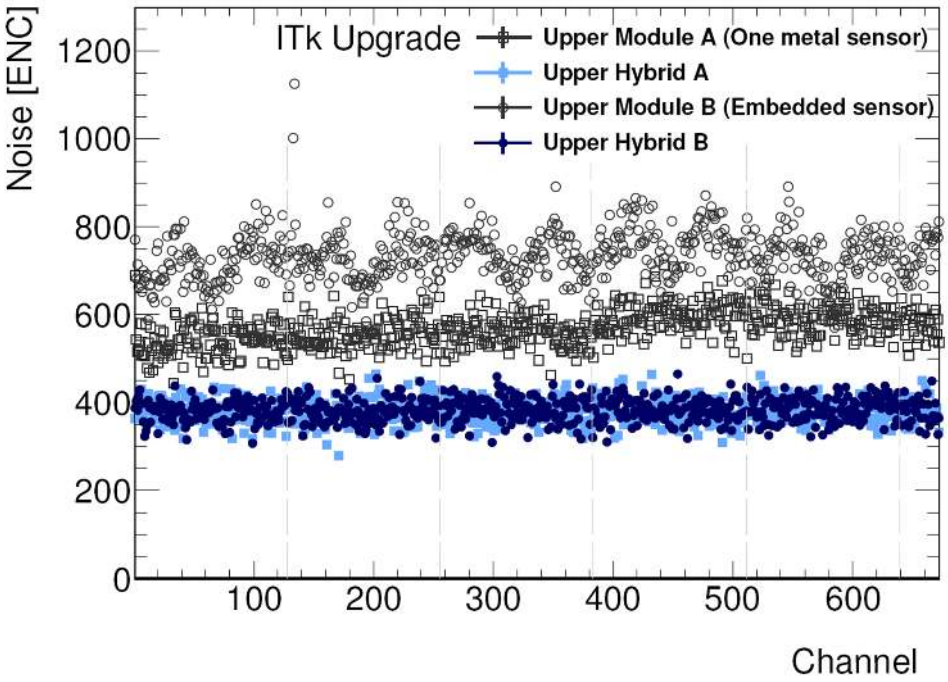

Figure 1: Noise results on module for sensors with and without EPA with the first layouts implemented.

2. DESIGN OF THE EMBEDDED PITCH ADAPTERS

In view of the results just mentioned about noise variability across the detector due to the different inter-strip capacitance in each channel for the initial design, 4 new layouts were designed in order to attempt reducing this variability and the rest of effects mentioned above. Fig 2 shows the 5 layouts that have been tried.

- **(a)** *Basic*: This is the first layout made for the initial batches and tests. The second-metal tracks keep the same angle (in each quadrant), i.e. they are parallel to each other, and this angle is the maximum that can be used for a minimum separation between tracks of 20 µm. This distance is chosen as a small but technologically safe distance between tracks in order not to compromise the yield.
- **(b)** *Equalized*: In this layout the second-metal tracks are parallel as in the *Basic*, but they are enlarged in order for them all to have the same length. This is done to equalize the inter-strip capacitance between all the channels and to avoid the variability in the noise.
- **(c)** *Varying*: In this layout the second-metal tracks have a constant angle with respect to each other. This angle is calculated so that they occupy all the 360 degrees (180º / 63 = 2.86º). In this way, the channels will be separated from each other, reducing their inter-strip capacitance. The channels are also enlarged in the center to make them have roughly the same length.
- **(d)** *Rectangular-A*: In this case, the second-metal channels go parallel to the first-metal channels from the pads until they can cross perpendicularly to them to reach their corresponding contact. The second-metal channels go in between the first-metal ones, and on top of the p-stop. In this way, the inter-strip capacitance to the first-metal channels is minimized.
- **(e)** *Rectangular-B*: In this case, the second-metal channels go parallel to the first-metal channels, but on top of them. This layout is more like a test structure (a worst-case) because in this case the inter-strip capacitance will be increased, although maybe the pick-up is minimized.

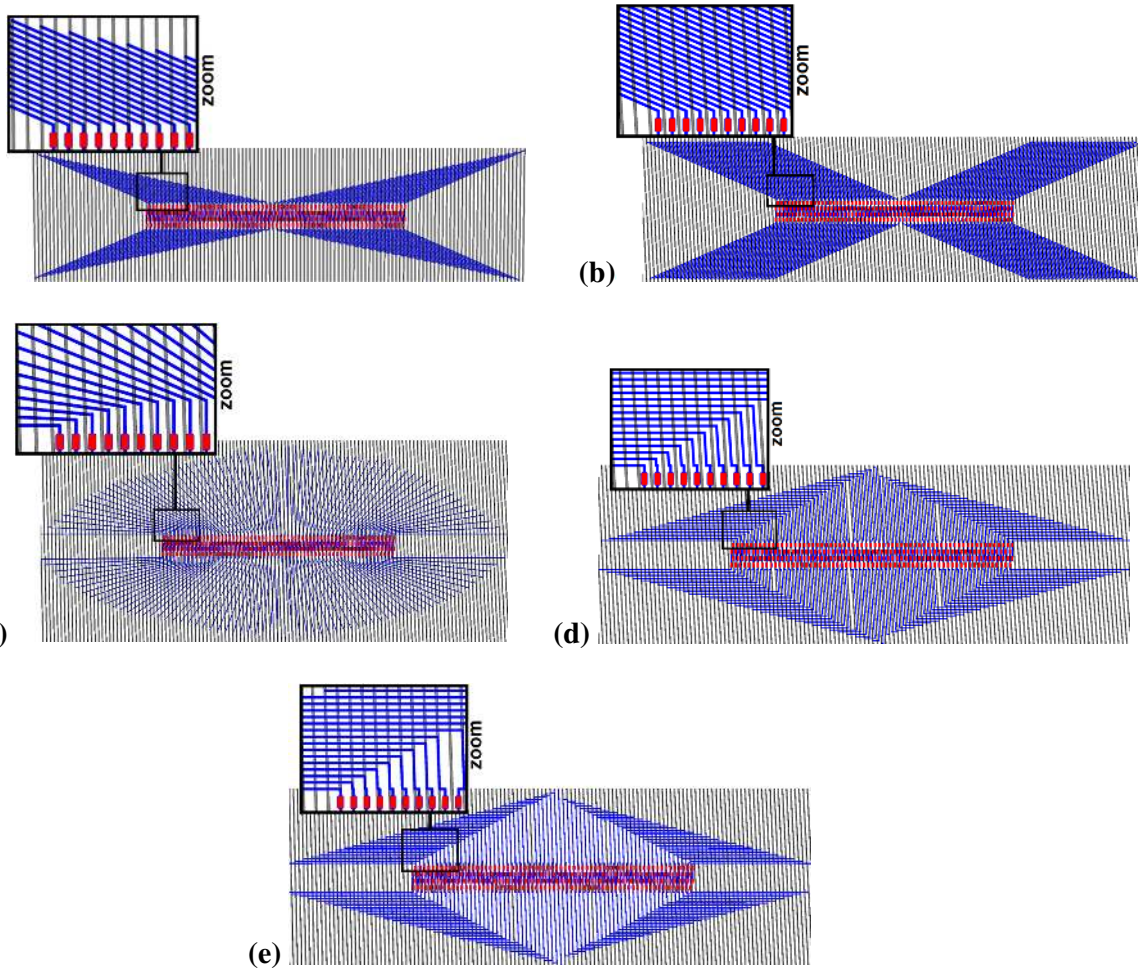

Figure 2: Images of the 5 different EPA layouts studied in this work.

Additionally, there are two options of each of these layouts: one in which the second-metal tracks have 20 µm width (as in the first designs), and another in which there tracks have 10 µm width. This second case is still far from the resolution limits of the technology but will allow a lower coupling between metal tracks.

All these layouts of EPA were added in a new full wafer mask which includes the two TOP sensors of the petalet prototype [4]. Each of these sensors has 2 strip rows and each strip row has 384 channels. The strip pitch in these sensors is variable, because the channels are oriented toward the beam in the End-cap part of the ITK, plus the strips are designed with built-in stereo angle. The strip pitch ranges then roughly from 93 µm to 104 µm across these sensors. The chips used for the readout in the petalet prototypes are the so-called ABC250 [7] which have 128 readout channels and pads staggered in two rows with constant pitch of 50 µm. Therefore there is room for 12 EPA in the whole wafer. One sensor (TOP-Left) includes the 5 EPA layouts with 20 µm track width, plus one basic design with 10 µm track width; and the other sensor (TOP-right) includes the 5 EPA layouts with 10 µm track width, plus one basic design with 20 µm track width. The full wafer design can be seen in Fig 3.

3. TECHNOLOGY AND FABRICATION

One full batch of TOP petalet sensors have been fabricated in the clean room of the Centro Nacional de Microelectronica (IMB-CNM, CSIC), Barcelona, Spain. High-resistivity, p-type, 300 μm thick wafers with 4 inches diameter have been used as substrates. The "standard" first-metal tracks, which are the top plate of the coupling capacitors, are made with a 0.5 μm thick sputtered Aluminum layer. The inter-metal oxide layer is deposited by a low-temperature Plasma Enhanced Chemical Vapor Deposition (PECVD) processing step. Four different inter-metal oxide thicknesses have been implemented in order to see the influence of this parameter and to study the technological difficulties. Finally, the second-metal tracks are made with a sputtered Aluminum layer which is 1.5 μm thick. A picture of one of the fabricated wafers is shown in Fig 3, where the different EPA designs can be clearly seen.

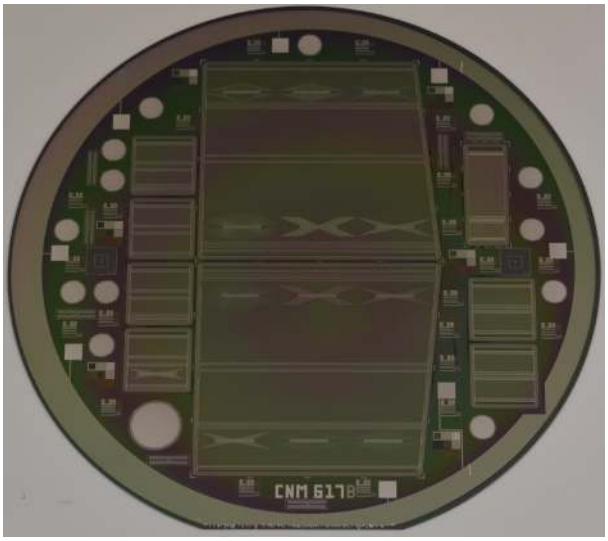

Figure 3: Picture of one of the wafers fabricated in the batch of TOP petalet sensors with the five EPA layouts, including also different mini-sensors and test structures.

Due to the different thermal expansion coefficients of silicon oxide and silicon, the inter-metal oxide layer creates stress. Many yield issues in multilevel technologies are related to stress [8]: cracking of dielectric layers, hillocks or stress voiding in aluminum lines, etc. These have not been observed during fabrication. We will therefore focus on the resulting wafer bowing which can affect the subsequent photolithographic steps, because it interferes with the alignment marks that are defined before and after the inter-metal oxide. The bowing of the sensors can also affect the assembly of the whole module, plus position resolution can be compromised. All this limits the inter-metal oxide thickness that can be used for the EPA fabrication. Consequently, the bowing of the different wafers was monitored during the fabrication of the sensors. Fig. 4 shows the results of wafer bowing tests for the different inter-metal oxide thicknesses. The bow is defined here, according to standards [9], as the distance between a point at wafer center, and a reference plane defined by three points at the wafer edges. Note that the bow can be positive or negative, which results respectively from compressive or tensile stress. In our case, the bow is positive because the stress from the inter-metal oxide is compressive. As it can be seen, the bowing is already very significant (roughly 300 μm) with 3 μm thick oxide, and although the photolithography could be realized without problems, this bowing would be too large for the proper assembly of the modules, and for particle position resolution for the tracking. In the case of 4 μm oxide thickness, the bowing of the wafers already generated difficulties in the processing, so this option is discarded already for technological reasons.

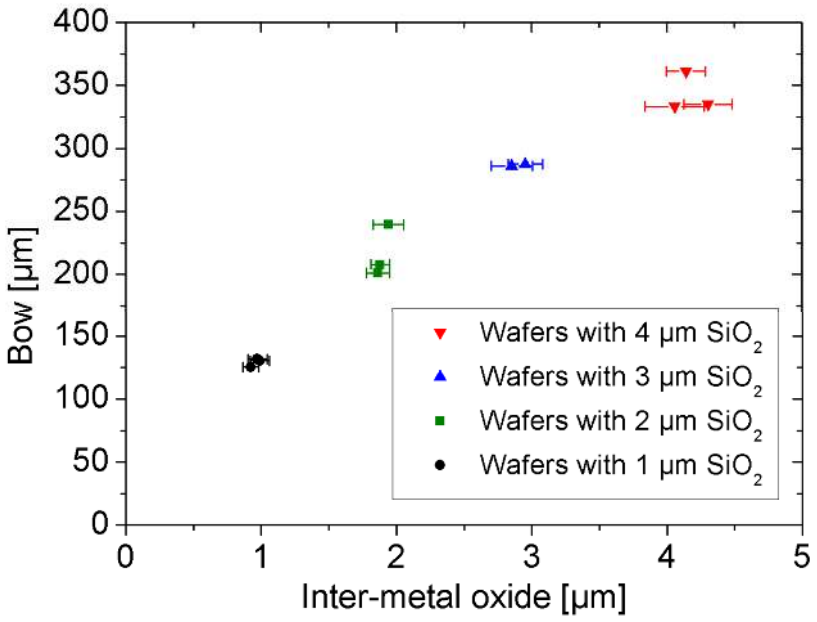

Figure 4: Wafer bowing as a function of the inter-metal oxide thickness for all the wafers fabricated.

The quality of the via contact between the second metal and the first metal was also checked in order to find out if this affects the yield of good channels in the sensors. Daisy-chain test structures including more than 200 vias were implemented in the wafer design for this purpose. The daisy chains are just series of vias connected in series such that the first via goes from metal 2 to metal 1, then a short line of metal 1 connects to the next via which goes from metal 1 to metal 2, then a short line of metal 2 connects to the next via with goes from metal 2 to metal 1, and so forth. Fig 5 shows the results obtained for the via resistance when different number of vias are measured in series. As it can be seen, the value stabilizes very nicely at about 0.18 Ohms/via for high number of vias series, when the influence of parasitic resistances from the setup becomes negligible (high number of vias measured in series). The resistance value is independent of the inter-metal oxide thickness, indicating a very good fill of the via contact with the metal. Regarding yield, not a single daisy-chain failure was found in measurements of 200 vias in series, measuring at least 2 daisy chains per wafer in all the wafers. The daisy chain test structures could not be distributed across the wafer, as it would have been optimal, due to layout limitations. The structures were placed only on one side, not very close to the center of the wafer. It has to be mentioned that a technological problem was found in the thick oxide wafers, where an incomplete etching of the vias produced defective contact from second to first metal in the center of the wafers. This is due to the combined inhomogeneity of the oxide deposition and etching process, and can be easily corrected by a controlled via over etch. Still, this is not considered a via yield problem, as the vias that are correctly etched make a correct low-resistance contact with no-measurable statistical failure.

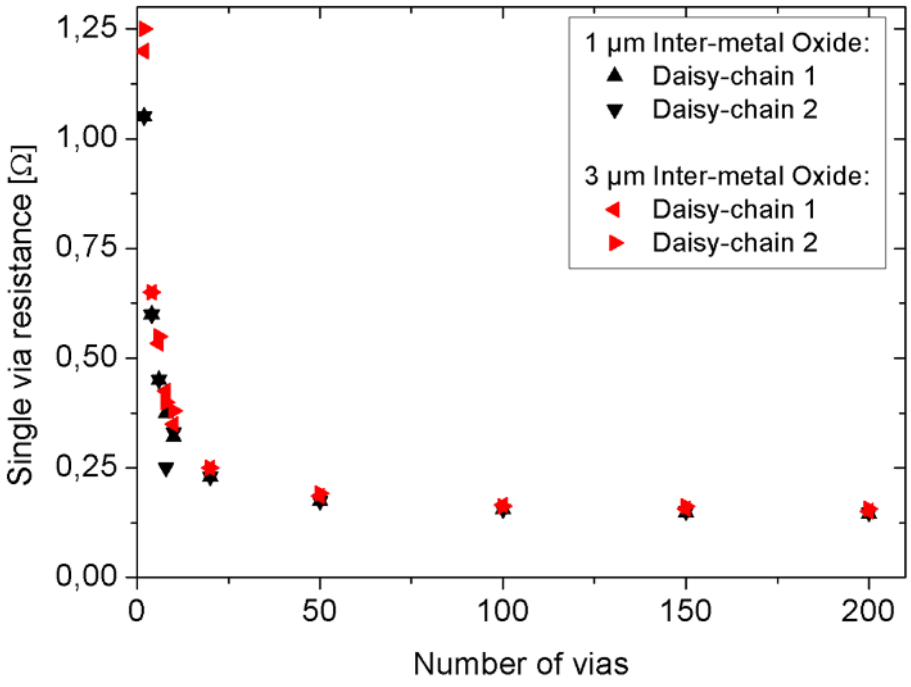

Figure 5: Values of the via resistance obtained from measurements of resistance of daisy-chains of vias in series, and for different number of vias. As it can be seen, when the number of vias in series is too small the error in the result is large because the parasitic resistances of the measurement become relevant Measurements shown for different daisy-chains and for different inter-metal oxide thicknesses.

4. INTER-STRIP CAPACITANCE TESTS

As explained above, the use of an additional second-metal track on every channel in order to make the connectivity and pitch adaptation to the ASIC, can produce an increase in the inter-strip capacitance of the channel. This will result in an increase of the noise per channel. Additionally, the inter-strip capacitance will vary from channel to channel as the second-metal track is in principle different for every channel, and so will do the noise, increasing the noise variability. In order to control that and to identify the differences between the five EPA layouts with respect to noise, inter-strip capacitance has to be measured for all the channels.

On the other hand, one specific feature of the EPA is that the second-metal channels cross on top of many of the first-metal channels, increasing the coupling between channels that are far from each other in the sensor, the "far neighbors". This implies that the usual way of testing inter-strip capacitance by measuring it only with respect of the 2 or 4 neighbors, is not a good approximation in this case. A test of the inter-strip capacitance of every channel has to take into account all the rest of the channels, "all neighbors", in order to have a proper measurement. Only this way the channel noise variability could be deduced from the inter-strip capacitance tests. For this purpose, a probe card with 128 probes has been used for inter-strip capacitance tests in this work. Only this way, the correct capacitance measurement can be done between the strip under tests and all the rest of the channels that are purposely grounded. In practice, our switching matrix has only 24 input channels, therefore the strips are measured in groups of 20, by moving the probe card across the EPA pads. But with the 128 probe card we can be assured that all the relevant neighbor channels (the ones that can cross the strips under test) are grounded during the measurement. The measurements have been performed using and Agilent 4284A LCR meter. A correction has been applied to all the

measurements individually. Before probing the pads, a capacitance measurement is performed in the 20 active probes without connecting the probe card to anything ('OPEN' configuration). This value is recorded for each probe and subtracted for every individual capacitance measurement that is taken with this particular probe.

The results of the inter-strip capacitance tests for the 5 EPA structures fabricated according to the 5 layouts described above using 20 µm track width can be seen in Fig 6. In the first plot (a) one can confirm that the inter-strip capacitance reproduces qualitatively the noise shape shown in Fig 1 for modules assembled with the first EPA layout implemented. The second plot (b) reveals that although the number of crossings between second metal and first metal and the total track length is made the same in this layout for all the channels, the coupling of the second-metal tracks with far neighbors is dominant because of the short separation between tracks, therefore, the channels with more neighbors show increased inter-strip capacitance, actually enhancing the undesired shape of the *Basic* layout. The third plot (c) shows that with the *Varying* layout, the inter-strip capacitance is "equalized" in the center of the structure with respect to the *Basic* structure, but the inter-strip capacitance reduction at the structure edges keeps its variability. The forth plot (d) shows the best equalization on inter-strip capacitance achieved with all structures, corresponding to the *Rectangular-A* layout. The fact that the second-metal tracts are quite separated from each other and from first-metal tracks, seems to be the dominant influence in this result. Finally, the fifth plot (e) shows the expected behavior of the *Rectangular-B* layout where the fact that the central tracks are on top of the first-metal tracks for long distances, increases the inter-strip capacitance for them.

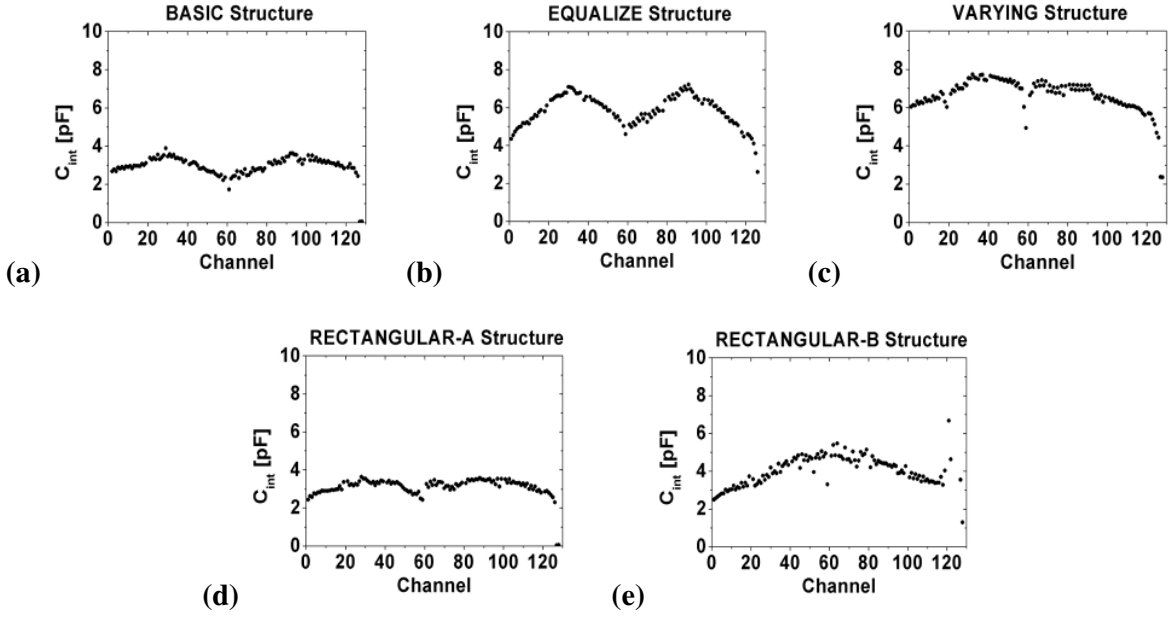

Figure 6: Inter-strip capacitance tests results for the 5 EPA layouts with 20 µm track width.
(a) *Basic*, (b) *Equalize*, (c) *Varying*, (d) *Rectangular-A*, and (d) *Rectangular-B*

Fig 7 represents the differences in inter-strip capacitance for 3 selected structures for second-metal track width of 20 or 10 µm. As can be seen in the first plot (a) the variability of the *Basic* layout is quite improved when the track width is reduced due to the important reduction in second-metal tracks coupling with each other when the track width is halved while maintaining the track pitch, which has effectively increased the track separation by a 50%. The same effect is observed, although enhanced, in the *Equalize* structure (b), where the inter-strip capacitance variability has been quite

reduced. Finally, *Rectangular-A* structure shows only a small effect of the track width reduction on inter-strip capacitance, as the separation between tracks is already large with 20 µm track width.

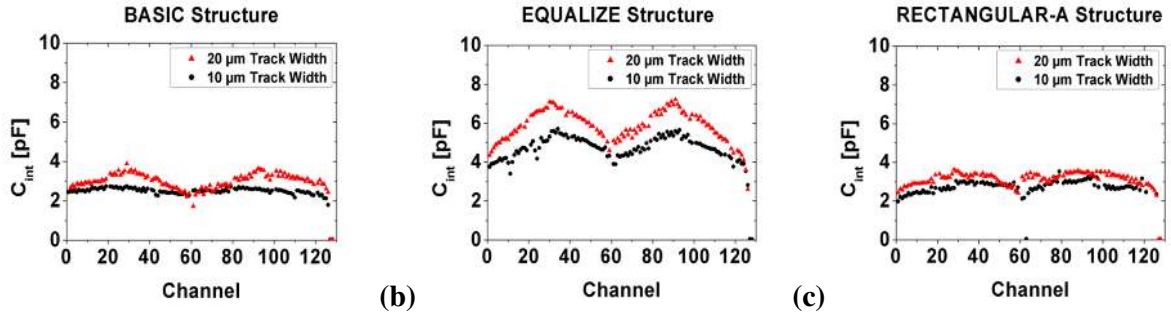

Figure 7: Inter-strip capacitance results for 20 and 10 µm track width for different structures: (a) *Basic*, (b) *Equalize*, and (c) *Rectangular-A*

Finally, Fig 8 shows the effect of inter-metal oxide thickness on the inter-strip capacitance in *Basic* and *Rectangular-A* layouts. In plot (a) one can see that the increase in inter-metal oxide does not have an effect in the inter-strip capacitance variability. This agrees with the fact that the inter-strip capacitance variability in the Basic layout comes mainly from the second-metal tracks coupling to each-other, and not with the coupling with the first-metal tracks. In plot (b) it can be seen that the inter-strip capacitance in *Rectangular-A* is flattened even more, resulting in quite a flat plot, reducing very much the variability. This is consistent with the fact that the inter-strip capacitance in *Rectangular-A* layout is mostly dependent on first metal to second metal coupling. On the other hand, in both cases a general increase of the inter-strip capacitance is observed for thicker oxides. We do not have an explanation for this result yet.

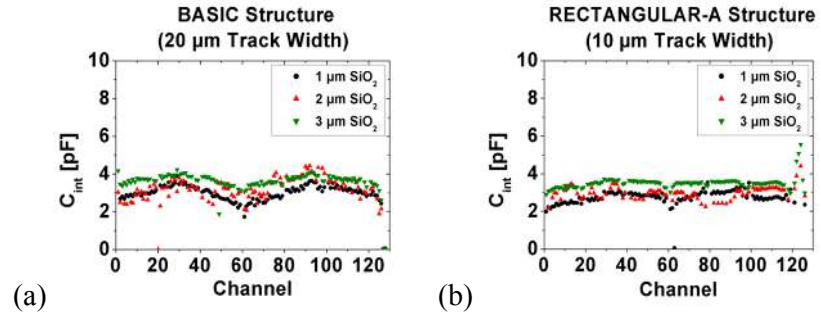

Figure 8: Inter-strip capacitance results for different inter-metal oxide thicknesses in two structures. (a) *Basic* and (b) *Rectangular-A*

The two TOP sensors from one of the wafers fabricated with 1 µm inter-metal oxide thickness were mounted in a module. Fig 9 shows the equivalent noise charge (ENC) measured for all the channels in this module, indicating the correspondence with the different EPA layouts. For the measurements, 2 fC charges are injected into all channels, then 200 triggers are sent into each channel and the ASICs are read out repeatedly with increasing thresholds. From the resulting S-curve, all characteristics of each channel, such as noise, are determined in a fit. The readout is done with the full testing setup [10]: the module is connected to HSIO ('High Speed Input Output') board developed by the ITk collaboration) [11], and read out with a root program called SCTDAQ developed at Rutherford Appleton Laboratory (RAL) [12]. One can confirm the expected good correlation between the inter-strip capacitance and the noise for the different structures [13][14], which demonstrates that the inter-strip capacitance measurements, with all-neighbors considered, are a proper test to estimate the noise behavior of the different EPA layouts [15].

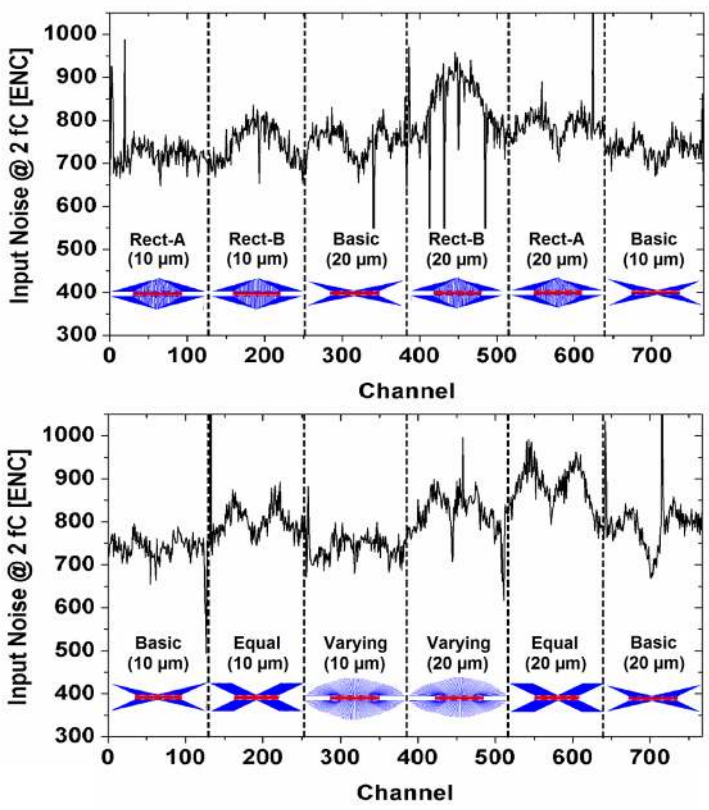

Figure 9: Noise results for the different EPA layouts measured on a module assembled with one of the wafers fabricated.

Additionally, some miniature sensors with EPA have been irradiated with 70 MeV protons at the Cyclotron and Radioisotope Center (CYRIC), Tohoku University, Japan, in order to see the influence of radiation on the inter-strip capacitance of sensors with EPA. The fluences achieved were 5.3×10^{14}, and 1.2×10^{15} 1 MeV equivalent neutrons/cm^2. The last fluence is the current target value for the strip sensors in the future ITk. Sensors irradiated to those fluences with the *Basic* EPA layout, 20 µm track width, and 1 µm inter-metal oxide thickness have been tested. At this point, only inter-strip capacitance measurements considering first neighbor channels have been taken, because the irradiated sensors need cooling in order to bias them at full depletion voltage with controlled leakage current, and the test setup with the 128-probes probe card does not have a cooling system available. Nevertheless, as it can be seen in Fig 10, the results of the tests performed on the irradiated miniature sensors do not show any influence of radiation in the inter-strip capacitance. This will have to be confirmed with all-neighbors inter-strip capacitance tests.

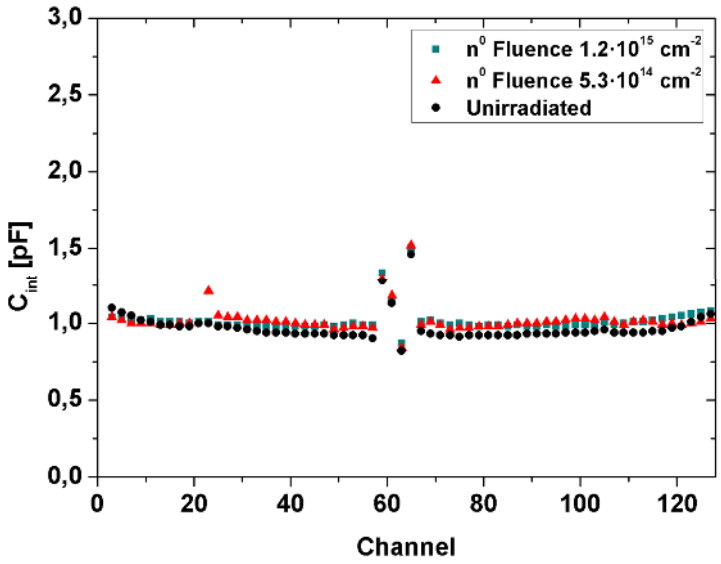

Figure 10:First-neighbors interstrip capacitance tests for the irradiated miniature detectors.

5. BEAM TEST

The full module assembled with two TOP petalet sensors from one of the wafers fabricated with 1 µm inter-metal oxide thickness have been subjected to test beam experiments at the Diamond Light Source synchrotron in the UK. The 15 keV beam has a rate of up to 2 kHz and it is microfocused to a spot size of 3.27µm x 1.65µm (FWHM) which guarantees to hit only one strip at a time. There is an xyz-stage with micron precision positioning to move the beam across the target. As for the setup, the module was held in place with vacuum, a chiller with a cooling liquid of a temperature of 15°C was used to cool the module. The environmental conditions inside the box where the module was mounted were monitored using temperature and humidity sensors placed close to the module. A low flow of nitrogen at room temperature was used to prevent condensation inside the box. During the whole duration of the measurement, inside the box temperature and humidity were stable at 20°C, and 50% humidity.

One quarter of each EPA structure was scanned with the beam hitting every other channel, meaning that 16 strips were scanned of each structure. Each structure was scanned twice: once on top of the second-metal tracks, and once away from them, in order to distinguish between cross-talk and pick-up. 3500 triggers were allowed per strip and per threshold, but the photon conversion efficiency inside a time window opened by a trigger is only roughly 60%, which results in about 2000 events registered per strip. Three threshold ranges were used: 80-200 mV in steps of 6.4 mV, 200-300 mV in steps of 39.4 mV, 300-450 mV in steps of 9.6 mV, resulting in 40 threshold steps per beam position on the strips. For each photon undergoing interactions in the silicon, a deposited charge of about 0.6 fC is expected, corresponding to a minimum signal of roughly 60 mV. Since multiple interactions can occur, up to 3 fC can be deposited. A minimum ionizing particle is expected to produce a signal of about 300 mV.

Fig 11 shows one typical result for the beam pointing to a specific strip (here strip 33) hit in a structure (here structure Rectangular B as the worst-case structure). The figure represents the ratio between the signal in every channel with respect to the signal in the channel being hit, once the background has been subtracted, for all the thresholds. The background has been determined by the

spurious signal, that is, noise, measured in a specific strip if the beam was pointing at a completely different area of the sensor that is read out by a different readout chip, and averaged over 16 times 10 measurements. As it can be seen, there is no sign of spurious signal in any channel above 170 mV threshold. On the other hand, the signal in the channels not being hit is below 1% of the signal recorded in the channel being hit, above 100 mV. The non-zero occupancy for the non-hit channel is likely due to the readout electronics performance at low threshold levels. All this is an indication that there is no sign of cross-talk or pick-up, at least to the level of statistics achieved in this test beam. A deeper analysis of the test beam results is being done to obtain more detailed information on the possible spurious signals at lower thresholds. More test beams are foreseen with tracking capabilities and using irradiated sensors to confirm these results.

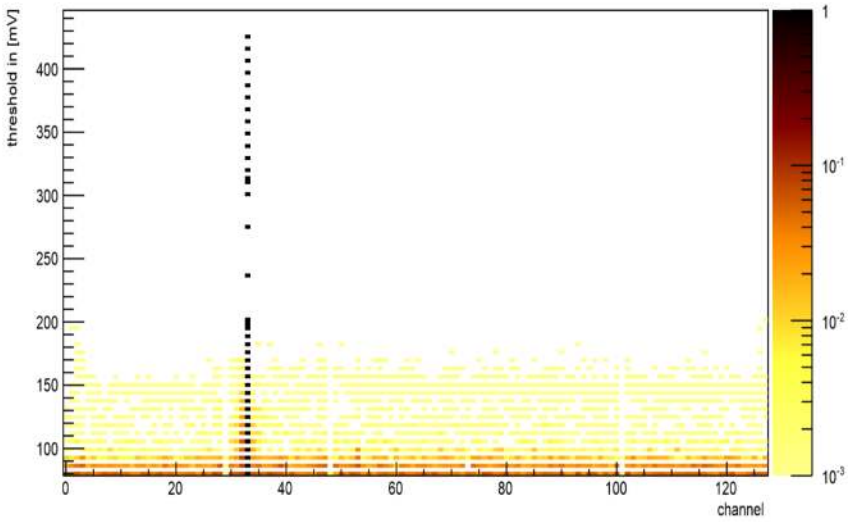

Figure 11: Channel signal ratio to the hit channel signal for all the thresholds (background subtracted). The color code on the right corresponds to ratio between the signal (number of hits) in the corresponding channel with respect to the signal in the channel being hit, once the background has been subtracted.

6. CONCLUSION

A new proposal is presented to improve the throughput and reliability of the interconnection between sensors and electronics in the Inner Tracker on the ATLAS Upgrade experiment for the HL-LHC. A second metal layer is used to make the pitch adaptation integrated in the sensor. New layouts for these Embedded Pitch Adapters are tested, together with new design and technological improvements such as the reduction of second-metal track width, and the increase in the inter-metal oxide thickness. The effect of these factors on the inter-strip capacitance is measured by a new method that takes into account the effect of all neighbors. The results presented demonstrate the reduction in interstrip capacitance variability down to a few tenths of pF with some of the designs and with the reduction of the second-metal track width. The increase in inter-metal oxide thickness helps in the flattening of the inter-strip capacitance for some of the structures, but produces a general increase of its value in all the channels of about 1 pF that is still to be fully understood. Measurements of miniature sensors irradiated at different fluences show no influence of radiation damage on the interstrip capacitance, for measurements with first neighbors. The analysis from the beam test shows no indication of cross-talk or pick-up above 170 mV threshold. A deeper analysis of the test beam results and more test beams with tracking capabilities are foreseen to confirm this result in detail.

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