# Embedded Two-Phase Cooling of High Flux Electronics Via Press-Fit and Bonded FEEDS Coolers

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*The increasing heat densities in electronic components and focus on energy efficiency have motivated utilization of embedded two-phase cooling, which reduces system-level thermal resistance and pumping power. To achieve maximum benefit, high heat fluxes and vapor qualities should be achieved simultaneously. While many researchers have achieved heat fluxes in excess of 1 kW/cm$^2$, vapor qualities are often below 10%, requiring a significantly large amount of energy spent on subcooling or pumping power, which minimizes the benefit of using two-phase thermal transport. In this work, we describe our recent work with cooling devices utilizing film evaporation with an enhanced fluid delivery system (FEEDS). The design, calibration, and experimental testing of a press-fit and bonded FEEDS test section are detailed here. Heat transfer and pressure drop performance was characterized and discussed. With the press-fit Si test chip, heat fluxes in excess of 1 kW/cm$^2$ were obtained at vapor qualities approaching 45% and a coefficient of performance (COP) approaching 1400. With the bonded SiC test chip, heat fluxes in excess of 1 kW/cm$^2$ were achieved at a vapor quality of 85% and heat densities approaching 490 W/cm$^3$.* [DOI: 10.1115/1.4039264]

*Keywords: high heat flux electronic cooling, two-phase flow, manifold microchannels, FEEDS*

## 1 Introduction

The rapid increase in heat dissipation of next-generation integrated circuits necessitates superior—and hence more complex—cooling methods for heat fluxes on the order of a kW/cm$^2$. In conventional electronic cooling systems, a source heat flux is reduced and transported to a remote heat sink through a series of thermal interface materials and heat spreaders (c.f., Fig. 1(*a*)). However, this causes an increase in thermal resistance between the heat sink and the source, and thus it becomes difficult to maintain chip temperatures below operating limits, especially for next-generation integrated circuits. Recently, embedded two-phase cooling (c.f., Fig. 1(*b*)), where the heat sink fins are etched directly into the semiconductor substrate, has gained attention due to their remarkable heat removal capability resulting from the elimination of thermal interface materials and caloric resistance that increase system-level (junction-to-ambient) thermal resistance [1].

Recent programs, such as DARPA's ICECool fundamentals [2], have motivated the development of high-performing and efficient two-phase cooling systems for electronics. DARPA has laid out strict objectives relating to heat flux, die temperature, heat density, vapor quality, pressure drop, and coefficient of performance (COP), summarized in Table 1. These aggressive goals require heat fluxes in excess of 1 kW/cm$^2$, heat densities in excess of 1 kW/cm$^3$, vapor qualities in excess of 90%, and pressure drops below 10% of absolute, while maintaining surface temperature rises of less than 30 K—an equivalent thermal conductance of 333 kW/m$^2$ K. While overall thermal conductances of this magnitude have been reached, they are often achieved at lower heat fluxes and outlet vapor qualities [3,4]. It is clearly a challenge to obtain all the metrics simultaneously.

While reducing hydraulic diameter increases heat conductance, it comes at the price of increased pressure drop and pumping power, thereby preventing an easy solution to the ICECool problem. To get the best of both worlds, a film evaporation with an enhanced fluid delivery system (FEEDS) cooler was proposed,

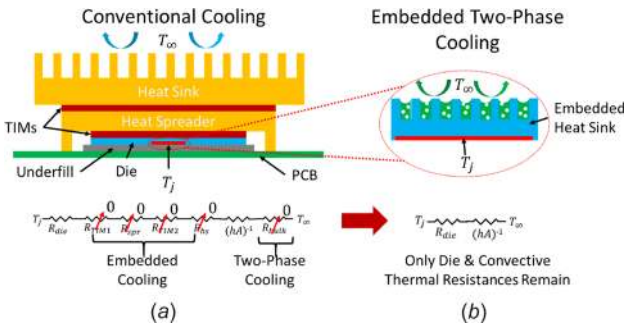


**Fig. 1 (*a*) Conventional cooling paradigm versus (*b*) embedded cooling paradigm**

**Table 1 Objectives of DARPA's ICECool fundamentals program [2]**

| Parameter | Value (units) |
|---|---|
| Outlet vapor quality | >90 (%) |
| Pressure drop | <0.1 $P_{sat}$ (kPa) |
| Heat flux | >1 (kW/cm$^2$) |
| Heat density | >1 (kW/cm$^3$) |
| Temperature rise above inlet | <30 (K) |
| Thermofluid COP | >30 |
| Minimum heat conductance | 333 (kW/m$^2$ K) |

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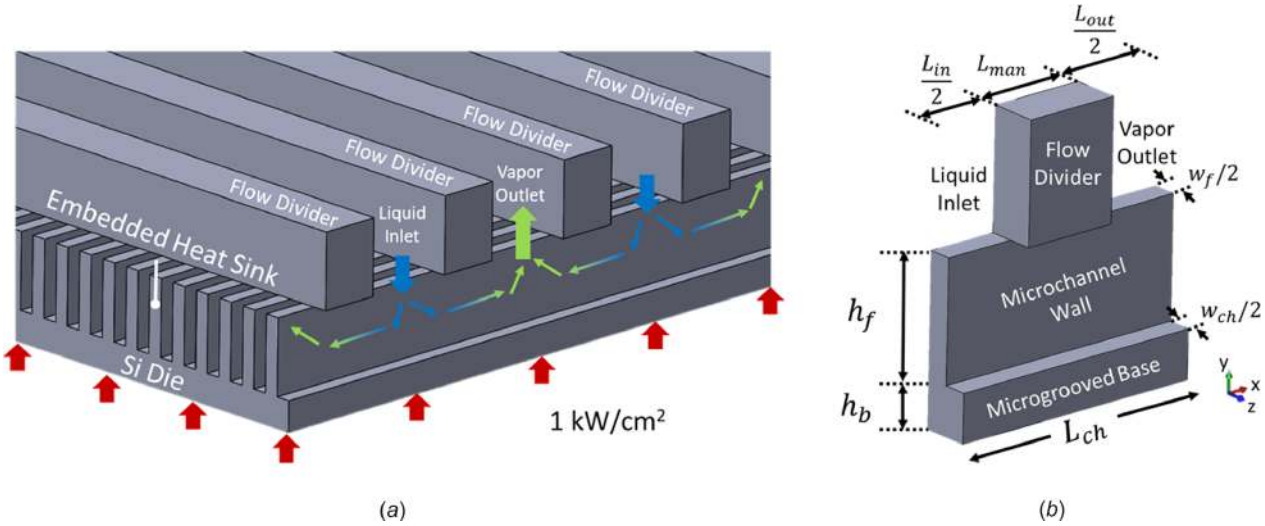


**Fig. 2 (*a*) Two-phase manifold-microchannel flow configuration and (*b*) geometric definitions of manifold-microchannel unit cell**

which provides a unique means of simultaneously enhancing heat transfer rate and reducing pressure drop and pumping power. FEEDS coolers are manifold microchannels that combine film evaporation with an enhanced fluid delivery system specifically designed to provide a uniform flow distribution in two-phase mode. Manifold microchannels work by dividing a microgrooved surface into a system of microchannels working in parallel. A manifold structure, containing alternating liquid feed channels and vapor outlet channels, is placed perpendicular to a microgrooved surface, as shown in Fig. 2(*a*). Subcooled or saturated liquid enters the liquid inlet, where it is forced downward between the fins into the microchannel. The liquid is then heated and evaporated, and the resulting two-phase mixture flows upward through the vapor outlet. It has been shown analytically in Ref. [3] that single-phase manifold microchannels have the potential to reduce pumping power by a factor of $n^2$—where $n$ is the number of flow divisions—due to the simultaneous reduction of flow rate and flow length, both of which are linearly correlated with pressure drop. Meanwhile, reduced flow length serves to enhance heat transfer by taking advantage of the higher heat transfer coefficients associated with a thermally developing flow regime. The FEEDS approach is also particularly appealing for two-phase cooling of hot spots in high flux electronics due to the ability of the manifold to locally feed the flow and reduce localized dry out. In addition, should a dry out event occur, the required spreading distance is greatly reduced due to the small pitch between manifolds.

## 2 Literature Survey

Much experimental work has been conducted in the field of two-phase ultra-high flux cooling. Palko et al. [5] utilized a diamond heat sink with laser-micromachined triangular grooves approximately 250 $\mu$m wide and 500 $\mu$m deep, and coated in a conformal 5 $\mu$m copper porous wick structure. Fluid was supplied via a manifold fabricated from polyimide layers designed to vent the vapor flow. A peak heat flux of 1340 W/cm$^2$ was obtained at a pressure drop of 42 kPa. However, due to extreme subcooling, the corresponding thermodynamic outlet vapor quality was near 0%. Kandlikar et al. [6], and more recently Kalani et al. [7], tested 200 $\mu$m wide by 200 $\mu$m deep microchannels with a 6% tapered gap manifold. The gap between the manifold and the microchannels allows vapor to escape from the microchannels, while the inertia of the flow due to the high mass fluxes (2300–5000 kg/m$^2$ s) ensures the liquid enters and stays in the microchannel. A peak heat flux of 1070 W/cm$^2$ and 30 kPa pressure drop were obtained using water at 14% thermodynamic outlet vapor quality. Zhu et al. [8] tested various micropillar arrays etched onto the bottom of a 500 $\mu$m wide by 500 $\mu$m deep microchannel. Water was used as the working fluid, and a mass flux of 300 kg/m$^2$ s was supplied to the microchannel. A peak heat flux of 969 W/cm$^2$ was obtained at a vapor quality of 29% and a pressure drop of 14.3 kPa. Houshmand et al. [9] utilized microtubes of diameters ranging between 150 and 265 $\mu$m to test saturated and subcooled flow boiling. Mass fluxes between 2000 and 7100 kg/m$^2$ s were tested at qualities ranging from −4% to 14% thermodynamic vapor quality. A peak heat flux of 1000 W/cm$^2$ was obtained using methanol. However, due to the high mass fluxes and subcooling, the thermodynamic outlet vapor quality was below zero. Li et al. [10] tested 300 $\mu$m wide by 1000 $\mu$m deep pin fins in spray cooling over a 9 cm$^2$ area. Mass fluxes ranging from 22 to 41 kg/m$^2$ s were tested at thermodynamic outlet vapor qualities ranging from 14% to 34%. A peak heat flux of 326 W/cm$^2$ was obtained using R134a at 16% thermodynamic outlet vapor quality. Drummond et al. [11,12] tested a manifold-microchannel array of 15 $\mu$m wide by 300 $\mu$m deep microchannels. Mass fluxes ranging between 1300 and 2070 kg/m$^2$ s and thermodynamic outlet vapor qualities between −7% and 30% were tested. A peak heat flux of 910 W/cm$^2$ was obtained using HFE7100 at 10% thermodynamic outlet vapor quality and 160 kPa pressure drop. Agostini et al. [13,14] tested an array of straight microchannels that were 223 $\mu$m wide by 680 $\mu$m deep. Mass fluxes ranged between 281 and 1501 kg/m$^2$ s, and outlet vapor qualities ranged between 0% and 78%. A peak heat flux of 221 W/cm$^2$ at 55% vapor quality was obtained with R236fa, and a peak heat flux of 190 W/cm$^2$ at 65% outlet vapor quality was obtained with R245fa. Finally, Cetegen [3] and Ohadi et al. [4] conducted experimental testing of two-phase manifold-microchannel coolers. Conductances as high as 330 W/m$^2$ K and heat fluxes above 1.2 kW/cm$^2$ were achieved separately at moderate pressure drops and vapor qualities ranging from 10% to 20% [3]. At lower heat fluxes, vapor qualities approaching 70% were achieved. A summary of the literature survey is given in Table 2.

## 3 Experimental Methods

Experimental results for two classes of FEEDS coolers will be reported here: press-fit FEEDS and bonded FEEDS. In the press-fit design, all of the components of the test section are held in place with mechanical force, as described in Refs. [15] and [16]; in the bonded design, the number of components is greatly reduced, and the chip and manifold are permanently bonded

**Table 2 Summary of two-phase ultrahigh heat flux cooling survey**

| Authors | Fluid | Mass fluxes (kg/m$^2$ s) | Channel width/height ($\mu$m/$\mu$m) | Subcooling (° C) | Vapor quality range (%) | Performance at max heat flux |
|---|---|---|---|---|---|---|
| Palko et al. [5] | Water | 14–43 | 500/500 | 75 | −13 to 13 | 1342 W/cm$^2$ at ∼0% and 42 kPa |
| Kandlikar et al. [6] and Kalani and Kandlikar [7] | Water | 2300–5000 | 200/200 | 10 | 0–14 | 1070 W/cm$^2$ at 14% and 30 kPa |
| Zhu et al. [8] | Water | 300 | 500/500 | 10 | 0–30 | 969 W/cm$^2$ at 29% and 14.3 kPa |
| Houshmand et al. [9] | Methanol | 2000–7100 | 150–265/(n/a) | 6–42 | −4 to 14 | 1000 W/cm$^2$ at −4% |
| Li et al. [10] | R134a | 22–41 | 300/1000 | <4 | 14–34 | 326 W/cm$^2$ at 16% |
| Drummond et al. [11,12] | HFE-7100 | 600–2070 | 15–30/35–300 | 5 | −7 to 30 | 910 W/cm$^2$ at 10%, 29 kW/m$^2$ K and 160 kPa |
| Agostini et al. [13] | R236fa | 281–1501 | 223/680 | ∼0 | 2–75 | 221 W/cm$^2$ at 55% |
| Agostini et al. [14] | R245fa | 281–1501 | 223/680 | 0–19 | 0–78 | 190 W/cm$^2$ at 65% |
| Cetegen [3] and Ohadi et al. [4] | R245fa | 200–1400 | 22–60/406–483 | 0–13 | 0–70 | 1200 W/cm$^2$ at 20%, 36 kW/m$^2$ K and 62 kPa |
| Present work | R245fa | 300–1200 | 8.5–9/50–100 | 0–5 | 0–85 | 1000 W/cm$^2$ at 85% and 30 kW/m$^2$ K |

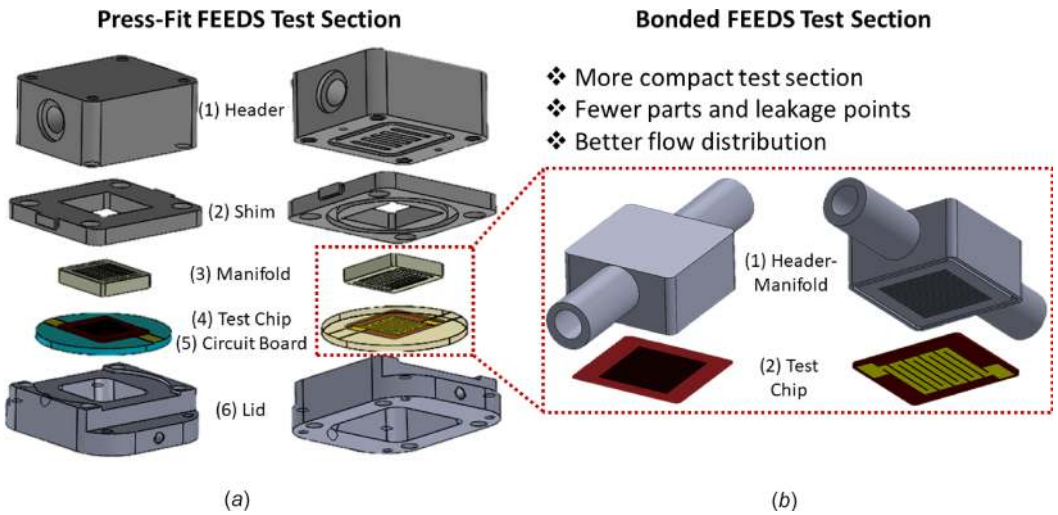


**Fig. 3 Film evaporation with an enhanced fluid delivery system experimental designs for (*a*) press-fit test section and (*b*) bonded test section**

together using a thin-film soldering technique, as described in Refs. [15], [17], and [18]. The press-fit test section, shown in Fig. 3(*a*), consists of six basic components:

(1) the header, which directs the separate liquid and vapor flows,
(2) the shim, which aligns and houses the manifolds and test chips,
(3) the manifold, which directs the liquid and vapor flow into the microchannels,
(4) the test chip with embedded heat sink and thin-film platinum resistance temperature detector (RTD) heater,
(5) the circuit board, which provides electrical connections to the test chip,
(6) the lid, which houses the circuit board and provides screw holes for clamping the assembly.

The internal flow path is shown in Fig. 4(*a*). Fluid enters through the liquid inlet in the header, where it is then fed into the manifold through the circular holes on the left and right sides of the manifold. The flow then passes through the microchannels to the outlet manifolds, where it is vertically vented and gathered into the outlet side of the header.

The header was machined from a solid block of stainless steel. The internal plumbing was drilled out of the block and welded closed. The shim was machined from high-temperature Teflon. The manifold was three-dimensional (3D) printed in alumina. Liquid- and vapor-side braces were needed for additional structural integrity in order to maintain parallel inlet and outlet channels after firing, as shown in Fig. 4(*b*). Braces were elongated in the direction of flow to minimize the disturbances to the flow. The alumina manifolds for the press-fit test section were lapped and polished to achieve 1 $\mu$m parallelism and 100 nm surface roughness in order to avoid microscopic gaps between the manifold and heat sink that could potentially adversely impact heat transfer and pressure drop [15,19]. The circuit boards were made of both glass, and the metal pattern screen-printed in the laboratory. The lid was machined from aluminum. A gasket was cut from Teflon and placed between the manifold and header to seal the liquid side from the vapor side, and to absorb and spread the screw-tightening force to prevent the chip, manifold, or circuit board from cracking during assembly. Viton O-rings were used for sealing and were placed in the O-ring grooves.

By contrast, the bonded FEEDS test section, shown in Fig. 3(*b*), consists of only two parts: (1) the electronic die with embedded microchannel heat sink and (2) the monolithic header manifold. The monolithic header manifold, shown in Fig. 5(*a*), was 3D printed from titanium and was designed to serve as a both header and manifold. The test chip is shown in Figs. 5(*b*) and 5(*c*) and is the same for both the press-fit and bonded FEEDS design.

There are many advantages of the bonded FEEDS design over the press-fit design. First, the header and manifold are 3D printed as one monolithic structure, and the microchannel fin tips and the manifold are directly bonded together, preventing the possibility of any flow bypassing the microchannels, which was shown in Refs. [15] and [19] to have a significant impact on pressure drop and heat transfer. Second, the use of additive manufacturing

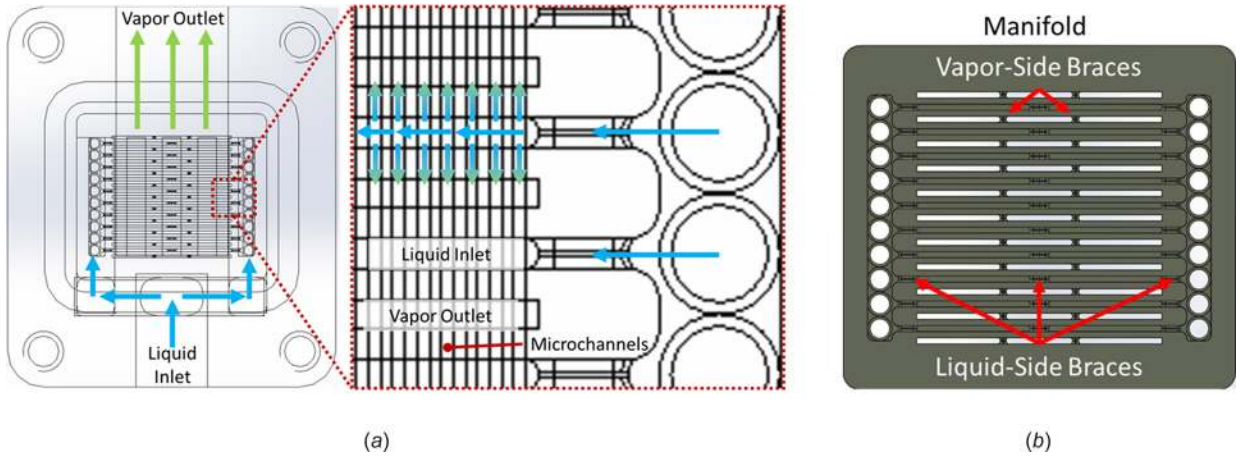


**Fig. 4 (*a*) Press-fit test section internal flow path and (*b*) press-fit manifold**

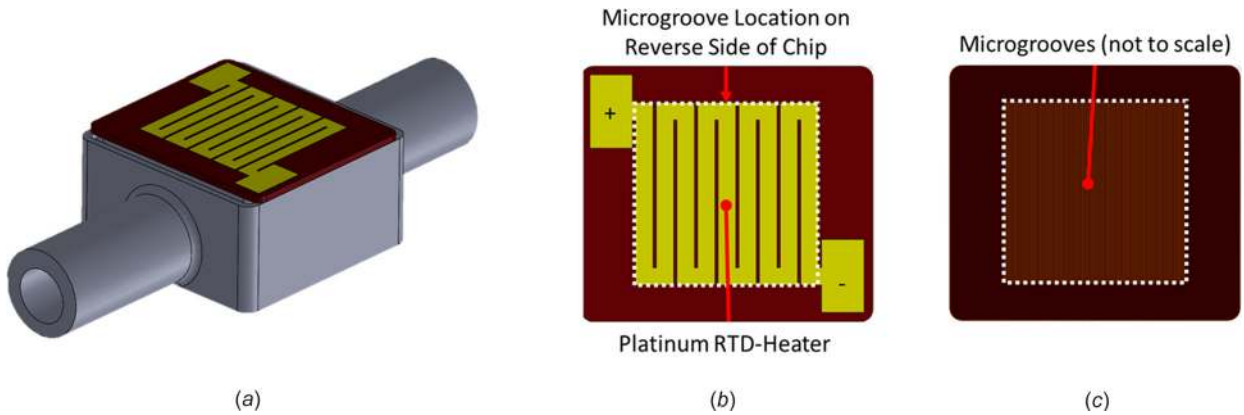


**Fig. 5 (*a*) Bonded FEEDS header manifold, (*b*) thin-film platinum RTD heater, and (*c*) DRIE embedded heat sink**

enables larger internal flow volume, which, in turn, improves intermicrochannel flow distribution. Finally, the overall volume of the manifold has been greatly reduced to allow for heat densities on the order of those required by the DARPA ICECool Fundamentals program (see Table 1).

The Si test chips were fabricated from a three-mask process on 0.5 mm thick substrates, while the SiC test chips were fabricated from 0.4 mm thick 4H polytype SiC substrates. First, a 440 nm/180 nm/440 nm thick oxide/nitride/oxide (ONO) stack was deposited in a low-pressure chemical vapor deposition furnace to electrically isolate the substrate from the future RTD heater. The ONO stack was then stripped from the microchannel side of the wafer, and the alignment marks were patterned on the remaining ONO stack. For SiC, 100 nm of Ti followed by 1 $\mu$m of Cu was evaporated using an e-beam evaporator and patterned using lift-off on the microchannel side; for Si, standard photoresists were patterned instead. The Cu and the photoresist formed the mask for the forthcoming deep reactive ion etch (DRIE) step to realize the grooves. The DRIE etch used sulfur hexafluoride ($SF_6$) and oxygen ($O_2$) as process gases. For SiC, the etch process was continuous with no intermediate cyclical polymerization step akin to those used in the standard silicon etch recipe. Etch time was approximately 80 min for SiC and approximately 50 min for Si.

Once the DRIE process was finished, the Cu mask and the photoresist were stripped, a new layer of photoresist was patterned, and 10 nm/400 nm Ti/Pt was sputtered uniformly. Next, using a lift-off process, the deposited metal layer was formed into a serpentine heater, which also functions as a RTD. The metal was annealed to 600 °C for 60 min, then ion milled to obtain a target resistance of 50 Ω. The heater side of the wafer was then coated with a protective layer of photoresist and diced. After dicing, the dies were stripped of photoresist, thereby completing the fabrication of Si/SiC test chips.

A diagram of the test loop used for both classes of test sections appears in Fig. 6. The test loop consists of a pump, a preheater, test section, test section isolation valves, condenser, and

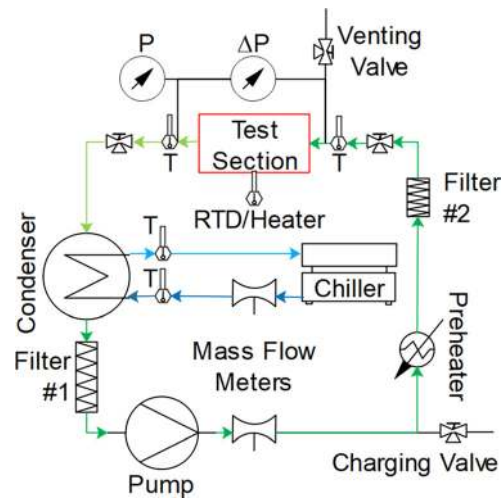


**Fig. 6 Test loop diagram**

**Table 3 Summary of equipment specifications and uncertainties**

| Equipment | Specifications | Uncertainty |
|---|---|---|
| Refrigerant Coriolis mass flow meter | 0–28 g/s | ±0.25% FS |
| Water-side Coriolis mass flow meter | 0–555 g/s | ±0.5% FS |
| Absolute pressure transducer | 0–100 psia | ±0.25% FS |
| Differential pressure transducer | 0–15 psig | ±0.25% FS |
| Pump | 0–1760 mL/min, 0–5 V control | n/a |
| Chiller | 2.41 kW | n/a |
| Power supply | 1.2 kW at 300 V and 4 A, 0–5 V control | n/a |
| Data acquisition system | Eight slot USB chassis | n/a |
| Voltage cDAQ card | 16ch, ±10 V, 100 kS/s | ±0.01% |
| Thermocouple cDAQ card | 16ch w/built-in cold junction compensation | ±0.8 °C |
| Voltage divider resistors | 1 and 30 MΩ, 0.5 W | ±1%, 200 ppm/°C |
| Platinum thin-film RTD heater | ∼62.5 Ω, 1 kW at 4 A | ±1 °C |
| Current-sense voltage transducer | ∼1 Ω, 16 W at 4 A | ±0.01% FS, 50 ppm/°C |

particulate filters. Instrumentation includes refrigerant and water-side mass flow rate measurements, absolute and differential pressure measurements on the test section, refrigerant inlet and outlet temperature measurements on the test section, water-side inlet and outlet temperature measurements on the condenser, and voltage drop and current measurements for the RTD temperature measurements. Table 3 summarizes the instrumentation, as well as the corresponding uncertainties, where applicable.

Since the platinum RTD is also functioning as a heater, the voltages were too large to be read directly by the data acquisition (DAQ) card. Accordingly, a voltage divider circuit was used to reduce the voltage from 300 V to less than 10 V, which could be directly read by the card. The voltage divider circuit is shown in Fig. 7(*b*). To ensure resistive heating and current losses would be reduced to negligible levels, 1 MΩ and 30 MΩ resistors were selected. The voltage divider was calibrated manually by applying a known voltage as an input and measuring the output voltage to eliminate the uncertainty in the manufacturer-specified nominal resistance values. Because of the high output impedance of this signal, a simultaneously sampling voltage card was required to prevent signal ghosting at the required high sampling frequencies. Three 3 Ω, 120 W low-temperature coefficient resistors were wired in parallel and served as a 1 Ω current-sensing voltage transducer with negligible self-heating effects. The current-sensing transducer was calibrated between 0 and 4 A to ensure that the transducer resistance did not increase significantly while dissipating the maximum heat load. Four-wire measurements were used for both RTD voltage drop and RTD current-sense measurements to ensure accurate voltage measurements.

The pump was controlled using a proportional–integral–derivative (PID) controller configured to supply the desired flow rates, ranging from 3 to 12 g/s. Chiller temperature was always set to 30 °C as a reference for fluid properties for comparisons to computational fluid dynamics simulations and to ensure that the condenser was always above room temperature for the two-phase tests. Therefore, the preheater, in conjunction with the outlet valve, was used to control inlet subcooling for two-phase tests. A 10 Ω coiled nichrome resistance-heater wire embedded into a Teflon tube served as a preheater. LabVIEW was used for all experimental monitoring, control, and data acquisition.

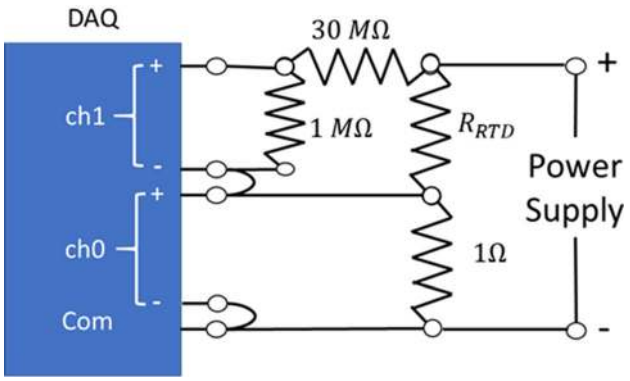


**Fig. 7 Voltage divider circuit**

The RTD-heater power supply was controlled in LabVIEW to ensure the fastest possible reaction time upon reaching critical heat flux or a thermal-runaway event. The RTD heater was controlled in LabVIEW using an analog output card. RTD temperature was sampled at ∼100 Hz to check whether it exceeded the preset temperature limit. Upon exceeding this limit, the power supply would be turned off to prevent overheating and damage from critical heat flux. The power supply would then remain off until a reset button was engaged to prevent the control system from rapidly reengaging and disengaging the power upon RTD temperature dropping below and exceeding the limit.

For the press-fit test section, the chip was first soldered to the glass circuit board before assembly. A solder alignment tool was machined out of aluminum to hold and align the chip and circuit board. The test chip was placed in the recess in the center of the tool, and then the circular circuit board was placed into the groove on top of the chip. An Sn3.5Ag eutectic solder (liquidus point of 221 °C) paste syringe was used to deposit a controllable and minute amount of solder onto the chip leads. After solder was deposited and a satisfactory alignment was achieved, the solder alignment tool was placed onto a preheated hotplate set to 300 °C. Metal tongues were used to apply force to the circuit board to enhance thermal contact and ensure complete solder coverage on the pads. Pressure was applied until there was visual confirmation that the solder had melted, after which, the alignment tool was removed from the hot plate and placed on an aluminum heat sink. Pressure was applied to minimize the gap between chip and board. After the solder had solidified, the board was hastily removed from the alignment tool to prevent potential damage to the chip resulting from the glass from becoming stuck in place due to thermal contraction of the aluminum tool.

For the bonded test sections, the test chip first had to be bonded to the manifold. The 3D printed manifold was first polished using fine grit sandpaper. The test chips and manifolds were then loaded into a sputtering machine, where the oxide layers were removed from the manifolds using a 10 min reverse sputtering process. A thin adhesion layer of Ti was then deposited, followed by a 100 nm thick Ni diffusion barrier layer, and finally a 2 $\mu$m thick layer of Ag. The chips and manifolds were then loaded into an e-beam evaporator, where 2 $\mu$m of Sn was deposited, followed by a thin layer of Ag to prevent oxidation. The e-beam evaporator was used for Sn deposition due to the slow sputtering rates of Sn. For all cases, solder was applied to both the chip and the manifold. The chips were then bonded to the manifolds using a specially designed bonding device and procedure described in Refs. [15] and [18]. The bonding device was designed to uniformly and

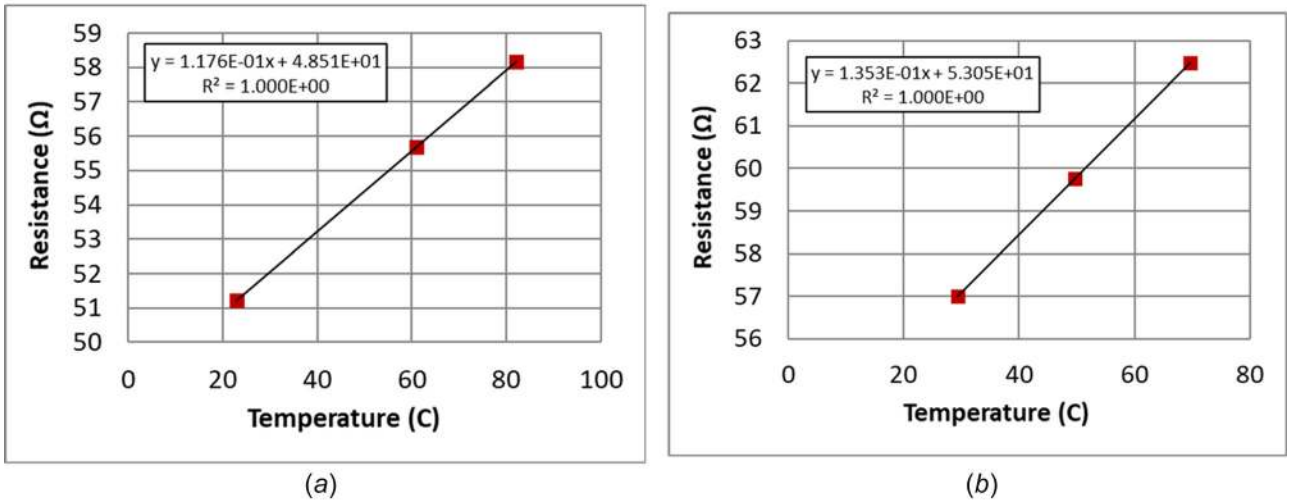


**Fig. 8 Calibration curves for (*a*) chip 1 (Si) and (*b*) chip 2 (SiC)**

conformally clamp the test chip onto the manifolds. Test chips were pressurized to 150 psig and submerged underwater to ensure leak tightness before testing.

The assembled test section was placed into the loop, evacuated from air, and charged with R245fa for RTD calibration. A PID-controlled pump was used to supply approximately 6 g/s of flow, while the PID-controlled preheater was used to heat the fluid to a desired temperature. Upon reaching steady-state, the RTD resistance was measured and calibrated using the thermocouples placed at the outlet of the test section. A battery was used to apply a 10 mA test current to measure resistance, producing less than 5 mW of power dissipation and resulting in a negligible amount of RTD self-heating due to the embedded heat sink. Three sampling points were taken to assess linearity. The obtained calibration curves for both chips are given in Fig. 8. Both curves were observed to be linear. Uncertainties in RTD temperature readings from resistance and thermocouple temperature measurement errors totaled to a maximum of ±1 °C.

## 4 Data Reduction

The heat load is calculated from Ohm's law

$$q'' = I^2 R_{\text{RTD}}/A_{\text{base}} \tag{1}$$

where $A_{\text{base}}$ is the base area of 1 cm$^2$.

The base superheat is defined as the temperature rise above the refrigerant saturation temperature

$$\Delta T_{\text{base}} = T_{\text{base}} - T_{\text{sat}} \tag{2}$$

where $T_{\text{base}}$ is the RTD temperature and $T_{\text{sat}}$ is the saturation temperature and is determined by computing the static pressure of the inlet and outlet of the microchannel and averaging the corresponding saturation temperatures

$$T_{\text{sat}} = \frac{T_{\text{sat}}(P_{\text{ch,in}}) + T_{\text{sat}}(P_{\text{ch,out}})}{2} \tag{3}$$

The static pressure in the inlet of the microchannel is computed using the Bernoulli equation, accounting for the change in area and the pressure loss due to contraction

$$P_{\text{ch,in}} = P_1 + \frac{1}{2}\rho_l v_1^2 - \frac{1}{2}\rho_l v_{\text{in}}^2(1 + K_c) \tag{4}$$

where $P_1$ is the measured static pressure at the inlet of the test section.

The contraction coefficient, $K_c$, can be determined from [20]

$$K_c = 0.42(1 - \sigma^2) \tag{5}$$

$$\sigma = \frac{w_{\text{ch}}}{w_{\text{ch}} + w_f} \tag{6}$$

and the velocities $v_1$ and $v_{\text{in}}$ can be determined from mass balance and the appropriate areas

$$v_1 = \frac{\dot{m}}{\rho_l A_1} \tag{7}$$

$$v_{\text{in}} = \frac{\dot{m}}{\rho_l A_{\text{in}}} \tag{8}$$

$$A_1 = \frac{\pi D_1^2}{4} \tag{9}$$

$$A_{\text{in}} = N_{\text{ch}} w_{\text{ch}} L_{\text{in}}/2 \tag{10}$$

$$N_{\text{ch}} = \frac{A_{\text{base}}}{(w_{\text{ch}} + w_f)L_{\text{ch}}} \tag{11}$$

Similarly, the static pressure in the outlet of the microchannel can be computed as

$$P_{\text{ch,out}} = P_2 + \frac{1}{2}\rho_2 v_2^2 + \frac{1}{2}\rho_{\text{out}} v_{\text{out}}^2(K_e - 1) \tag{12}$$

where $P_2$ is the measured static pressure at the test section outlet, $\rho_2$ is the density of the two-phase mixture at the outlet of the test section, $\rho_{\text{out}}$ is the two-phase mixture density at the outlet of the microchannel, $v_2$ and $v_{\text{out}}$ are the appropriate velocities at the outlet of the test section and outlet of the microchannel, respectively, and $K_e$ is the expansion loss coefficient.

The density of the two-phase mixture at the outlet of the test section, $\rho_2$, can be assumed to be homogenous, due to the presence of entrained liquid droplets in the flow

$$\rho_2 = (1 - \alpha_H)\rho_l + \alpha_H \rho_v = \frac{1}{\left(\frac{(1 - X_{\text{out}})}{\rho_l} + \frac{X_{\text{out}}}{\rho_v}\right)} \tag{13}$$

where $\alpha_H$ is the homogenous vapor void fraction given by

$$\alpha_H = \frac{1}{1 + \frac{1 - X_{\text{out}}}{X_{\text{out}}} \frac{\rho_v}{\rho_l}} \tag{14}$$

The density of the two-phase mixture at the outlet of the microchannel, $\rho_{\text{out}}$, can be assumed to be computed from the area-weighted average of the liquid and vapor densities assuming annular flow. For annular flow, the Zivi annular void fraction correlation can be used, and is of the form

$$\alpha_Z = \frac{1}{1 + \frac{1 - X_{\text{out}}}{X_{\text{out}}} \left(\frac{\rho_v}{\rho_l}\right)^{2/3}} \tag{15}$$

Accordingly, the two-phase mixture density of the outlet of the microchannel can be computed as

$$\rho_{\text{out}} = (1 - \alpha_Z)\rho_l + \alpha_Z \rho_v \tag{16}$$

The expansion loss coefficient, $K_e$, can be computed as [20,21]

$$K_e = (1 - \sigma)^2 \tag{17}$$

Finally, the velocities, $v_2$ and $v_{\text{out}}$, can be computed using the appropriate areas and densities

$$v_2 = \frac{\dot{m}}{\rho_2 A_2} \tag{18}$$

$$v_{\text{out}} = \frac{\dot{m}}{\rho_{\text{out}} A_{\text{out}}} \tag{19}$$

$$A_2 = \frac{\pi D_2^2}{4} \tag{20}$$

$$A_{\text{out}} = N_{\text{ch}} w_{\text{ch}} L_{\text{out}}/2 \tag{21}$$

The base heat transfer coefficient is defined as

$$U_{\text{base}} = q''/\Delta T_{\text{base}} \tag{22}$$

The fin heat transfer coefficient is defined by removing the thermal conductances of the oxide-nitride-oxide layer height, $h_{\text{SiO}_2}$, and silicon or silicon-carbide substrate base height, $h_b$, as

$$U_{\text{fin}} = \left(\frac{1}{U_{\text{base}}} - \frac{h_{\text{SiO}_2}}{k_{\text{SiO}_2}} - \frac{h_b}{k_S}\right)^{-1} \tag{23}$$

The wall heat transfer coefficient can be computed from the fin heat transfer coefficient using the fin efficiency equations

$$U_{\text{wall}} = U_{\text{fin}} \frac{w_{\text{ch}} + w_f}{2\zeta h_f} \tag{24}$$

$$\zeta = \frac{\tanh(m h_f)}{m h_f} \tag{25}$$

$$m = \sqrt{\frac{2U_{\text{wall}}}{k_S w_f}} \tag{26}$$

The temperature dependence of thermal conductivity of the substrates was accounted for by assuming the following relationship [22]:

$$k_S = \frac{a}{(273.15 + T)^n} \tag{27}$$

where $T$ is in °C, and $a = 3.037 \times 10^5$(W/m K) and $n = 1.334$ for silicon [22,23]. For SiC, a constant value of $k = 390$ W/m K given by the manufacturer data sheet was used due to the lack of reliable temperature dependent data on 4H-SiC. The thermal resistance of the nitride layer was neglected, due to its relatively thinner length and significantly higher thermal conductivity.

Finally, thermodynamic outlet vapor quality is calculated from

$$X_{\text{out}} = \frac{q'' A_{\text{base}} - \dot{m} C_{p,l} \Delta T_{\text{sub}}}{\dot{m} \Delta h_{\text{lv}}} \tag{28}$$

where the subcooling, $\Delta T_{\text{sub}}$, is defined as temperature difference between saturation and inlet

$$\Delta T_{\text{sub}} = T_{\text{sat}} - T_{\text{in}} \tag{29}$$

All data analysis was conducted in MATLAB, using a custom script to load each test data file, temporally average the values in the data file, propagate errors using finite differences, and plot the results. Uncertainty was propagated using the standard formula, given here in index notation

$$\Delta U_j = \sqrt{\sum_i \left(\frac{\partial U_j}{\partial x_i} \Delta x_i\right)^2} \tag{30}$$

where $U_j$ is a value calculated from one of the above equations for which uncertainty propagation is desired—for example, Eqs. (1)–(29)—and $x_i$ is a measured variable with a given uncertainty—for example, $R_{\text{RTD}}, I, T_{\text{RTD}}, T_{\text{in}}, P_1, P_2,$ and $\dot{m}$. To obtain the partial derivatives, finite differences were used.

## 5 Results and Discussion

The experimental results of two test chips are reported here, the first chip being made from Si and having been tested using the press-fit test section, and the second chip having been made from SiC and directly bonded to the header manifold. Scanning electron microscopy (SEM) measurements were taken for both the chips and their manifolds. Chip dimensions were measured using cross section of the chips after testing was completed. The bonded chip was first debonded before being cross-sectioned. Details of bonding and debonding are given in Refs. [15], [17], and [18].

A summary of the SEM measurements of the two chips and manifolds is given in Table 4. The geometric variables are defined in Fig. 2(*b*).

Pressure drop and base temperature measurements were performed at up to four different mass flow rates—3, 6, 9, and 12 g/s—and heat flux increased until surface temperature exceeded 100 °C. For all tests, chiller temperature was held close to 30 °C, and an inlet subcooling of less than 5 °C was maintained

**Table 4 Summary of measured dimensions from SEM cross sections [24,25]**

| Dimension, variable (units) | Chip 1 | Chip 2 |
|---|---|---|
| Die material | Si | SiC |
| Microchannel width, $w_{\text{ch}}$ ($\mu$m) | 9 | 8.5 |
| Microchannel fin width, $w_f$ ($\mu$m) | 11 | 11.5 |
| Microchannel fin height, $h_f$ ($\mu$m) | 105 | 50 |
| Substrate base thickness, $h_b$ ($\mu$m) | 405 | 350 |
| Manifold type | Press-fit | Bonded |
| Manifold inlet, $L_{\text{in}}$ ($\mu$m) | 285 | 200 |
| Manifold wall, $L_{\text{man}}$ ($\mu$m) | 235 | 300 |
| Manifold outlet, $L_{\text{out}}$ ($\mu$m) | 300 | 230 |

for consistency. When possible, all tests were performed twice to assess repeatability. Heat losses were measured by restricting coolant flow and applying power to the chip until the RTD temperature reached 100 °C. For the chips tested here, less than 5 W of heating was required, and accordingly, heat losses are negligible and were therefore not included in the data analysis. Due to the reduced fin height of chip 2, pressure drops were higher than anticipated, and flowrates above 9 g/s were not tested to avoid overloading the differential pressure transducer. However, a pressure isolation valve was installed to isolate the differential pressure transducer to enable the continuation of tests at high vapor qualities. Thus, some pressure drop measurements for chip 2 are not available. Nevertheless, due to the linear dependence of pressure drop with vapor quality, the pressure drop can be extrapolated to estimate the average microchannel static pressure computed in Eq. (3).

Figure 9 shows the graph of base heat flux through the chip footprint versus RTD superheat for both chips. It is observed that for low base heat fluxes, a higher mass flow rate will require a higher superheat for the same heat flux. This trend is due to the dependence of wall heat transfer coefficient on vapor quality: for the same base heat flux, a higher mass flow rate will operate at a lower outlet vapor quality, and therefore, the wall heat transfer coefficient will be lower, resulting in a higher surface superheat. In addition, a steep change in slope is observed for each of the mass flow rates, which implies a steep reduction in wall heat transfer coefficient, which will be discussed in more detail below.

Figure 10 shows the relationship between wall heat transfer coefficient and outlet vapor quality. Note that the uncertainties for heat transfer coefficient are higher for experimental data points at lower outlet vapor qualities due to small $\Delta T_{sat}$ present at low heat fluxes. For low vapor qualities, an increase in vapor quality results in an increase in wall heat transfer coefficient for all flow rates and chips. This is due to two independent factors. First, increasing vapor quality requires an increase in average wall heat flux, which in turn, increases surface superheat. This increase in surface superheat increases the efficiency of the nucleate boiling process, resulting in an increased wall heat transfer coefficient [26]. Second, it was shown in Ref. [15] that for these narrow channels, direct conduction through the liquid film can produce heat transfer coefficients the same order of magnitude as those reported here. Accordingly, as vapor quality increases, void fraction increases, resulting in a thinner liquid film and an increased wall heat transfer coefficient. However, as vapor quality increases further, wall heat transfer coefficient is observed to peak and then decrease. It was shown in Refs. [15] and [27] that due to the asymmetric feeding and heating present in FEEDS manifold microchannels, a region of dry out tends to form underneath the outlet. As vapor quality increases, this region of dry out increases, and eventually acts to reduce wall heat transfer coefficient, resulting in the optimal vapor qualities that were observed. For the case of chip 2, the observed reduction in heat transfer coefficient past this optimal vapor quality is extremely steep, indicating an unstable and rapidly receding liquid film. However, as vapor quality is increased further, heat transfer coefficient was observed to remain constant, indicating the regaining of a stable liquid film.

In addition, for the same outlet vapor quality, wall heat transfer coefficient is observed to increase with increasing mass flow rate. This is partially due to the increased surface superheat required to obtain the same vapor quality at a higher mass flow rate, which, in turn, improves the nucleate boiling process and increases wall heat transfer coefficient [26]. Furthermore, using a momentum balance, it was shown in Ref. [15] that at the same vapor quality, a higher mass flux will produce a higher vapor void fraction and thinner liquid film. Thus, increasing mass flow rate also increases wall heat transfer coefficient by reducing the average liquid film thickness.

Similar to Cetegen [3] and others [11,12], an optimal vapor quality was found, at which increases to vapor quality resulted in reduced heat transfer coefficient. Thus, each heat flux will have an optimal flow rate that would produce a maximum heat transfer coefficient and minimum base temperature. Furthermore, unlike previous experimental two-phase results where optimal vapor qualities were between 10% and 20% [3] or 2.5–12.5% [11], in the present work, optimal vapor qualities were found to be between 30% and 50% for the two tested chips. This is due to the increased ratio of flow length underneath the manifold wall ($L_{man}$) relative to the height of the fin ($h_f$): when the manifold wall length is significantly larger than the height of the channel, the manifold-microchannel system becomes closer to a straight microchannel, which tends to have optimal vapor qualities in excess of 75% [28]. In addition, this is also responsible for the slightly increased wall heat transfer coefficients of the SiC chip compared to the Si chip: while the Si chip has a 2:1 ratio between flow length underneath the manifold and height of the fin, the SiC chip, due to its shorter fin height, has a 6:1 ratio.

Figure 11 shows the relationship between total pressure drop and outlet vapor quality. Referring to Fig. 11, it is clear that for a given flow rate, increasing the heat flux, and therefore the vapor quality, results in an increased pressure drop. This is because the velocity of the two-phase mixture increases faster than the two-phase viscosity decreases, resulting in an increased pressure drop. It is worth noting that the drop in total pressure is plotted here to eliminate the effect of the pressure drop due to the acceleration of the two-phase mixture as the vapor quality increases. In addition, it was noted that at the same vapor quality, a higher mass flow rate will have a higher pressure drop, since a higher mass flow

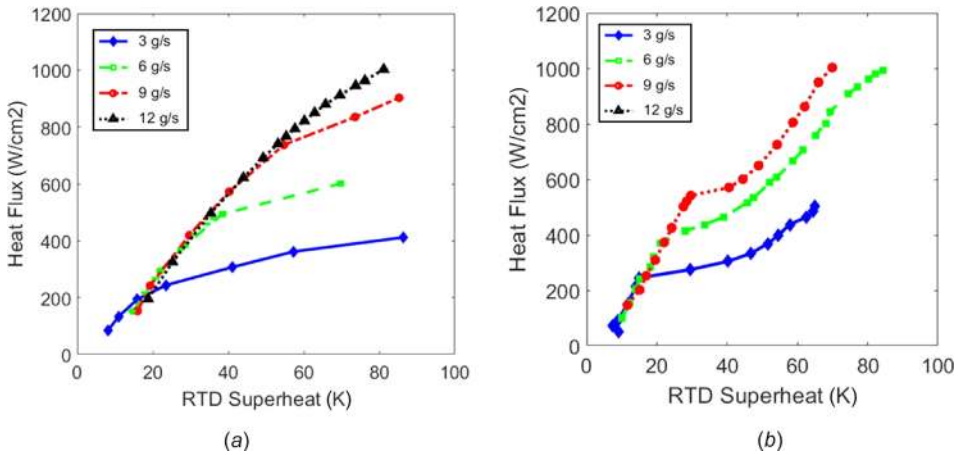


**Fig. 9 Base heat flux versus RTD superheat for (*a*) chip 1 and (*b*) chip 2**

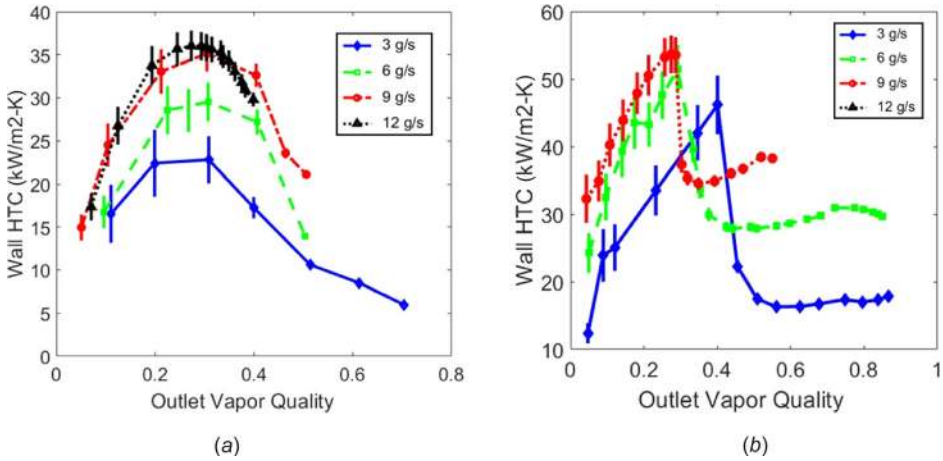


**Fig. 10 Wall heat transfer coefficient versus outlet vapor quality for (*a*) chip 1 and (*b*) chip 2**

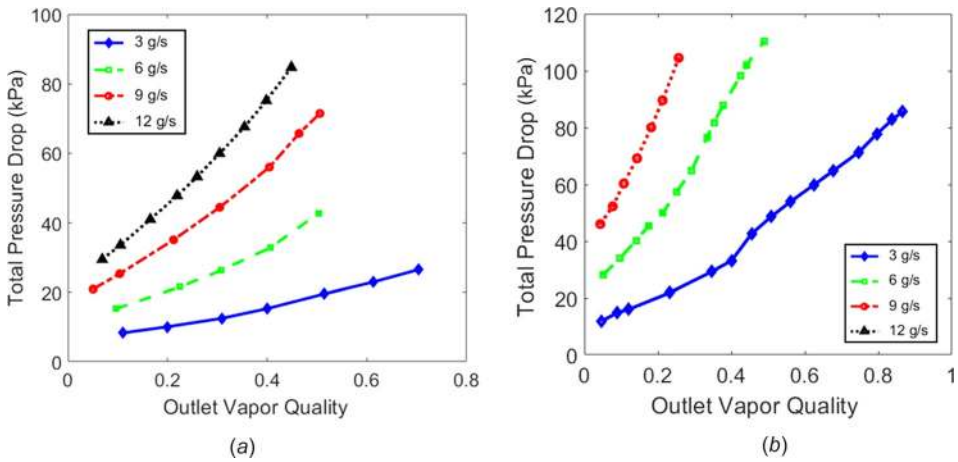


**Fig. 11 Pressure drop versus vapor quality for (*a*) chip 1 and (*b*) chip 2**

rate will have a higher velocity at the same vapor quality. As expected, the pressure drops for chip 2 are notably higher than chip 1 due to the reduced channel depth. Due to the increase in the pressure drop for chip 2, it is worth noting that the differential pressure transducer had to be isolated to prevent damage. Thus, the pressure drop measurements for the points are not available above a vapor quality of ~50%.

Finally, the results show that for the press-fit setup, stable operation at heat fluxes in excess of 1 kW/cm$^2$ was obtained at outlet qualities near 45%, total pressure drops below 90 kPa, and a COP—defined as $Q/(\dot{m}\Delta P/\rho_l)$—of nearly 1400. Meanwhile, the bonded test section was able to achieve, a peak heat flux of 1 kW/cm$^2$ and heat density of 490 W/cm$^3$ (1000 W in a volume of 1.6 cm × 1.6 cm × 0.8 cm) at a vapor quality of 85%. Thus, for the first time, both the heat flux and outlet vapor quality metrics imposed by DARPA ICECool Fundamentals have been achieved simultaneously. In order to meet the ICECool metrics for heat density, the manifold size will have to be reduced without sacrificing flow maldistribution.

## 6 Conclusions

Two embedded microcoolers utilizing FEEDS were designed, calibrated, and tested in a two-phase heat transfer/fluid flow mode. The first chip was made from silicon and was tested in a press-fit FEEDS test section, while the second chip was made from SiC and was tested in a bonded FEEDS test section. For both chips, heat transfer and pressure drop measurements were performed, and the results characterized. With the press-fit Si test chip, heat fluxes in excess of 1 kW/cm$^2$ were obtained at vapor qualities approaching 45% and a coefficient of performance approaching 1400. With the bonded SiC test chip, heat fluxes in excess of 1 kW/cm$^2$ were achieved at a vapor quality of 85% and heat densities approaching 490 W/cm$^3$. In addition, behaviors of pressure drop and heat transfer coefficients were examined and explained in regard to surface superheat, vapor quality, mass flux, and liquid film thickness. Performance differences between the press-fit Si versus the bonded SiC were caused by the geometrical differences in the ratio of flow length to the height of the fin. In comparison to FEEDS geometries studied in previous works, both of the tested chips displayed higher optimum vapor qualities in the range of 30–50%, as opposed to 10–20% in previous studies, due to the higher ratios, signifying the importance of geometrical parameters on the performance of FEEDS cooler.


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## Nomenclature

$A_{base}$ = base area (m$^2$)
$A_{in}$ = microchannel inlet area (m$^2$)
$A_{out}$ = microchannel outlet area (m$^2$)

$C_p$ = specific heat (J kg$^{-1}$ K$^{-1}$)
COP = coefficient of performance, $Q/(\dot{m}\Delta P/\rho_l)$
$h_b$ = height of the substrate base (m)
$h_f$ = height of the fin (m)
$h_{SiO_2}$ = height of the glass layer (m)
$I$ = electrical current (A)
$k$ = thermal conductivity (W m$^{-1}$ K$^{-1}$)
$K$ = dynamic pressure loss coefficient
$L_{ch}$ = length of the microchannel, $L_{in}/2 + L_{man} + L_{out}/2$ (m)
$L_{in}$ = length of the inlet (m)
$L_{man}$ = length of the manifold (m)
$L_{out}$ = length of the outlet (m)
$m$ = fin efficiency parameter (m$^{-1}$)
$\dot{m}$ = refrgierant mass flow rate (kg s$^{-1}$)
$N_{ch}$ = number of microchannels
$P$ = pressure (Pa)
$q''$ = heat flux (W m$^{-2}$)
$R_{RTD}$ = RTD electrical resistance (Ω)
$T$ = temperature (K)
$U$ = heat transfer coefficient (W m$^{-2}$ K$^{-1}$)
$v$ = velocity (m s$^{-1}$)
$w_{ch}$ = width of the channel (m)
$w_f$ = width of the fin (m)
$X$ = vapor quality

## Greek Symbols

$\alpha_H$ = homogenous void fraction
$\alpha_Z$ = Zivi void fraction
$\Delta h_{lv}$ = latent heat of vaporization (J kg$^{-1}$)
$\zeta$ = fin efficiency
$\rho$ = density (kg m$^{-3}$)
$\sigma$ = pressure loss parameter

## Subscripts

$c$ = contraction
ch = microchannel
$e$ = expansion
in = inlet
fin = microchannel fin
$l$ = liquid
man = manifold
out = outlet
ref = reference
$s$ = substrate
sat = saturation
sub = subcooling
$v$ = vapor

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