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EMI Mitigation With Multilayer Power-Bus Stacks and via Stitching of Reference Planes

Xiaoning Ye, David M. Hockanson, Min Li, Yong Ren, Wei Cui, James L. Drewniak, and Richard E. DuBroff

Abstract—**General methods for reducing printed circuit board (PCB) emissions over a broad band of high frequencies are necessary to meet EMI requirements, as processors become faster and more powerful. One mechanism by which EMI can be coupled off a PCB or multichip module (MCM) structure is from high-frequency fringing electric fields on the dc power and reference planes at the substrate periphery. An approach for EMI mitigation by stitching multiple ground planes together along the periphery of multilayer PCB power-bus stacks with closely spaced vias is reported and quantified in this paper. Power-bus noise induced EMI and coupling from the board edges is the major concern herein. The EMI at 3 m for different via stitch spacing and layer thickness is modeled with the finite-difference time domain (FDTD) method. Design curves and an empirical equation are extracted from a parametric study to summarize the variation of the radiated EMI as a function of layer thickness and stitch spacing.**

Index Terms—**DC power bus, EMI mitigation, Finite-difference time domain, fringing electric fields, via stitching.**

I. Introduction

ELECTRONIC devices continue to operate at increasing speeds and consume more power, which significantly increases EMI concerns and makes it more challenging to meet the radiated emissions requirements. There are a number of theories as to how radiated emissions result from printed circuit boards (PCBs). Possible radiation mechanisms include coupling from the traces (microstrip structures) [1], [2], dipole-like radiation from a PCB with attached cables [3], multi-board configurations driven by an effective noise source at the connection [4], direct radiation from components or heatsinks on PCBs [5], [6], [7], or direct radiation from the power bus [8]. The transient currents of present high-speed devices can be on the order of tens of amps, which may result in significant voltage fluctuations on the power bus [9]. As a result, power-bus noise has become a major concern for EMC engineers in printed circuit board (PCB) designs.

Multilayer power-bus stacks, viz., using multiple power/ground plane sets for dc power, are common scenarios in PCB designs, where the power plane and ground planes are typically of appreciable electrical extent, and may function as radiators or effective coupling paths at high frequencies [1], [3], [10], [11]. More specifically, for multilayer structures with entire power and ground layers, the power and ground plane pair is essentially a radiating microstrip-patch antenna, where radiation occurs as a result of the fringing electric field at the board edges [12]. Alternatively, these fringing fields can couple to enclosure modes, or directly couple to slots and apertures, and result in radiation. Recent work for mitigating radiation from the edge of PCBs utilizes resistive termination along the board edges to reduce the resonance peaks [13]. For power-bus geometries with multiple power/ground plane pairs or ground planes, stitching the ground planes together at the periphery of the board using closely spaced vias can effectively shield the board edges, and reduce the level of the radiation that results from the fringing fields. Although this concept is already often applied in practice, little work has been done regarding the effectiveness of ground plane stitching and quantifying the via spacing. Consequently, the integrity of the via-stitch spacing is not always maintained in board areas of high design density, and the EMI effectiveness of the approach is compromised. One recent study of ground-plane stitching could be found in [14]. Other reported via stitching works include controlling the cross talk between PCB traces by applying a double row of plated hole vias adjacent to the microstrip trace [15], or placing via fences on both sides of the stripline and studying their effects on the coupling between adjacent striplines [16], [17].

The studies presented herein focuses on the impact of ground plane stitching on radiated EMI. A direct approach of performing an effective study on the EMI consequences of the ground plane stitching is to conduct a series of EMI measurements in a chamber. However, this requires sophisticated measurement facilities, and construction of numerous boards for a parametric study. Throughout this work, finite-difference time domain (FDTD) modeling is used as an alternative method [18], and radiated EMI at 3 m for various power-bus structures is computed through the numerical modeling. The modeled results are analyzed to provide insight into relevant physics, and to develop design guidelines for via stitching of ground layers.

In Section II, the effectiveness of the FDTD method in modeling power-bus problems is demonstrated by comparing the modeled results with the measurements for two modeling examples, which contain the basic geometries of interest in the

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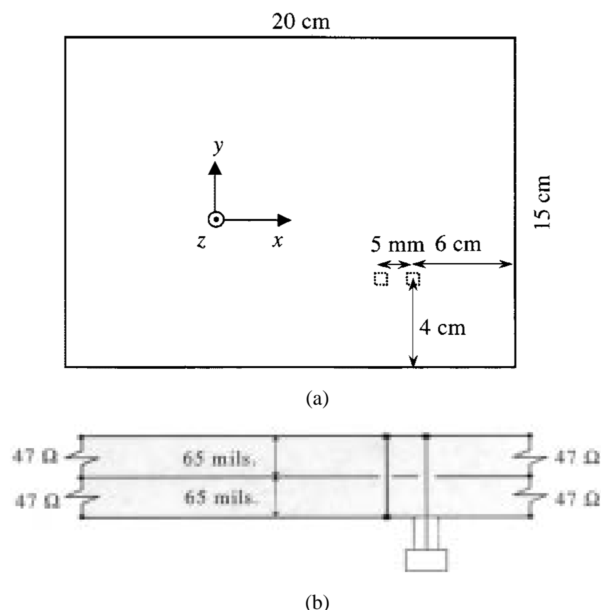


Fig. 1. Geometry of the three-layer test board for the FDTD study. (a) Top view. (b) Side view.

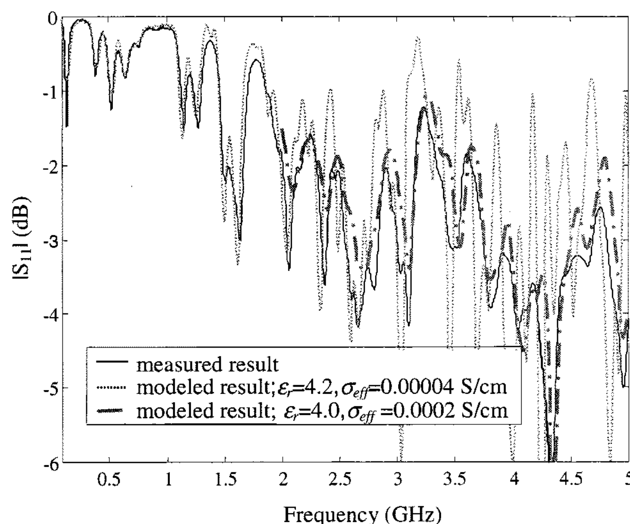


Fig. 2. FDTD modeled and measured $|S_{11}|$ for the configuration shown in Fig. 1.

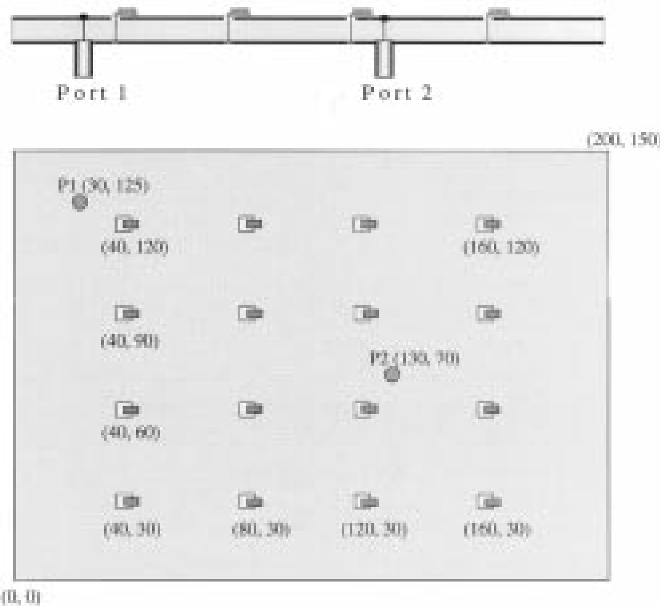


Fig. 3. Schematic of the test board with 16 decoupling capacitors—side view and top view. All dimensions are in millimeters (mm).

power-bus problems. In the next section, the FDTD method is used to investigate the functional variation of the radiated EMI as compared to the thickness of the power-bus stack. A parametric study is then conducted in Section IV, by evaluating the radiated EMI of typical multilayer power-bus stacks with different ground plane via-stitch spacings and different layer thicknesses. The studied power-bus stacks have either a GND-PWR-PWR-GND or a GND-PWR-GND-PWR layer stack-up, where PWR denotes a voltage plane. Two families of design curves are extracted to provide quantitative direction for EMI mitigation of this particular radiation mechanism, and an empirical design equation is then extracted. In Section V, the effects of nonuniform stitch spacing are considered. This study focuses primarily on applications to PCB design, but may be applicable to other substrate types such as multichip modules (MCMs) as well.

II. FDTD Modeling in DC Power-Bus Design

A reliable power-bus modeling approach is a powerful tool that can be integrated into the design procedure to provide design insight, and can be used for developing design guidelines. For complex designs of PCBs, e.g., boards with a significant number of SMT capacitors, or boards with segmented power or ground planes, the number of unknowns for traditional frequency-domain methods may increase significantly, and computation can be rather time and memory consuming. The important advantage of the FDTD method is that it allows straightforward extension of the method to more complicated layouts and multiple number of layer structures with only a modest increase in the computational domain. Here, FDTD modeling is used, since multiple frequencies can be analyzed with a single time-domain simulation, and it is well suited for a rectilinear geometry.

Two modeling examples are presented first in this section to experimentally demonstrate the FDTD method for modeling multilayer PCB structures. The first example is a three-layer board which contains the geometry of a via penetrating a complete plane. The board was constructed by compressing a double-sided PCB and a single-sided PCB together, as shown in Fig. 1. The dimension of the PCB was 15 cm × 20 cm, with a 65-mil layer spacing FR4 dielectric. The signal was fed by a 0.085″ semi-rigid coaxial cable with an SMA connector. The feeding point was 6 cm away from the short edge, and 4 cm away from the long edge of the ground plane. Two square apertures were cut in the middle plane by removing the copper cladding, so that signal and return pins penetrated the middle plane without electrically contacting it. The size of both apertures was 1.5 mm × 1.5 mm. The radius of the wire connecting the top and bottom planes was 12 mil. At each of the four board corners, two 1206 SMT resistors were soldered

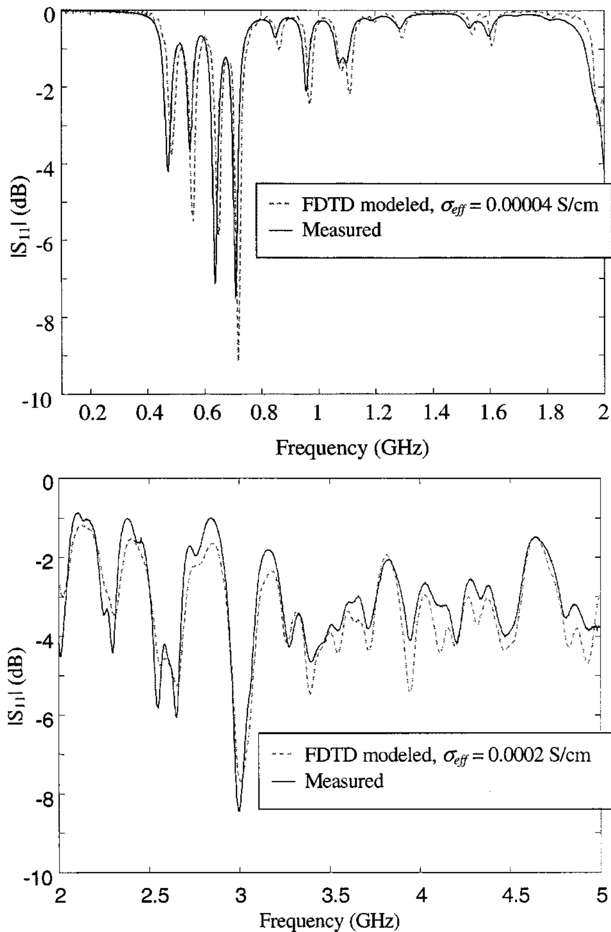


Fig. 4. Measured and FDTD modeled $|S_{11}|$ for the two-layer board with 16 decoupling capacitors.

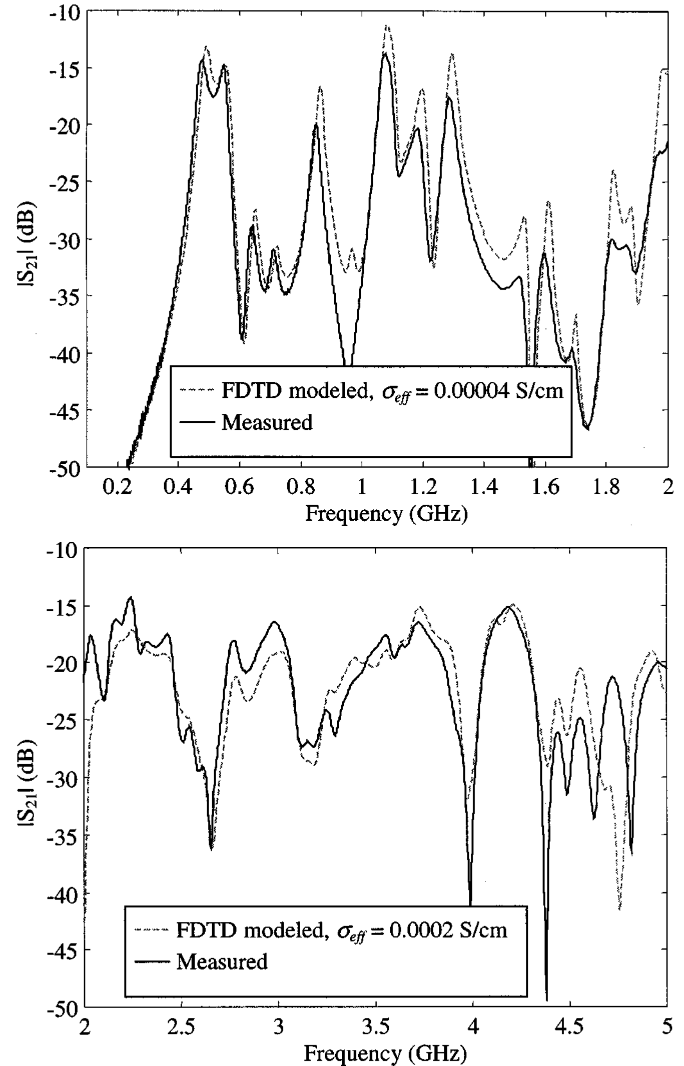


Fig. 5. Measured and FDTD modeled $|S_{21}|$ for the two-layer board with 16 decoupling capacitors.

to the planes, with one soldered to the middle and top plane, and the other soldered to the middle and bottom plane. The purpose of these resistors was to reduce the artificially high Q of the parallel plane resonances at frequencies below 2 GHz, though this is not entirely necessary.

The $|S_{11}|$ of the test board was measured using an HP 8753D network analyzer and compared to the FDTD modeled results. In the FDTD modeling, the cell size was chosen as 1 mm×1 mm×0.55 mm (x, y, z), and each aperture in the middle plane was approximated with four cells (therefore, the size of the aperture was 2 mm × 2 mm in the modeling). Both the dielectric loss and conductor (skin effect) loss can impact the Q value of the parallel plane mode resonances at higher frequencies. Using the formulas for calculating quality factor of a microstrip patch antenna as given in [12], the dielectric loss was determined to be the dominant factor for this configuration and was included in the numerical modeling, while the skin effect loss can be neglected. Although incorporating a frequency-dependent dielectric loss in the modeling is feasible, a simpler approach was taken by dividing the studied frequency range in half and using a uniform effective dielectric conductivity in each range [19]. For this particular problem, the effective conductivity of the dielectric material determined by matching experimental and FDTD results on a two-layer structure of similar material was 0.000 04 and 0.0002 S/cm over the frequency range 100 MHz–2 GHz, and 2–5 GHz, respectively. An effective conductivity of 0.000 04 S/cm is equivalent to a loss tangent of 0.0245 at 700 MHz for a relative dielectric constant of $\varepsilon_r = 4.2$, while an effective conductivity of 0.0002 S/cm is equivalent to a loss tangent of 0.0245 at 3.5 GHz. The source in the modeling was a sinusoidally modulated Gaussian voltage source with a source impedance of 50 Ω. Since the response of the feeding semi-rigid coaxial cable was removed in the measurement calibration procedure, the voltage source in the modeling was applied vertically above the ground plane in the FDTD modeling, which was a complete plane in the model. All three planes were modeled as perfect electric conductors (PECs) of zero thickness. The wire structures were modeled using a thin wire algorithm [20], and the resistors were modeled as lumped elements [21], with the encircling magnetic field components modified in a fashion similar to the thin wire case. Eight perfectly matched layers (PML) were placed at each boundary plane of the computational domain [22], and seven white-space layers were placed between the PML and the

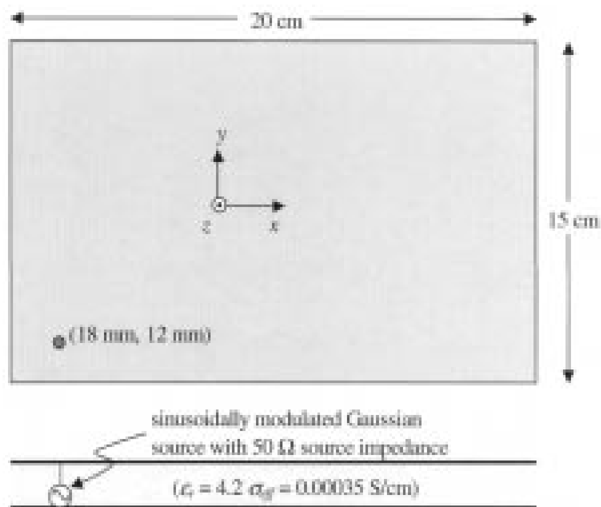
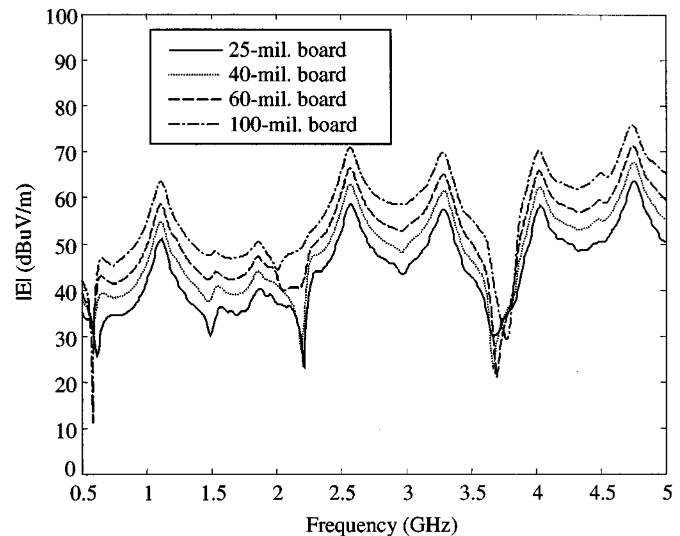
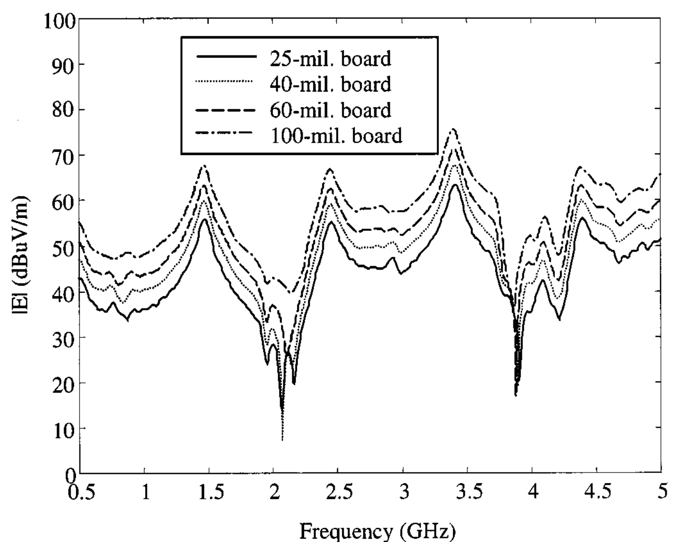


Fig. 6. Schematic of the PWR-GND two-layer board used for FDTD modeling.



(a)



(b)

Fig. 7. Modeled $|E|$ field at 3 m for different layer thickness. (a) E_x polarization. (b) E_y polarization.

test fixture. The same number of PML and white-space layers are used throughout the rest of this study. The comparison of the modeled and the measured results is shown in Fig. 2. The modeled results with higher dielectric loss agree well with the measured results at high frequencies, while the modeled results with lower dielectric loss agree well with the measured results at low frequencies. Using a small dielectric loss in the modeling results in excessively high Q resonances at high frequencies, which demonstrates that the dielectric loss had a prominent effect on the Q value of the modal parallel plane resonances.

Modeling and measurement of a dc power-bus structure that included SMT decoupling capacitors was also considered. The schematics of this example are shown in Fig. 3. It is a simple PWR-GND structure with decoupling capacitors distributed over the board. The board size was 15 cm × 20 cm, and the dielectric was a 65-mil FR4 material. For the experimental board, one end of each decoupling capacitor was soldered directly to the top plane, while the other end was connected to the bottom plane by a short piece of *AWG 24* wire. A 2-mm- × -2-mm square aperture was cut in the upper plane to allow each *AWG 24* wire to penetrate the plane without electrical contact. The positions of the aperture centers (where the wires penetrate the plane) are shown in the figure. A two-port measurement was conducted using an *HP 8753D* network analyzer with all sixteen capacitors mounted on the board, and the measured results were compared to the FDTD modeled results.

In the FDTD modeling, the relative dielectric constant was $\varepsilon_r = 4.2$, and the uniform effective dielectric conductivity was 0.000 04 S/cm and 0.0002 S/cm over the range 100 MHz–2 GHz and 2 GHz–5 GHz, respectively. Each capacitor was modeled by an ideal capacitor in series with a resistor (for the ESR). The nominal capacitance used was 9 nF and the resistance was 130 mΩ, which were determined by an impedance measurement on one component using an *HP 4291A* impedance/material analyzer. By including the lead wires of the capacitor in the modeling, the parasitic inductance of the SMT capacitor interconnect was taken into account automatically. The algorithm for incorporating a capacitor sub-cell in the FDTD modeling can be found in [21]. The source was modeled using the same approach as described in the previous modeling example. The measured and modeled results of $|S_{11}|$ and $|S_{21}|$ are shown in Figs. 4 and 5, respectively. Good agreement was achieved for both frequency ranges. The results indicate that the FDTD method is suitable for power-bus modeling with decoupling capacitors, provided that the dielectric loss is adequately included in the modeling.

These two modeled examples contain the basic geometries of interest in the power-bus problems considered in this work. The FDTD method is demonstrated to be suitable for modeling power-bus problems, and will be used as the numerical tool throughout the rest of this paper.

III. Radiated EMI Versus Layer Thickness

Experimental investigations of the effect on radiated EMI of power-bus layer thickness have been reported in [8], where radi-

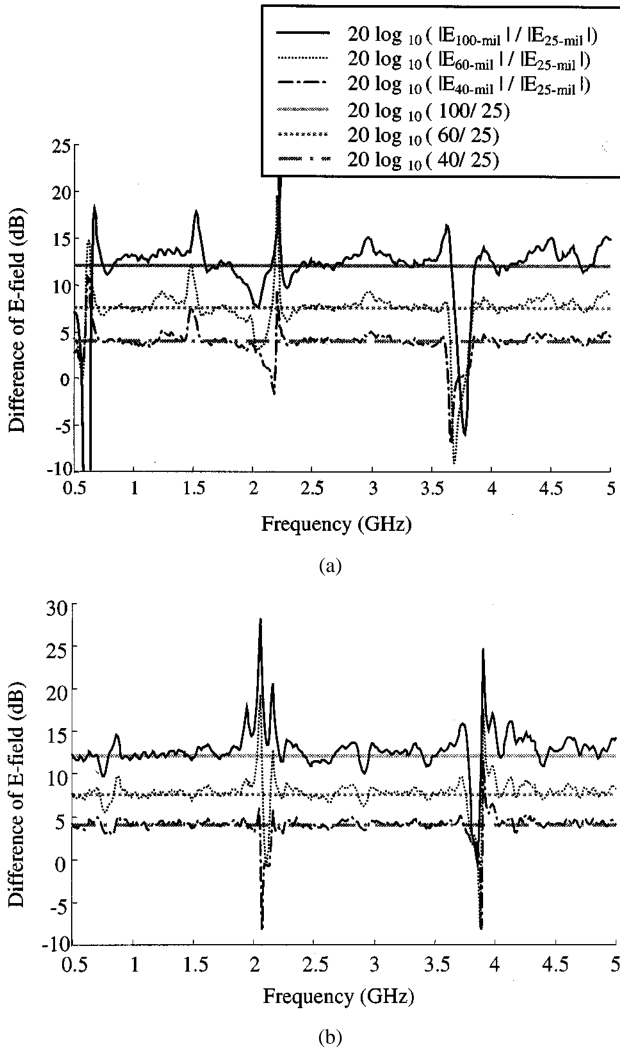


Fig. 8. The FDTD modeled and predicted (by linear relation to layer thickness) EMI difference for different layer thicknesses. (a) Horizontal polarization. (b) Vertical polarization.

ation from a 60-mil bare-board was approximately 10 dB higher than that from a 20-mil board. As indicated previously, the direct approach for a parametric study of the relationship between radiated EMI and layer thickness is to conduct a series of EMI measurements in a chamber. However, it requires sophisticated measurement facilities, and construction of numerous boards. Furthermore, ensuring the repeatability of the measurements is time-consuming and tedious. In Section II, the FDTD method was demonstrated to be a suitable numerical tool for power-bus modeling. In order to investigate the radiated EMI, the radiated far-zone field was calculated by applying equivalence theory to the FDTD modeling results. Specifically, the electric and magnetic fields on a virtual surface, S', completely surrounding the FDTD model of the test fixture were calculated from the FDTD modeling. From the calculated values of the electric and magnetic fields on this surface, equivalent magnetic and electric surface current distributions were determined. The far-zone electric field components were then calculated from these equivalent current distributions residing on S'. The same modeling tool has been shown to correctly predict the $|E|$ field at 3 m for frequencies above 500 MHz [23], [24]. It is then applied here to model the radiated EMI at 3 m from a PWR-GND two-layer board with different layer thicknesses. A parametric study was conducted to determine the functional relationship between the radiated EMI and the layer thickness.

The schematic of the PWR-GND two-layer board is shown in Fig. 6. Both the ground plane and the power plane were 15 cm $\times$ 20 cm. A sinusoidally-modulated Gaussian voltage-source was placed in between the planes, and the feeding point was (18 mm, 12 mm) away from the left-bottom corner of the board. The modeled EMI at 3-m broadside (in the $z$direction) to the PCB for dielectric layer thicknesses of 25, 40, 60, and 100 mil is shown in Fig. 7. The results are normalized to a 1 mA current source at all frequencies. The radiated EMI increases as the layer thickness increases, and the increment is almost constant over the entire frequency band. The results are re-plotted in Fig. 8, by calculating the difference (in decibels) of the radiated E-fields for the 40, 60, and 100 mil boards compared to that for the 25-mil board. The straight lines in the figure are the predicted difference if the radiated E-field is exactly proportional to the layer thickness. The results shown in Fig. 8 indicate that the radiated EMI is nearly proportional to the power-bus layer thickness, except at the nulls. However, these nulls are of little consequence when evaluating the EMI differences.

The input impedance and power-bus voltage of this two-layer board with different layer thicknesses were also studied to provide insight into the physics that relates the layer thickness to the radiated EMI. The geometry shown in Fig. 6 is essentially a microstrip-patch antenna. From microstrip antenna theory, when the layer thickness $h \ll \lambda$ (λ is the wavelength), the far-zone E-field of the antenna can be written as (for the TM_{10} mode) [12]

$$E_r \approx E_\theta = 0 \tag{1a}$$

$$E_\phi \approx j2\frac{V_0 e^{-jkr}}{\pi r}\sin\theta\frac{\sin\left(\frac{kw}{2}\cos\theta\right)}{\cos\theta}\cos\left(\frac{kl}{2}\sin\theta\sin\phi\right) \tag{1b}$$

where V_0 is the voltage across the radiating edge, and l and w are the length and width of the microstrip antenna. For a rectangular coordinate system, the E-field components of a far zone point at broad-side to the antenna are schematically shown in Fig. 9, where only the E_x component is not zero for the TM_{10} mode. The equations indicate that the radiated EMI is proportional to the voltage across the radiating edge, which is proportional to the thickness. Although the equations are derived from the TM_{10} mode (where power-bus voltage is uniformly distributed over the radiating edge), the linear relationship between the radiated field and edge voltage is expected to be applicable for higher modes (where power-bus voltage is not uniformly distributed over the radiating edge length), where the larger thickness is still small with respect to wavelength. Fig. 10 shows the voltage difference between two planes at the board corner closest to the feeding point obtained from the FDTD modeling. The results are normalized to a 1-mA source voltage at all frequencies, and the source impedance is 50 Ω. The voltage differences on the power bus resulting from different layer thicknesses are approximately proportional to the layer thickness, and are consistent with other published results [25]. A larger

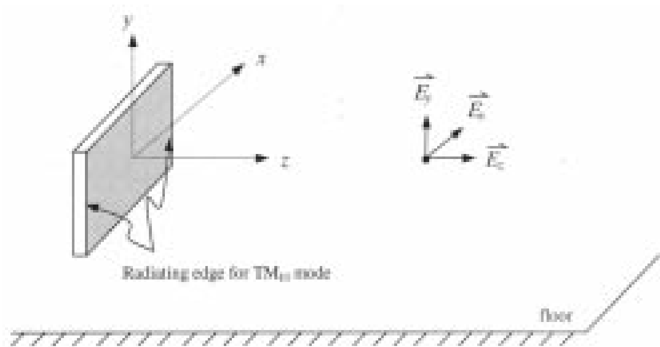


Fig. 9. A schematic representation of the E-field components of a far zone point broadside to the microstrip antenna.

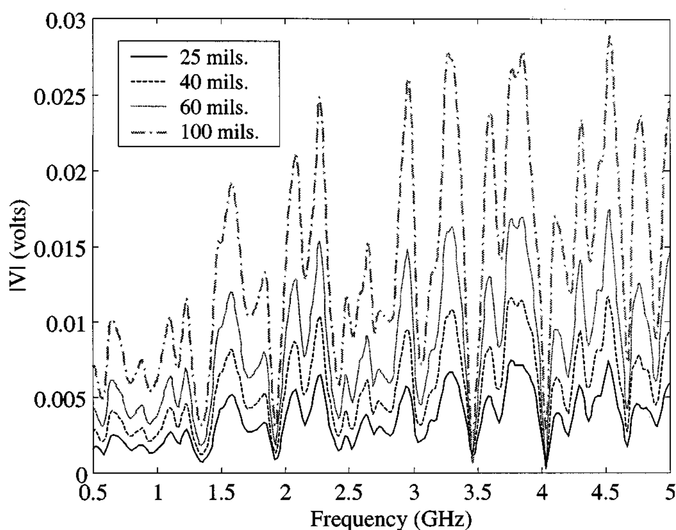


Fig. 10. The FDTD modeled power-bus voltage (at the board corner closest to the feeding point) for the board shown in Fig. 6 with different layer thicknesses.

layer thickness results in a larger voltage difference across the board edges (the voltage differences at other locations along the board edge are not shown herein for brevity), and is expected to result in greater radiation from the equations shown above.

Further study on the input impedance of the board helps to explain how the layer thickness affects the power plane voltage. The FDTD modeled input impedance of the two-layer power-bus stack with different layer thicknesses is shown in Fig. 11. Larger layer thickness results in a larger input impedance. This board input impedance is in series with the 50 Ω source impedance, and is driven by the Gaussian voltage source. These two impedances work as a voltage divider, and the actual voltage applied across the power and ground planes increases as the input impedance of the power-bus stack increases. If this input impedance is substantially smaller than the source impedance (which is the case for the studied geometry), the voltage between the power plane and the ground plane at the feeding point is then approximately proportional to the input impedance (or, the noise source is effectively behaving as a current source).

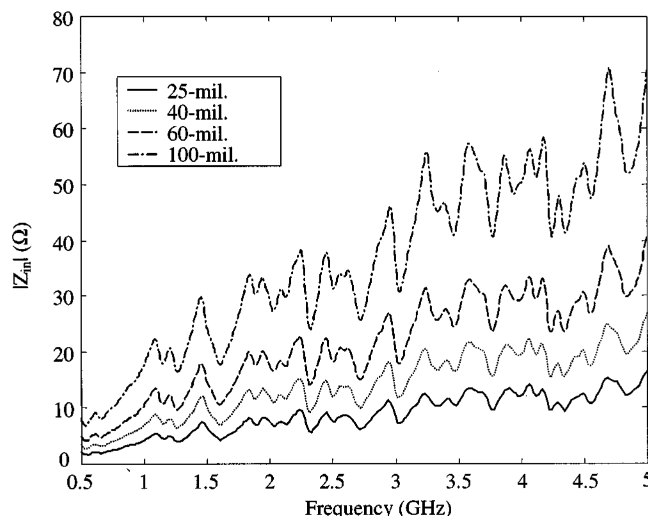


Fig. 11. The FDTD modeled input impedance for the board shown in Fig. 6 with different layer thicknesses.

IV. EMI Benefits of Ground Plane Stitching in Multilayer Power-Bus Stacks

For designs that employ multiple power-ground layer sets, proper ordering of the layer stack-up, and using via stitching to connect outer ground planes together along the periphery can mitigate radiation due to fringing edge electric fields. A qualitative and quantitative study of this effect on EMI in multilayer PCB stack-ups is presented in this section. The EMI at 3 m for different via stitch spacing and layer thickness is obtained from the FDTD modeling. The effects on EMI of nonuniform stitching will also be investigated in the next section.

The FDTD method was first applied to study the radiation mechanism for two multilayer power-bus structures, a GND-PWR-PWR-GND (GVVG) stack-up and a GND-PWR-GND-PWR (GVGV) stack-up, as shown in Fig. 12. The board dimensions were 15 cm × 20 cm, and each individual dielectric layer between two adjacent planes was 25 mil thick. The relative dielectric constant was $\varepsilon_r = 4.2$, and the effective dielectric conductivity was set as 0.000 35 S/cm to represent the dielectric loss of the board. The conductor on the PWR layers was recessed 8 mm at all of the four board edges as indicated by the dashed line in Fig. 12(c). The feeding point was 6 cm away from the 15-cm edge, and 4 cm away from the 20-cm edge of the ground plane. All the via holes penetrating a plane in the structure were modeled as 2 mm × 2 mm apertures. The spacing between the two shorting wires that connected the GND/PWR plane pairs together was 3 mm. The cell size in the FDTD modeling was 1 mm × 1 mm × 0.212 mm (x, y, z). The thickness of each dielectric layer was then modeled with 3 FDTD cells. A sinusoidally-modulated Gaussian voltage-source with a 50 Ω resistor in series was applied at the feeding point.

The effect of stitching around the periphery of the PCB board on the radiated EMI at 3 m was studied. For both configurations, the two GND planes were stitched together continuously by a number of vias at all the board edges. The spacing between adjacent stitching vias was 3 mm in the first case considered. Each stitching point was 1 mm (1 cell of the FDTD grid) away

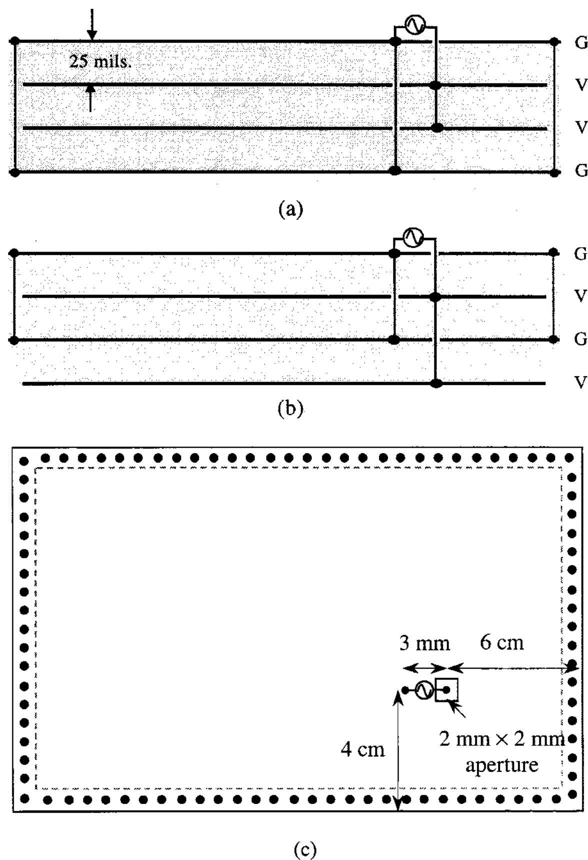


Fig. 12. Schematics of the GVVG and GVGV stack-ups with via stitching at board peripheries. (a) GVVG side view. (b) GVGV side view. (c) Top view.

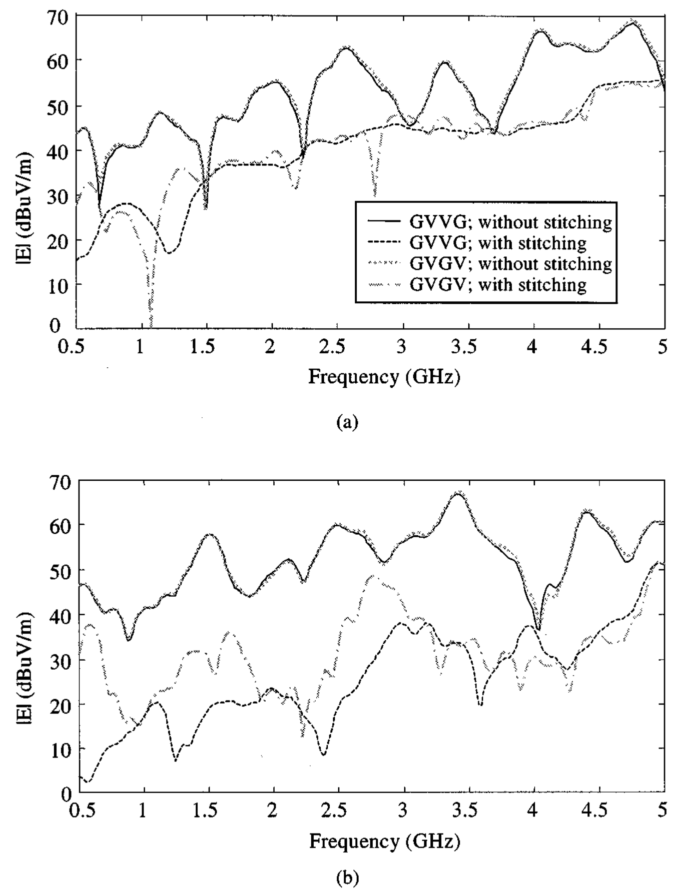


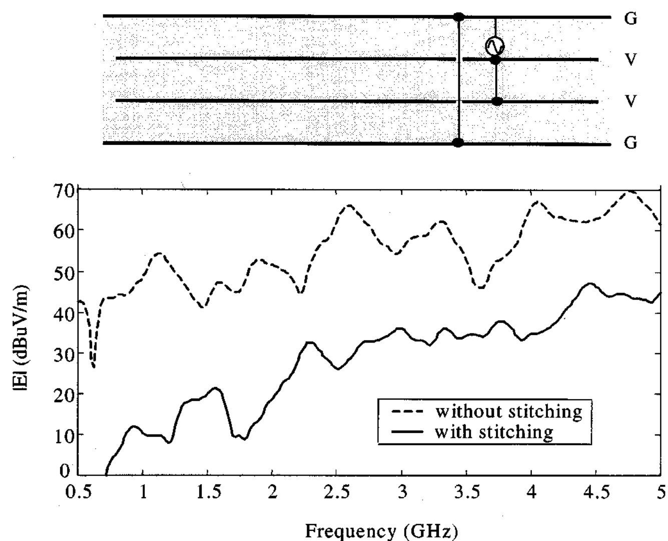
Fig. 13. Modeled EMI at 3 m for the cases with and without stitching for the GVVG and GVGV configurations with the source on top of all planes. (a) E_x polarization. (b) E_y polarization.

from the board edge. The EMI at 3 m with the stitching was obtained from FDTD modeling, and is compared to the EMI without stitching in Fig. 13. The results are normalized to a 1 mA current source at all frequencies. Each simulation requires approximately 140 MB of memory and takes approximately 8 h on a Pentium III 750 MHz CPU. The computation time may be reduced using the Generalized Pencil of Function (GPOF) technique for extrapolating the time series [26].

The stitching improves the EMI performance (as seen in Fig. 13), and the improvement for GVVG or GVGV configurations is generally the same, except some variation at low frequencies for the E_y polarization. However, the improvement for different polarizations is not comparable. The stitching reduces the EMI by an order of 20–30 dB for the E_y polarization, while only 10–20 dB for the E_x polarization. The polarization-dependent improvement is due to direct radiation from the feeding source on top of the board. As seen in Fig. 12, there is a 3-mm long wire placed horizontally on top of the boards. To eliminate the effect of this wire, another comparison of EMI with and without stitching of the ground planes was made on the GVVG configuration with a source placed in between the planes, as shown in Fig. 14. Here the excitation mechanism of the power plane sets is the same as before, however, the small radiator above the planes is eliminated, and the single EMI mechanism resulting from the fringing electric field can be studied. The E-fields at 3 m obtained from the modeling are compared in the same figure. For this case, the improvement in EMI performance with and without stitching for both polarizations is approximately the same. These results show that the 3-mm wire placed on top of the planes can result in an appreciable level of horizontally polarized radiated EMI. This level of EMI is smaller than that resulting from the fringing fields at board edges for the case without stitching, but larger than that resulting from the fringing field at board edges for the case with stitching. The implication for circuit design is that the EMI will be dominated by other mechanisms suggested previously, including direct radiation from active components, when coupling from fringing edge fields is minimized.

The EMI from a fringing edge field of the GVVG and GVGV stacks is then summarized in Fig. 15. The fringing field at the board edges of the top two planes is the dominant radiating source. Therefore, the GVVG stack-up and GVGV stack-up have a similar EMI performance. A dense stitching all around the board edges effectively shields the radiation from fringing edge fields, and, hence, considerably reduces the radiated EMI. The radiation is then dominated by other coupling paths.

The improvement in the EMI performance for ground plane stitching is evident, as shown in Figs. 13 and 14. However, the study was based on configurations with the source placed on top of the board. If there are active components on the other side of the board, then the bottom power plane set is the dominant radiation mechanism. Stitching will help to reduce the radiation



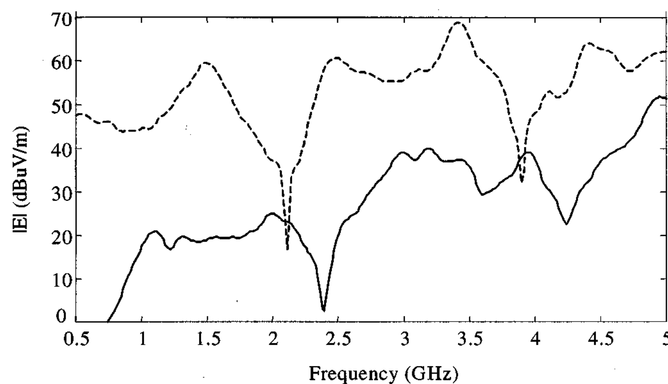


Fig. 14. Modeled EMI at 3 m for the cases with and without stitching for the GVVG configuration with a source placed in between planes. (a) E_x polarization. (b) E_y polarization.

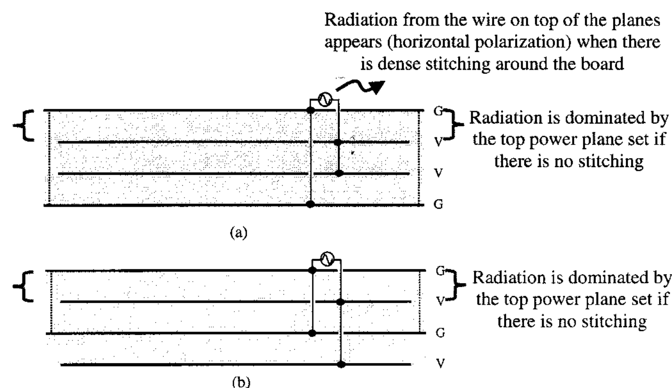


Fig. 15. Schematic summarizing the EMI radiating mechanisms when the component is placed on top of the board.

for the case of the GVVG stack-up, since the dominant fringing fields are still contained in the enclosure formed by the ground planes and stitching vias. However, it will not appreciably improve the EMI performance for the case of a GVGV stack-up, since the fringing fields of the bottom two planes are outside of the effective enclosure.

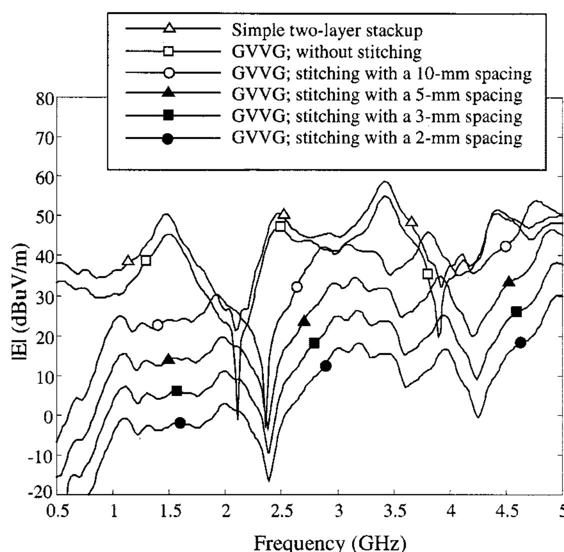


Fig. 16. The modeled EMI at 3 m for different stitching cases, together with the case without stitching and a two-layer stack-up. The layer thickness was 25 mil for all cases.

FDTD modeling was then used to quantify the functional variation of EMI with respect to the layer thickness and via-stitch spacing. The GVVG configuration shown in Fig. 14 was selected as the test bed (EMI source mechanisms other than the fringing fields are avoided for this configuration). During the first step of the study, the layer thickness was fixed at 25 mil and the stitch spacing was selected as 2, 3, 5, and 10 mm. The modeled results for different stitching cases, together with the results of the case without stitching, are shown in Fig. 16. The result for the case of a two-layer stack-up with only a single power/ground plane set is also shown. All the far fields obtained from FDTD modeling are the E_y polarization, and are normalized to a 1-mA current source at all frequencies (results for the E_x polarization are similar). The results indicate that stitching significantly reduces the EMI, and a denser stitch spacing around the periphery of the board can improve the EMI performance for a radiation mechanism dominated by fringing fields from the board edge. The EMI reduction for denser stitch spacing is generally a constant over the studied frequency range. Other comparisons show that the four-layer stack-up only marginally improves the EMI performance compared to a two-layer stack-up with the same layer thickness, since the layer thickness of the dominant radiating GND-PWR plane pair is the same for two cases.

FDTD modeling was then applied to other GVVG configurations with layer thicknesses of 15, 40, 60, and 100 mil The objective was to extract design curves that show the EMI variation as a function of layer thickness and stitch spacing. A family of curves was generated, as shown in Fig. 17. Each curve is the relationship between the E-field at 3 m and the layer thickness. When the stitch spacing reaches a certain density, the modes in the resulting cavity are not appreciably changed by increasing the density, as seen in Fig. 16. Consequently the decrease in the radiated EMI is nearly constant with frequency. The family of design curves is then just this difference in the curves in dB. Different curves have different values of stitch spacing. The magnitude of the E-field for the 15-mil board with 2-mm stitch spacing is used

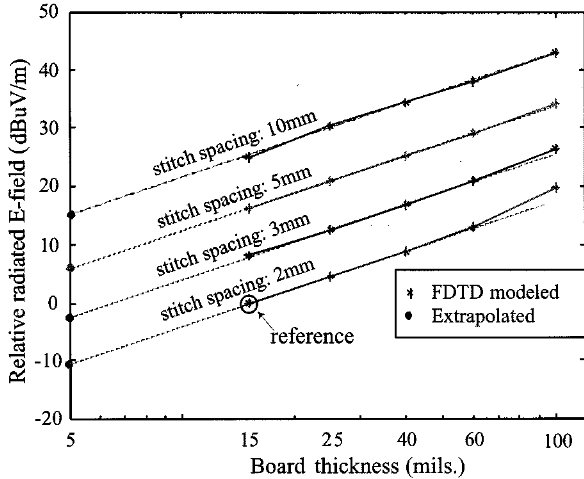


Fig. 17. The EMI at 3 m as a function of layer thickness for different uniform stitch spacings.

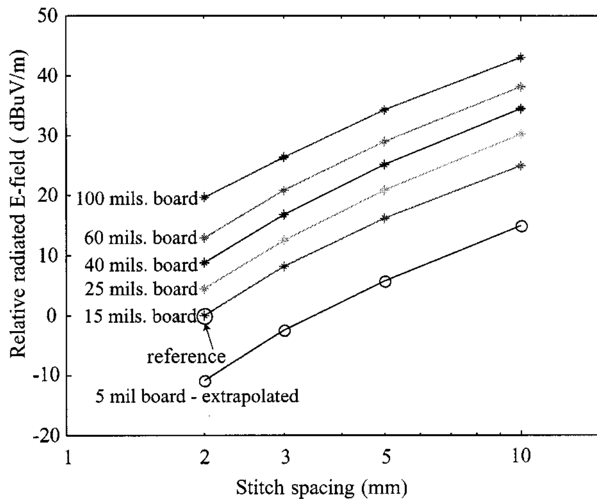


Fig. 18. The EMI at 3 m as a function of stitch spacing for different layer thicknesses.

as the reference (0 dB). The results for a 5-mil layer-thickness are extrapolated from the nearly linear variation of the curves with layer thickness. This nearly linear variation of the radiated EMI and the layer thickness on the log-log scale plot is approximately 21 dB per decade, which means that the E-field is approximately proportional to layer thickness. The conclusion is similar to that drawn in Section III for a PWR-GND power-bus structure without stitching. The results also demonstrate that the radiated field has an approximately linear relationship (on a log-log scale) to the stitch spacing for the cases considered with the stitch spacing ranging from 2 to 10 mm, as shown in Fig. 18. The slope of the curves in the figure is approximately 30 dB per decade, which means that the radiated E-field varies approximately as a function of $s^{3/2}$, where s is the stitch spacing. Therefore, an approximate design equation is:

$$E_{3m} \approx C \cdot h \cdot s^{1.5} \tag{2}$$

where C is a constant and h is the layer thickness. The equation is valid for the stitch spacings considered herein ranging from 2 to 10 mm. For a spacing smaller than 2 mm, the actual opening

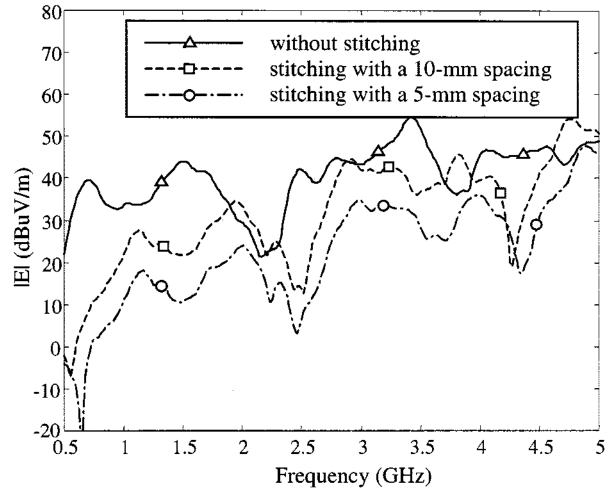


Fig. 19. The FDTD modeled EMI at 3 m for the GVVG power-bus stack with sixteen decoupling capacitors distributed on top of the stack.

between adjacent vias is smaller than the stitch spacing since the radius of the via must be considered. While for a spacing larger than 10 mm, the radiated E-field approaches the case of without stitching, and the relationship in (2) may not hold.

In order to investigate the validity of the ground plane stitching technique in practical circuit design, sixteen decoupling capacitors were placed over the GVVG four-layer power-bus stack shown in the top of Fig. 14. The capacitors were connected to the top two planes, the connections and the locations of the capacitors were the same as that shown in Fig. 3. The layer thickness here was 25 mils. The calculated EMI at 3 m for the cases of no stitching, 10-mm stitching and 5-mm stitching are shown in Fig. 19. The results indicate that the presence of the decoupling capacitors does not significantly change the EMI benefits of the ground plane stitching.

V. Nonuniform Stitching

The previous study and design curves were based on a uniform stitch spacing over the periphery of the board edges. However, a uniformly dense stitch spacing may not be easily achievable in an actual circuit due to a high design density. Effects on EMI for nonuniform stitching are considered in this section. The study includes several configurations with nonuniform stitching over certain segments of the board edge. Some representative configurations are shown in the top of Fig. 20. The layer thickness was 15 mil, and the layer stack-up is the same as that shown on top of Fig. 14. Case A has no stitching at all edges, and Case D has a uniform stitching (2 mm spacing) over all four edges. Cases B and C have larger stitching spacing (10 mm) over a certain segment (one third of the entire edge length), while the rest of the board edges have a uniform stitch spacing of 2 mm. The position of the "larger opening" for Cases B and C differs, with that for Case B closer to the feeding source.

The FDTD modeled radiated EMI at 3 m is shown in Fig. 20. All the results are for the E_y polarization (radiation from the 20-cm board edge), and are normalized to a 1 mA current source. The results indicate that larger stitching spacing over certain segments increases the EMI compared to uniform stitching (comparing Cases B and C to Case D). The increment

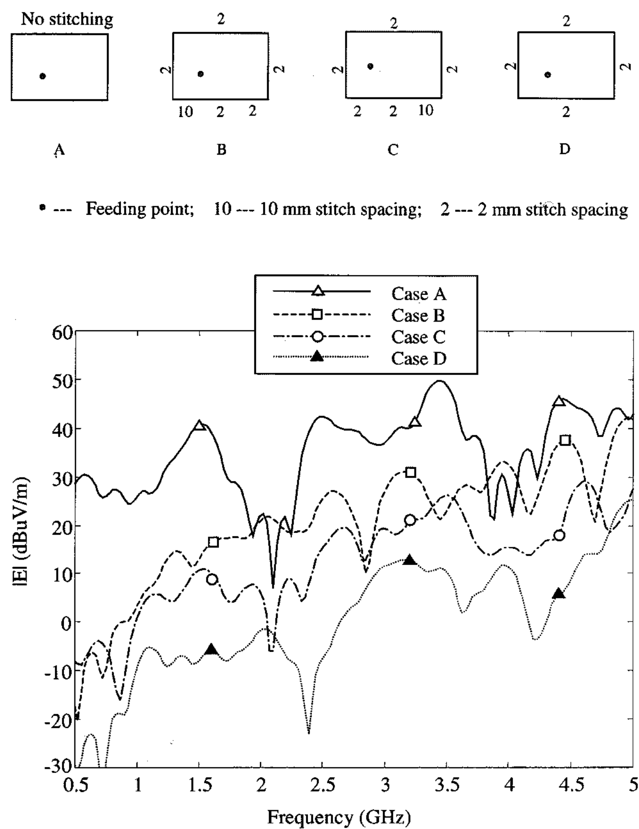


Fig. 20. Effects on the radiated EMI at 3 m of nonuniform stitching.

is related to the location of the larger stitch-spacing segment with respect to the feeding point, (Case B has smaller EMI compared to Case C). This is probably because the "larger opening" is farther away from the feeding point for Case C. It could also be related to the modal distribution.

The E_x polarization results have no significant difference among all the stitching cases (the results are not shown herein since they are virtually on top of each other), since the radiated field for E_x polarization results from the vertical edges where a uniform 2-mm stitching is applied for all the stitching cases. Furthermore, the level is lower than the E_y polarization for cases with an intermittent larger stitch spacing, which means that the E_y polarization dominates with the "larger openings" along the horizontal (20-cm long) edges.

VI. Summary and Conclusions

The EMI benefits of ground plane stitching in multilayer power-bus stacks were studied herein. Experimental work was conducted to corroborate the validity of the FDTD method for power-bus modeling. The good agreement between the measurements and FDTD modeling provides confidence in the FDTD method for developing the power-bus design approach. The EMI benefits of the ground plane stitching were demonstrated through the FDTD modeled E-field of a GND-PWR-PWR-GND four-layer power-bus stack. Different layer thickness and different stitching spacing were considered. A number of simulations were conducted, and, design curves and an empirical equation were generated to demonstrate the variation of radiated EMI as a function of the layer thickness and the stitch spacing.

Generally, for PCBs with multiple power and ground layers, arranging the layer stack-up such that ground layers are the first complete layers (or portions thereof) from the top and bottom board sides, and stitching the ground planes together all around the edges can achieve in excess of 10–20-dB EMI reduction for EMI dominated by the fringing edge fields on the power bus. A minimum of 2-mm stitch spacing was investigated in this report, for which approximately 20-dB EMI reduction was achieved. Further studies indicate that for the same multilayer stack but with a number of decoupling capacitors on the board, the effectiveness of this ground-plane stitching technique is virtually the same.

The EMI mechanism of concern in this study was radiation dominated by the fringing electric field at the edges of the power area. Other potential EMI coupling paths and radiation mechanisms that are related to noise on the dc power bus include power-bus noise conducted through the power pins of a connector and coupled to a radiating structure on a different board, coupling to an I/O line that transitions through the dc power bus, and direct radiation from the active components themselves. For the PCBs whose dominant EMI-coupling mechanism comes from the fringing field of the power bus, the EMI improvement of the functioning system from the ground plane stitching can be compromised due to other coupling mechanisms, which may show up and become dominant when the original dominant coupling mechanism is mitigated. The EMI benefit of the ground- plane stitching can also be compromised for nonuniform stitching when there is intermittently larger stitch spacing on an edge, which is sometimes inevitable in practical design. The compromise occurs for the polarization associated with that board edge.

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