Energy-Efficient Capacitive-Sensor Interface Based on A Multi-Slope ADC

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Abstract

This thesis presents an energy-efficient capacitive sensor interface based on a multi-slope analog-to-digital converter (ADC). This highly stable capacitance-to-digital converter (CDC) utilizes precision resistor as reference components. By utilizing a multi-slope analog-to-digital converter, the conversion time of this design is reduced down to 50us. The counter works as a sinc filter to reduce the noise, which helps to achieve a resolution of 15 bits with a 0.2W power consumption.

Keywords – Capacitance-to-digital converter, multislope analog-to-digital converter, precision resistor, sinc filter.

Abstract

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Chapter1

Introduction

Closed-loop control systems are widely used in many industrial applications to position and align accurately static objects. For example, in high-performance lithography machines, such systems are required to align critical components [1]. Due to their accurate performance and inexpensive and simple structure, capacitive displacement sensors are one of the preferred choices to measure the relative position and the drift/vibration of the controlled objects. In these applications, the capacitive sensor has to provide a high-resolution and a high-accuracy with minimum latency. Because of the high cost of the calibration process in these accurate positioning systems, it is beneficial to use a measurement system with high level stability especially which has low drift with temperature variation.

To satisfy the practical requirements, a Capacitance-to-Digital Converter (CDC) with high accuracy and excellent stability has been reported in [2], based on the multi-slope analog-to-digital conversion principle. Despite of demonstrated impressive stability of less than 2 ppm/ºC, the CDC has one disadvantage – it dissipates a significant amount of heat due to its relatively high power consumption. This property prevents the positioning of the CDC close to the capacitive sensor in a tightly controlled environment, resulting in the need to use relatively long cables, which increase the noise gain and reduce the resolution. One way to implement the same conversion principle with reduced power consumption is to integrate all analog parts.

In this thesis, based on a multi-slope Analog-to-Digital Converter (ADC), a kind of CDC is designed, which is optimized for low power consumption utilizing stable resistors as reference components.

In this chapter, first a brief introduction of capacitive sensors, including their measurement principles, is presented in section 1.1. After that, readout approaches with long-term stability are discussed in section 1.2. Finally, the organization of this thesis is described.

1.1 Capacitive Sensors

Because of their accurate performance, inexpensive and simple structure, capacitive sensors are popular in many industrial applications, such as keypads, micrometers, lamp dimmers, and more. Capacitive sensors can be used to measure many different types of variables, like displacement, humidity, acceleration, liquid level, etc. The most commonly utilized structure is parallel plate capacitive sensor (Figure 1-1).

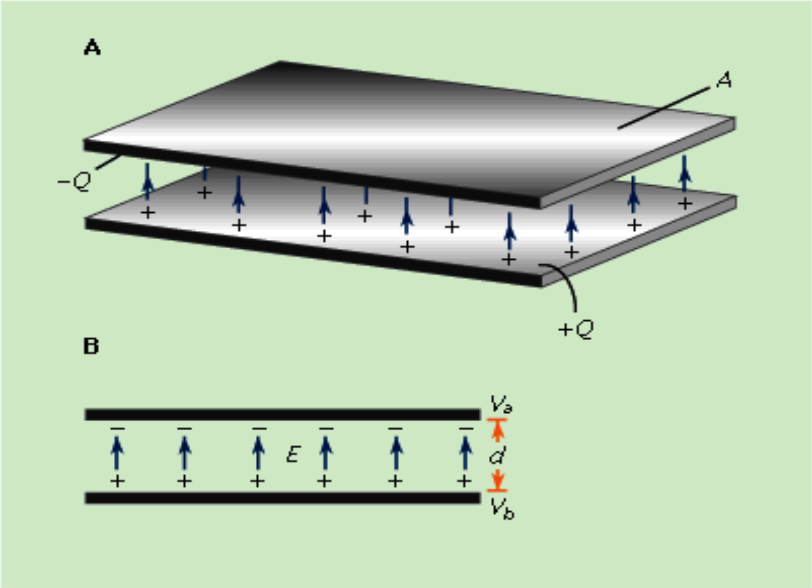

Figure 1-1 Parallel-plate capacitor: (A) two parallel plates with area A, (B) two parallel plates with distance d [3].

These two plates are in parallel with overlapping area A, distance d and a dielectric permittivity ε, the capacitance of this capacitive sensor is:

$$C_0 = \varepsilon \frac{A}{d}. \quad (1\text{-}1)$$

In this thesis, it is used as a capacitive distance sensor, which converts the change of displacement to the change of capacitance.

1.1.1 Measurement Principles

Normally, capacitive sensors are connected to an electronic interface to measure their capacitance. There are several ways to do this by utilizing different excitation signals, just as Figure 1-2 shows.

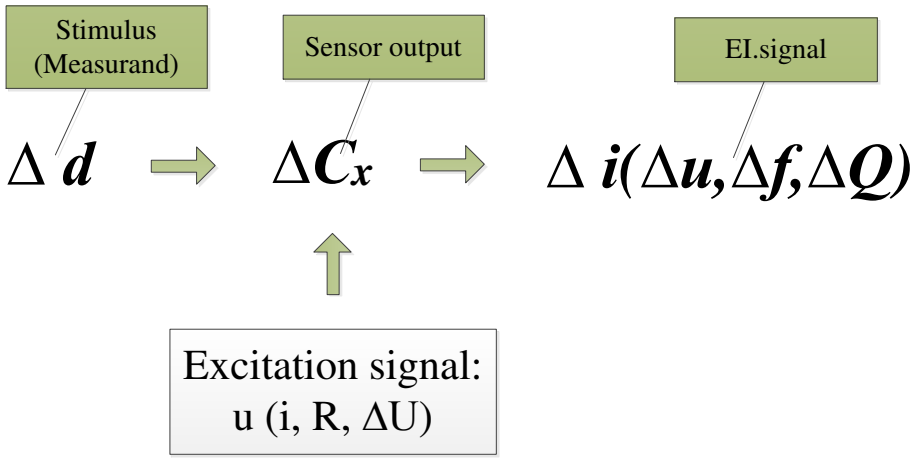

Figure 1-2 Electronic interface with different reference excitation signals [4]

One way to measure capacitance is to utilize an oscillator circuit together with another passive component. In this case, the frequency is used as the measurement signal to obtain the value of the unknown capacitance [5]. Another way is to use harmonic excitation signals (u or i) to measure the reactance of the unknown capacitance. Beside these two ways, an alternative approach based on charge balancing principle can also be used to measure the capacitance value, which is first converted into charge Q_x stored in the capacitive sensor. The charge Q_x can be expressed as:

$$Q_x = C_x \times U_{ref}, \quad (1\text{-}2)$$

where U_{ref} is a reference voltage to charge the capacitive sensor [4].

Resolution, measurement time and stability are three main performance parameters to evaluate the performance of a capacitive-sensor electronic interface. In some particular industrial applications, such as in lithography machine, a stable electronic interface with high resolution and minimum latency is needed. Therefore, the third method is chosen in this thesis by utilizing stable reference components, like precision resistor.

1.2 Readout Approaches

In order to get an excellent stability, stable reference components must be chosen in a CDC. There are three readout approaches which utilize precision resistor as reference component: First Order Relaxation Oscillator, Sigma-Delta AD converter and Dual/Multi Slope AD converter.

1.2.1 First Order Relaxation Oscillator

A relaxation oscillator is a conventional circuit which is used in many applications. In this section, only the first-order relaxation oscillator used as a capacitive-sensor interface is discussed. This type of electronic relaxation oscillators normally stores and removes electrical energy in a capacitor repeatedly to set up the oscillations. Figure 1-3 shows the schematic circuit of a modified Martin first-order relaxation oscillator [5]. The oscillator consists of an Op-Amp, a comparator, two inverters, a capacitor C_{int} and a resistor R_{int}.

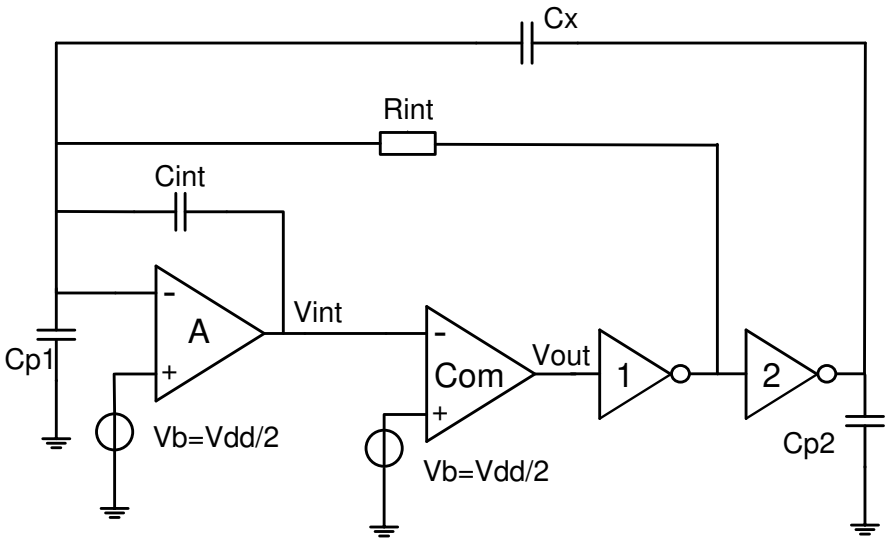

Figure 1-3 First-order relaxation oscillator

This oscillator is used to measure the unknown capacitor C_x. When the output voltage of inverter 2 changes, C_x is re-charged with a charge Q_x, which flows to the inverting input of the Op-Amp A and is stored in the capacitor C_{int}. Then the capacitor C_{int} is discharged though a stable resistor R_{int} to drive the output voltage V_{int} of the Op-Amp A back to its initial value. After the output voltage V_{int} across V_b, the output voltage of inverter 1 changes, which means that the output voltage of inverter 2 also changes, so that the unknown capacitor C_x is re-charged with an opposite polarity. Capacitor C_{p1} and capacitor C_{p2} are the parasitic capacitances to ground which are caused by connecting cables. The period of the oscillator output signal T_x can be expressed as:

$$T_x = 4 \times R_{int} \times C_x. \quad (1\text{-}3)$$

Advantage

The first-order relaxation oscillators produce period-modulated output signal, which can be interfaced directly to a microcontroller.

Disadvantage

A basic disadvantage of first-order relaxation oscillator is related to the measurement time, which depends on the value of the measured capacitance. When the measured capacitance is exceedingly large, it needs a long time to be measured.

1.2.2 Sigma-Delta AD converter

Sigma-Delta AD converters are synchronous indirect AD converters which are synchronized to a clock and so does the output signal of the AD converters. Two

types of Sigma-Delta AD converter will be briefly introduced: First-Order Sigma-Delta Modulators and Second-Order Sigma-Delta Modulators.

• First-Order Sigma-Delta Modulators

Figure 1-4 depicts a first-order sigma-delta modulator, which typically consists of at least one integrator and a comparator. The comparator is used to detect the voltage difference between the output voltage of the integrator and "virtual ground", then utilizing feedback to drive the output voltage of the integrator back to zero. The input signal V_{in} is continuously integrated, while the reference voltage is subtracted fromV_{in}, if the integrator's output voltage exceeds "virtual ground". This comparator only changes its output on the rising edges of the clock. Its output is a synchronous sequence of 0's and 1's, which are called bitstream [6].

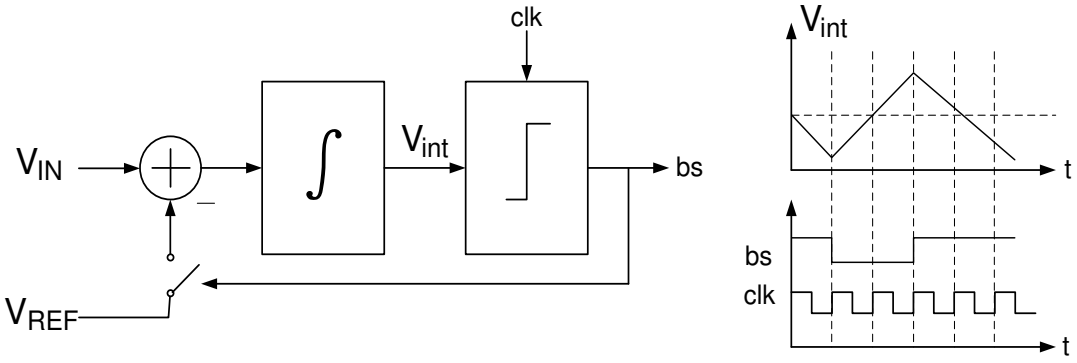

Figure 1-4 Block diagram and timing of a first-order Sigma-Delta modulator [6]

When the total number of clock cycles is N_{total}, while the bitstream is one during N_1 clock cycles, the charge balancing implies:

$$N_{total} \cdot V_{IN} = N_1 \cdot V_{REF}. \quad (1\text{-}4)$$

To rewrite it as:

$$\frac{N_1}{N_{total}} = \frac{V_{IN}}{V_{REF}} \quad (1\text{-}5)$$

It means that the fraction of ones in of the bitstream is equal to the ratio of V_{IN} and V_{REF}. It can be simply measured by a counter.

• Second-Order Sigma-Delta Modulators

First-order sigma-delta modulator has the advantages of simplicity and stability, but its overall performance in terms of resolution is inadequate for most applications.

Figure 1-5 shows a second-order sigma-delta modulator with a feedback path of gain *b* to the input of the second integrator. When *b >> 1*, the entire loop is stable over the full input range but it works as a first-order modulator, which means that the effect of the first integrator is negligible. On the other hand, when *b << 1*, the loop is conditionally stable, which means that it results in very large integrator outputs. The typical choice of *b* is 2 [6].

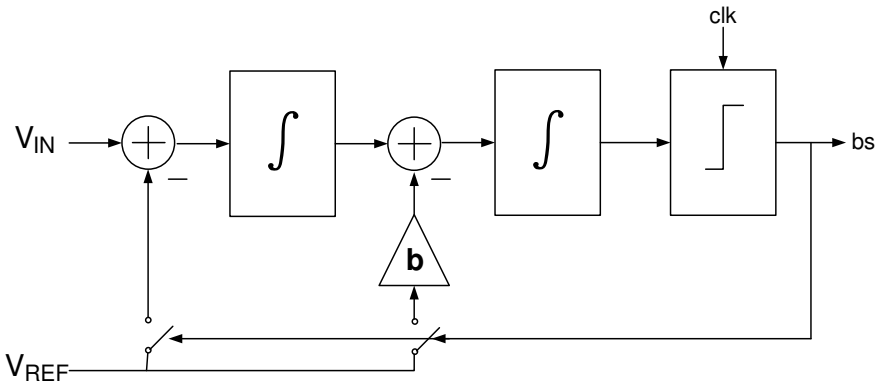

Figure 1-5 Block diagram of a second-order Sigma-Delta modulator [6]

Advantages

- **Noise shaping:** Sigma-Delta Modulator is an oversampling AD converter. It can achieve a resolution higher than that of the quantizer. The quantization noise in the band B to $f_s/2$ can be filtered out by a digital filter, where B is the bandwidth of this Sigma-Delta modulator. For every doubling of the oversampling ratio, the quantization noise power in the signal band is halved, so that increasing the resolution by 0.5 bits [6].

- **Less critical:** Compared to Nyquist AD converter, the requirements for the anti-aliasing filter can be relaxed, because the frequency band from B to $f_s/2$ is available for roll-off.

- **Energy-efficient:** Resolution can be improved with oversampling ratio, increasing a factor of 2^{2N} can obtain an increase of N bits. However, this means that it needs more power. The problem can be solved by utilising higher order modulator. In other words, utilizing higher order Sigma-Delta modulator can achieve higher resolution with the same oversampling ratio, assuming that the quantization noise is dominant.

Disadvantages

- **Instability:** One disadvantage of higher-order Sigma-Delta modulator is that it has a limited DC input range, otherwise it will be instable. For inputs close to zero or V_{ref}, the integrator outputs become excessively large and the modulator produces low-frequency limit cycles that result in a strong increase of the quantization error.

- **Latency:** Another drawback is the long latency of Sigma-Delta modulator.

1.2.3 Multi Slope AD converter

Multi Slope AD converter (also called integrating AD converter) is another type of synchronous modulator. It is always used in a system which needs a high resolution and excellent stability.

Multi Slope AD converter is an improved version of Dual Slope AD converter. In order to understand the operating principle of Multi Slope AD converter, the operating principle of Dual Slope AD converter will be shown first.

- Dual Slope AD converter

As Figure 1-6 shows, the analog part of a Dual Slope AD converter consists of two components: an integrator and a comparator.

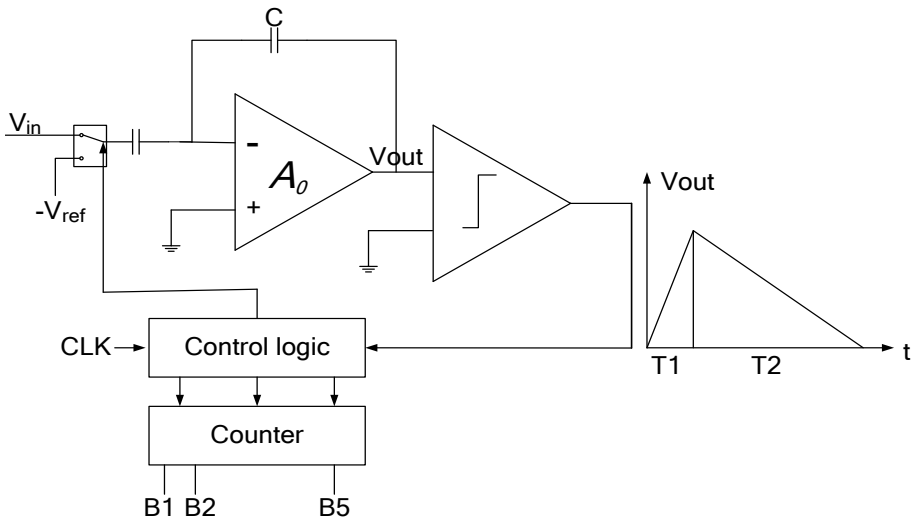

Figure 1-6 Block diagram and timing of a Dual Slope AD converter

The amplifier A_0 is used as an integrator, which means that the output voltage of integrator V_{out} is the integral of V_{in}:

$$V_{out} = -\frac{1}{RC}\int_0^T V_{in}(t)dt. \quad (1\text{-}6)$$

In order to digitize the input voltage V_{in}, a reference voltage $-V_{ref}$ with opposite polarity needs to be supplied to drive the output of the integrator back to zero. Because of the charge balance, the unknown voltage V_{in} is calculated by the following equation:

$$\frac{V_{in}T_1}{RC} = \frac{V_{ref}T_2}{RC}, \quad (1\text{-}7)$$

where T_1 is a predetermined time to charge capacitor C, T_2 is the time to discharge capacitor C. The discharging time T_2 can be counted by a digital counter. In order to get an N bits resolution, the minimum discharging time T_{2_min} has to be:

$$T_{2\_min} = 2^N \times T_{sampling}, \quad (1\text{-}8)$$

where $T_{sampling}$ is the sampling time of the counter.

• Multi Slope AD converter

Dual Slope AD converter has advantages of simplicity and stability, however, the problem of prolonged latency needs to be improved. Figure 1-7 depicts the main analog part of a Multi Slope AD converter, which also consists of two components: an integrator and a comparator.

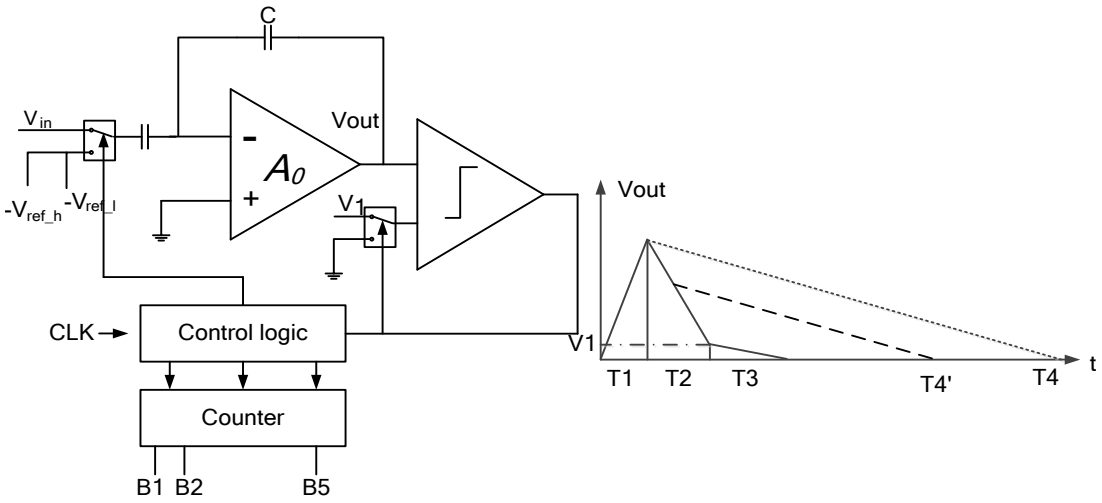

Figure 1-7 Block diagram and timing of a Multi Slope AD converter

Compared with the structure of the Dual Slope AD converter, the only difference is the presence of a second reference voltage: $-V_{ref\_l}$ and $-V_{ref\_h}$. The equation to calculate the unknown voltage V_{in} changes to:

$$\frac{V_{in}T_1}{RC} = \frac{V_{ref\_l}T_2}{RC} + \frac{V_{ref\_h}T_3}{RC}, \quad (1\text{-}9)$$

where T_1 is a predetermined time to charge capacitor C, T_2 is the time to discharge capacitor C with reference voltage $-V_{ref\_l}$ and T_3 is the time to discharge capacitor C with reference voltage $-V_{ref\_h}$ The discharging time T_2 and T_3can be counted by a digital counter. The total discharge time T_{tot} is the sum of T_2 and T_3. Assuming the voltage V_{ref_l} is 2^n times bigger than the voltage V_{ref_h}, to get the same resolution of N bits, the minimum discharging time T_{tot_min} can be expressed as:

$$T_{tot\_min} = (2^n + 2^{N-n}) \times T_{sampling}. \quad (1\text{-}10)$$

When *n* is half the value of *N*, the minimum discharging time T_{tot_min} is:

$$T_{tot\_min} = \left(2^{\frac{N}{2}} + 2^{N-\frac{N}{2}} \right) \times T_{sampling}. \quad (1\text{-}11)$$

The minimum discharging time can be rewritten as:

$$T_{tot\_min} = 2^{\frac{N}{2}+1} \times T_{sampling}. \quad (1\text{-}12)$$

Compared to the minimum discharging time of Dual Slope AD converter, which is $T_{2\_min} = 2^N \times T_{sampling}$, the ratio can be written as:

$$\frac{T_{2\_min}}{T_{tot\_min}} = 2^{\frac{N}{2}-1}. \quad (1\text{-}13)$$

It can be seen that using Multi Slope AD converter can save at most $2^{\frac{N}{2}-1}$ times latency compared with Dual Slope AD converter.

Advantages

- **Stability:** As the foregoing analysis showed, the Multi (Dual) Slope AD Converter converts analog input signal into a time signal, which is highly stable.

- **Resolution:** Figure 1-8 shows that Multi (Dual) Slope AD converter can reach a really high resolution, because the conversion accuracy is free from non-linear capacitor *C*. It simply depends on the noise of reference resistor and integrator and the quantization noise. It can also tolerate the offset of the comparator and the integrator.

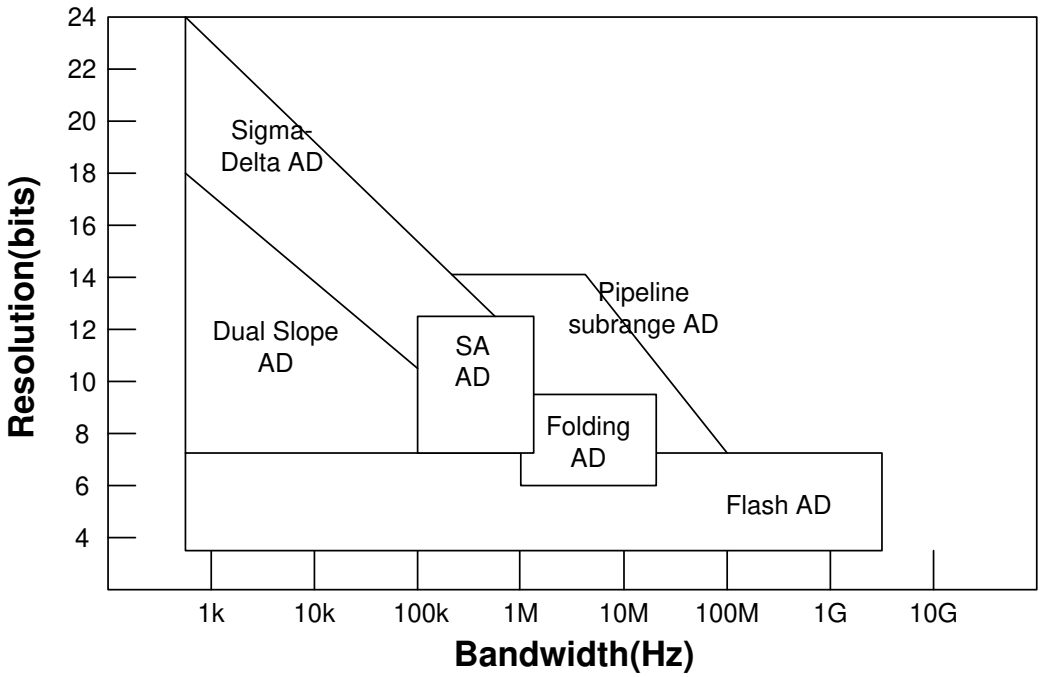

Figure 1-8 Different types of ADCs based on the resolution and conversion rate [7]

- **Latency:** As foregoing analysis shows, utilizing Multi Slope AD converter decreases measuring time a lot. This can also be proved in Figure 1-7, where time period T_4 is the minimum discharging time to reach *N* bits resolution by utilizing Dual Slope AD converter.

Disadvantage

One drawback of Multi Slope AD converter is the high specifications of the comparator. In order to get *N* bits resolution, the comparator needs to compare small signals, which are $\frac{V_{out}}{2^N}$, during time $T_{sampling}$.

1.2.4 Comparison and Final solution

The comparison of the three different types of AD converter showed that each one has its own advantages and disadvantages. According to my specifications, I choose Multi Slope AD converter as my approach. In this work, I have developed a capacitive-sensor interface, using AMS 0.35-μm CMOS technology.

1.3 Organization of the Thesis

The remainder of this thesis consists of four chapters, presenting different aspects of the investigation and the design process.

Following this introductory chapter, Chapter 2 predominantly deals with the architecture-level analysis and the design of the proposed readout approach. Target specifications, operating principles of different sub-blocks (front-end circuit, comparator and counting circuitry), proposed architectures, error analysis in several aspects and finally, sub-block design requirements will be given in chapter two.

The circuit-level analysis and design of the capacitive-sensor interface are presented in Chapter 3. The proposed circuit will be discussed in several sub-sections, including the charge amplifier, dynamic comparator and switches. The simulation results are also presented and analyzed in this chapter. Apart from the analog design and the simulation results, the digital design is similarly introduced.

In Chapter 4, the measurement results are shown, including the fabricated chip, measurement setup and analysis of the measurement results.

Finally, in Chapter 5, conclusions are drawn and the main contributions of this work are summarized. Some recommendations for future research are also presented.

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Chapter 2

Architecture-level Analysis and Design

In this chapter, the architecture-level analysis and design of the proposed approach are presented in six sections: target specifications; the operating principles of an existing CDC; the operating principles of this work, including the front-end operation, discharge operation and counting circuitry operation; error analysis, which consists of thermal noise, quatization noise, flicker noise, offset and comparator delay; three measuring modes; conclusions.

2.1 Target Specifications

The main task of this thesis is to optimize an existing CDC [1] for low power consumption. A performance summary of CDC reported in [1] and the expectations of this work are shown in Table 1.

Table 1 Performance summary and expectations

	CDC in [1]	This work
Power(analog part)	215mW	10mW
Supply Voltage	$\pm$9V	3.3V
Conversion Time	63.2us	50us
Sensor Capacitance Range	1pF	10pF
Resolution	12 bits	15 bits

2.2 Existing CDC Principle

The CDC reported in [1] achieves high accuracy and excellent stability by carefully cancelling out different sources of errors and utilizing two high precision resistors as references. The operating principle of this CDC will be briefly introduced.

2.2.1 Operating Principle

Figure 2-1 shows the circuit schematic. The entire circuit is designed to obtain the value of the unknown capacitor (C_x) by measuring the transferred charge at the sensing electrode. When changing the voltage at the excitation electrode with a predetermined value, there are some charge transferred to the input amplifier (A_1) and amplified. Then the amplified charge is collected by an integrator (A_2). It is calculated by utilizing a specified value of charge with opposite polarity, which is generated by the charge generators, to drive the output voltage of the integrator (A_2) to be 0V. The integrator output is monitored with a comparator (A_3) and the comparator output controls the reference charge polar. A 15 bits Up/Down counter is used to count the precise value of reference charge. Therefore, knowing the

amount of reference charge, the gain of the input amplifier and the excitation voltage, the unknown capacitance can be calculated.

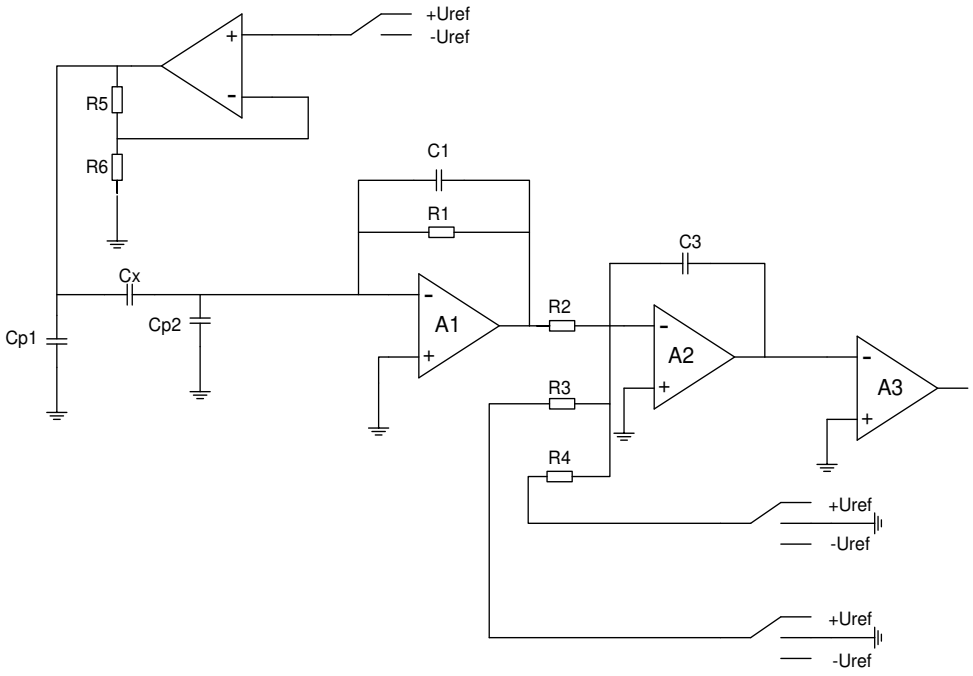

Figure 2-1 Electrical schematics of analog part [1]

2.2.2 Timing Diagram

The timing diagram is depicted in Figure 2-2.

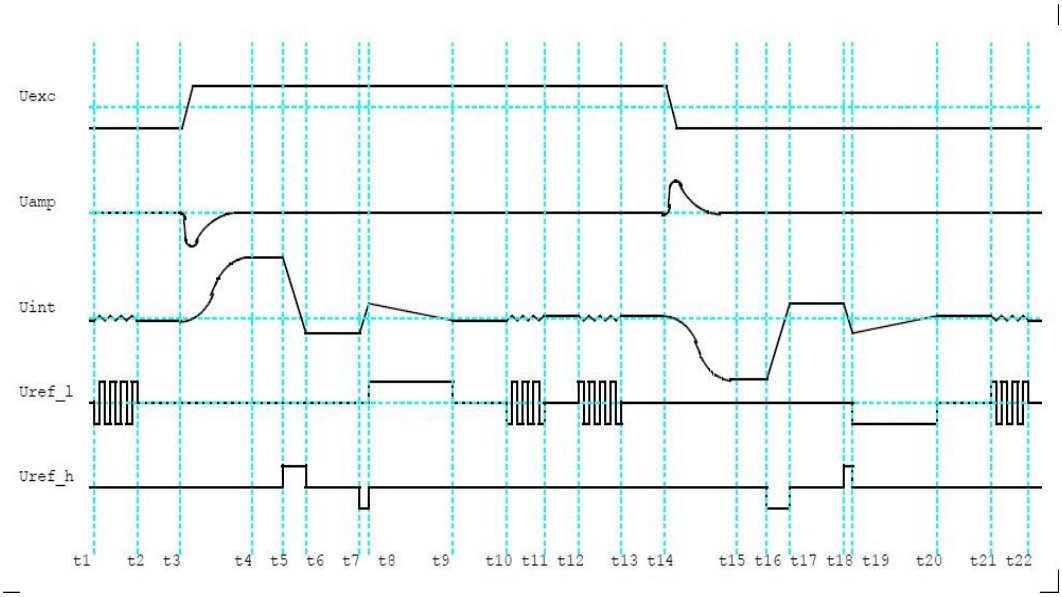

Figure 2-2 Timing diagram [1]

The description of timing diagrams is as follows:

- $t_1 - t_2$: In order decrease the effect of noise, the Control Logic utilizes Fine Charge Generator to keep the output voltage of integrator A_2 around 0V.

- $t_3 - t_5$: The excitation voltage U_{EXC} turns on from its negative value to its positive value, so that a predetermined value of the charge stores on the unknown capacitor C_x. Then the charge transfers to the input amplifier (A_1) and capacitor C_1. Capacitor C_1 starts to discharge through resistor R_1 and the charge amplifies via resistor R_2. The amplified charge is stored in capacitor C_3.

- $t_5 - t_6$: The system starts to use coarse charge generator to discharge capacitor C_3.

- $t_6 - t_7$: When the output voltage of the integrator (A_2) goes below ground, the discharging operation stops.

- $t_8 - t_{12}$: The system starts to utilize fine charge generator to discharge capacitor C_3.

- $t_{12} - t_{22}$: This time interval is the second half cycle of the measurement, which charges the unknown capacitor in the opposite direction.

These time intervals are controlled by an off-chip CPLD.

2.3 Operating Principles

This section describes the operating principles of the proposed architecture for the interface circuit depicted in Figure 2-3, where each functional block is presented with a simplified electronic circuit. The functional blocks are: front-end circuit, comparator, coarse charge generator, fine charge generator and counting circuit. Two reference charge generators are used to reduce the conversion time, i.e. to increase the measurement speed.

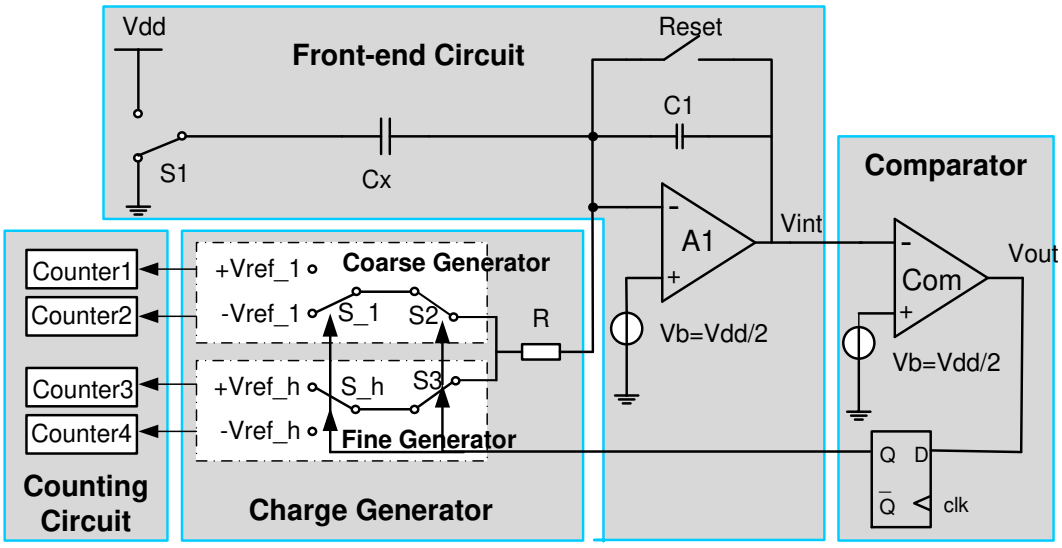

Figure 2-3 Proposed architecture

The main function of the circuit is to obtain the value of the unknown capacitor C_x by measuring the transferred charge at the sensing electrode (the right electrode of C_x in Figure 2-3), which is fixed to a potential $\sim V_{bias}$ provided by the integrator A_1. When changing the voltage level at the excitation electrode (the left electrode of C_x in Figure 2-3), C_x is re-charged with a charge Q_x which flows to the inverting input of the integrator A_1 and is stored in the feedback capacitor C_1. This unknown charge is afterwards compensated by utilizing the same value of charge with opposite polarity, which is generated by the charge generator. The role of the compensating charge is to drive the output voltage of the integrator back to its initial value by removing completely the unknown charge fromC_1. The polarity of the compensation charge is controlled by the comparator, which is controlling the switch of coarse and fine charge compensation. A D-flipflop, which followes behind the comparator, changes its output on the dropping edges of the clock. Its output, also called bitstream, is a synchronous sequence of 0's and 1's. The bitstream can be simply measured by a counter. The charge generator consists of a precision resistor and four different reference voltages. Switch S_2 is used to choose coarse reference charge generator and Switch S_3 is used for fine reference charge generator.

2.3.1 Front-end Operation

The front-end circuit includes three parts: the excitation source, the feedback capacitor and the Op-Amp.

The front-end circuit operation can be divided into two phases:

- Phase 1: Reset the circuit

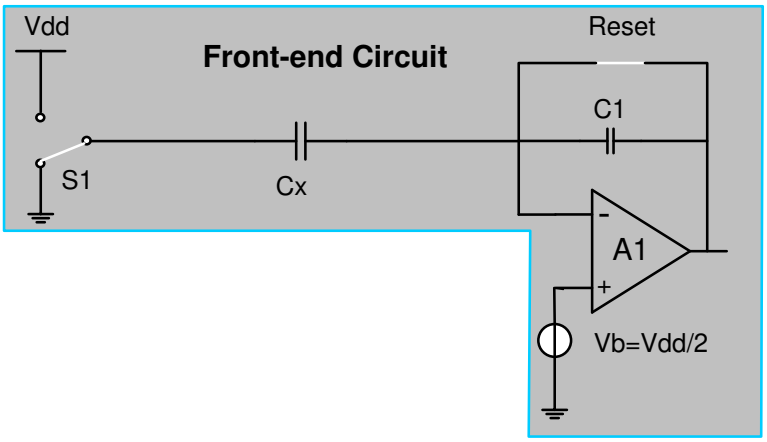

Figure 2-4 Front-end operation in phase 1

In phase1, switch Reset is closed to put the integrator in unity-gain mode (Figure 2-4). As a result, there is no charge left in capacitor C_1, which means the output voltage of the Op-Amp is set to "virtual ground" V_b.

- Phase 2: Transferring the charge on the capacitive sensor C_x.

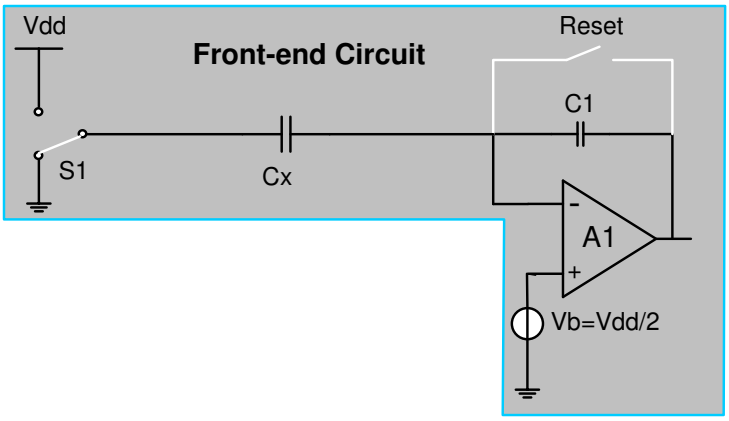

Figure 2-5 Front-end operation in phase 2

In phase2, Switch S_1 chooses ground, the unknown capacitor C_x is charged with Q_x, which can be formulated as:

$$Q_x = -C_x V_b, \quad (2\text{-}1)$$

where V_b is the virtual ground voltage (Figure 2-3). Simultaneously, the identical charge transferred to capacitor C_1. As showed in Figure 2-8, the output voltage of the integrator V_{int} changes to V_1, which can be expressed as:

$$V_1 = \frac{V_b \times C_x}{C_1}. \quad (2\text{-}2)$$

The circuit works as a charge amplifier during this period.

2.3.2 Discharging Operation

The discharging operation is also divided into two phases:

- Phase 1: Coarse charge generator discharging

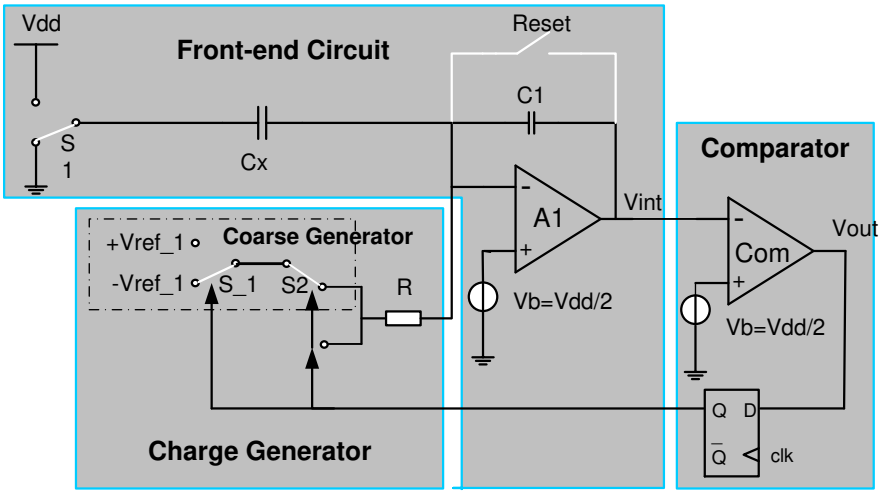

Figure 2-6 Discharging operation in phase 1

In Phase 1, switch S_2 chooses the side with voltages $+V_{ref\_1}$ ($-V_{ref\_1}$). The capacitor C_1 will be discharged by a current I_1, which can be expressed as:

$$I_1 = \frac{\pm V_{ref\_1}}{R}. \quad (2\text{-}3)$$

The polarity of the current is controlled by the comparator and the D-flipflop.

- Phase 2: Fine charge generator discharging

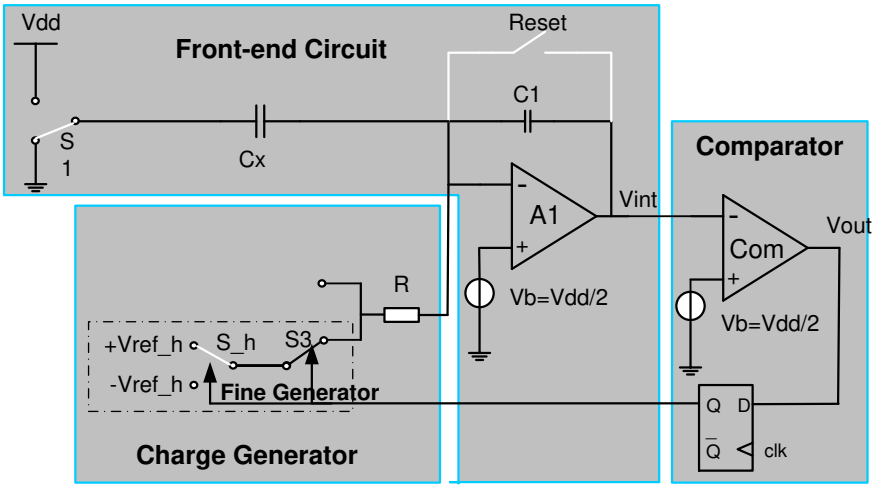

Figure 2-7 Discharging operation in phase 2

In Phase 2, switch S3 chooses the side with voltages $+V_{ref\_h}$ ($-V_{ref\_h}$). The capacitor C_1 will be discharged by a current I_2, which can be formulated as:

$$I_2 = \frac{\pm V_{ref\_h}}{R}, \quad (2\text{-}4)$$

where the current I_2 is 64 times smaller than the current I_1 of coarse charge generator. And its polarity is controlled by the comparator and the D-flipflop.

2.3.3 Comparator and Counting Operation

The bitstream (the output of the comparator) can be simply measured by a counter. The charge can be calculated by (without taking the charge polarity into account):

$$Q_x = N_1 \times T_{sampling} \times I_1 + N_2 \times T_{sampling} \times I_2 \quad (2\text{-}5)$$

where N_1 is the number of clock cycles when the bitstream equals 1 during the coarse discharge operation and N_2 is the number of clock cycles when the bitstream equals 1during the fine discharge operation.

2.4 Error analysis

In reality, there are a number of factors which have an effect on the performance of the interface circuit, such as thermal noise, quantization noise, flicker noise, offset, the comparator time delay.

2.4.1 Thermal noise

Thermal noise is unavoidable at non-zero temperature, here it supposes to be the room temperature *T*. There are three main noise contributors: thermal noise V_{nR} of the precision resistor, input referred voltage noise V_{ni} of amplifier at the non-inverting port and voltage noise V_{ncom} of comparator.

The output referred voltage noise V_{no} can be formulated as:

$$V_{no} = V_{ni} \times \left(1 + \frac{X_{c1}}{R}\right), \quad (2\text{-}6)$$

where X_{c1} is the impedance of capacitor C_1, which can be expressed as:

$$X_{c1} = \frac{1}{jwRC_1}. \quad (2\text{-}7)$$

Assuming f_p is the pole frequency of the low-pass filter created by the integrator, which can be written as:

$$f_p = \frac{1}{2\pi RC_1}. \quad (2\text{-}8)$$

Then the output referred voltage noise V_{no} can be expressed in terms of pole frequency of the low-pass filter:

$$V_{no} = V_{ni} \times (1 - \frac{jf_p}{f}). \quad (2\text{-}9)$$

Here, for simplicity, an infinite gain of the amplifier *A* without feedback is assumed.

The voltage noise V_{nR} of resistor is:

$$V_{nR} = \sqrt{4kTR \times BW}, \quad (2\text{-}10)$$

where BW is the bandwidth of noise, which can be seen as:

$$BW = \frac{\pi}{2} \times \frac{1}{RC_1}. \quad (2\text{-}11)$$

Its referred voltage noise V_{noR} at the output of amplifier is:

$$V_{noR} = -\frac{1}{jwRC_1} \times V_{nR}. \quad (2\text{-}12)$$

The total voltage noise V_{ntot} at the output of the amplifier is:

$$V_{ntot} = \sqrt{V_{no}^2 + V_{noR}^2 + V_{ncom}^2}. \quad (2\text{-}13)$$

2.4.2 Quantization noise

The quantization noise is dependent on the minimum charge $Q_{min} = T_{sampling} \times I_2$ delivered by the fine charge generator. In order to reach *N*-bit resolution, the minimum charge Q_{min} needs to obey following formula:

$$Q_{min} < \frac{Q_{xmax}}{2^N}, \quad (2\text{-}14)$$

2.4.3 Flicker noise and Offset

Flicker noise and offset of the amplifier are the other two principal error sources, which exist in the low frequency part of bandwidth. In order to decrease their effect, a two-step measurement with opposite polarity of the excitation voltage is used. By subtracting the two results, it works as a high-pass filter to cancel all slow-varying input signals, including the offset voltages and the flicker noise below chopping frequency $f_{ch} = \frac{1}{T_{measure}}$, in the meantime, it adds two measurement results to get an average value.

The chopping effect can be simply formulated as:

$$U_{no} \approx \frac{U_{ni}}{1 - \mathrm{j} f_{ch}/f}. \quad (2\text{-}15)$$

2.4.4 Digital Filtering

Except for counting, the counter also works as a Sinc Filter [2], with a transfer function:

$$H\left(e^{j2\pi f}\right) = \frac{sinc(Nf)}{sinc(f)}, \quad (2\text{-}16)$$

where $sinc(f)$ is defined as:

$$sinc(f) = \frac{sin(\pi f)}{\pi f}. \quad (2\text{-}17)$$

The total noise can be filtered by this digital filter.

Taking into account all the filter effects, the total noise V_{N_tot} at the output of the amplifier is:

$$V_{N\_tot} = V_{ntot} \times \left(\frac{1}{1-\mathrm{j}f_{ch}/f}\right) \times \frac{sinc(Nf)}{sinc(f)}. \quad (2\text{-}18)$$

2.4.5 Comparator Delay

Another non-ideality which affects the detection limit is the comparator delay. *A* delay in the comparator causes an error in the final result. Assuming the propagation delay Δt_d of the comparator is between time intervals ΔT_{n-1} and ΔT_n, where ΔT_n can be formulated as:

$$\Delta T_n = n \times T_{sampling}\ (n = 1,2,3 \ldots). \quad (2\text{-}19)$$

The result will lose *n* clock cycles. In the worst case, the bitstream equals 1 during *n* clock cycles. The measured charge Q'_x is:

$$Q'_x = N_1 \times T_{sampling} \times I_1 + (N_2 - n) \times T_{sampling} \times I_2. \quad (2\text{-}20)$$

The detection error ΔQ is:

$$\Delta Q = n \times T_{sampling} \times I_2. \quad (2\text{-}21)$$

Therefore, the best way to achieve high resolution with minimum measuring time is to keep the propagation delay of the comparator (Δt_d) smaller than the sampling time ($T_{sampling}$).

2.5 Measuring Modes

Three measuring modes are discussed in the following parts. A direct comparison of the resolution can be made by comparing Mode 1 and Mode 2, based on the same measurement time. By exploring the performance in Mode 3, the relation between latency and resolution can be studied.

2.5.1 Measuring Mode 1

The timing diagram of Mode 1 is depicted in Fig 2-9.

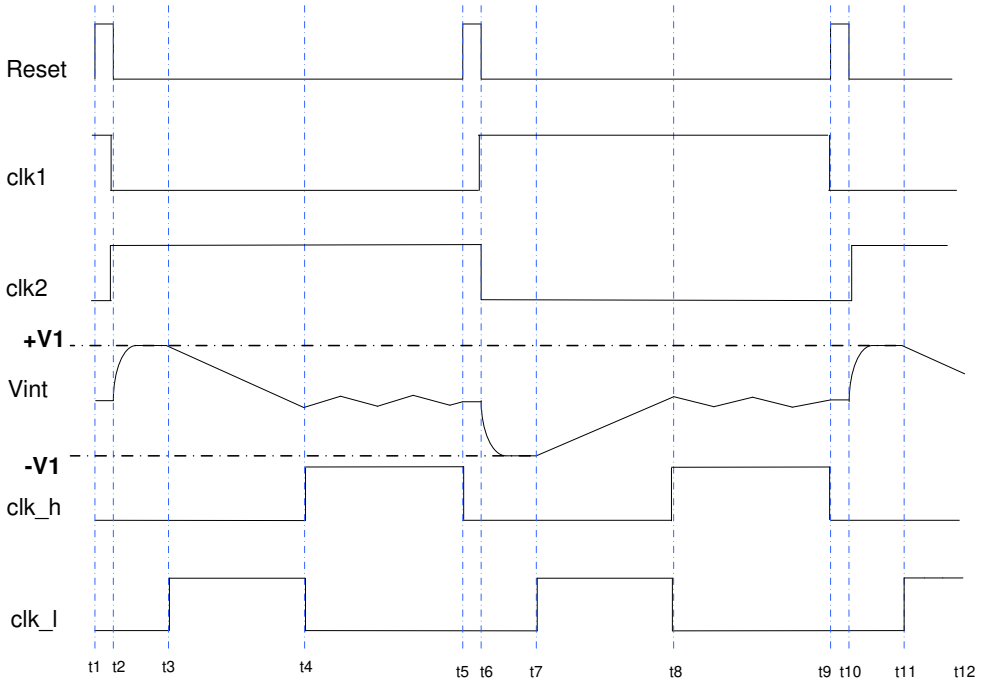

Figure 2-8 Timing diagram of mode 1

The operation of the circuit is as follows:

- $t_1 - t_2$: Switch Reset is closed to reset capacitor C_1, which means there is no charge left in capacitor C_1.

- $t_2 - t_3$: Switch S_1 chooses ground. The unknown capacitor C_x is charged with a certain negative value of the charge. Then the charge will be transferred to capacitor C_1 . The entire system works as a charge amplifier during this period.

- $t_3 - t_4$: Switch S_2 selects voltages $+V_{ref\_1}$. The system starts to use the coarse charge generator to discharge capacitor C_1. The entire system works as an integrator.

- $t_4 - t_5$: After the coarse charge generator pumps out an amount of charge from C_1 to force the output voltage of the integrator first across V_b, the fine charge generator is switched on at the moment t_4. The time interval $t_3 - t_5$ is a fixed period, which means the fine charge generator still works to keep the output of the integrator around "virtual ground", after it expels all the charge from capacitor C_1. By doing so, it can decrease the effect of noise.

- $t_5 - t_9$: During this time interval, the second half cycle of the measurement takes place, which repeats the identical sequences but with opposite polarity.

2.5.2 Measuring Mode 2

The timing diagram is presented in Fig 2-9.

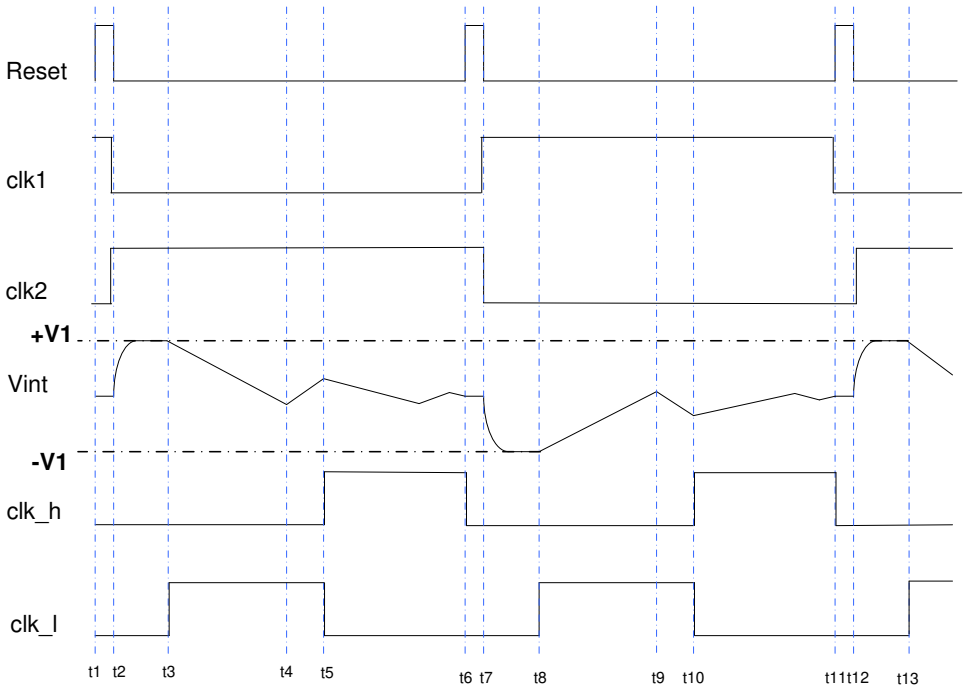

Figure 2-9 Timing diagram of mode 2

The operation of the circuit is as follows:

- $t_1 - t_2$: Switch Reset is closed to set the output voltage of the integrator to "virtual ground".

- $t_2 - t_3$: Switch S_1 selects ground to charge the unknown capacitor C_x with a definite negative value of charge. Therefore, the charge will be transferred to feedback capacitor C_1 .

- $t_3 - t_4$: Switch S_2 chooses voltage $+\mathrm{V_{ref\_1}}$, which means that the coarse charge compensation takes place during this time interval. The capacitor C_1 is discharged by the coarse charge generator to discharge. The circuit operates as an integrator.

- $t_4 - t_5$: After the coarse charge generator pumps out an amount of charge from C_1 to bring the output voltage of the integrator first across V_b, the coarse charge generator continues to discharge capacitor C_1 2 clock cycles with opposite polar charge.

- $t_5 - t_6$: The fine charge generator starts to work at the moment t_5. Just like the time period $t_3 - t_5$ in Mode 1, this is also a preset time interval.

- $t_6 - t_{11}$: During this time interval, the second half cycle of the measurement takes place. All the operation is repeated in the same sequences but with opposite polarity.

2.5.3 Measuring Mode 3

Fig 2-10 displays the timing diagram of measuring Mode 3.

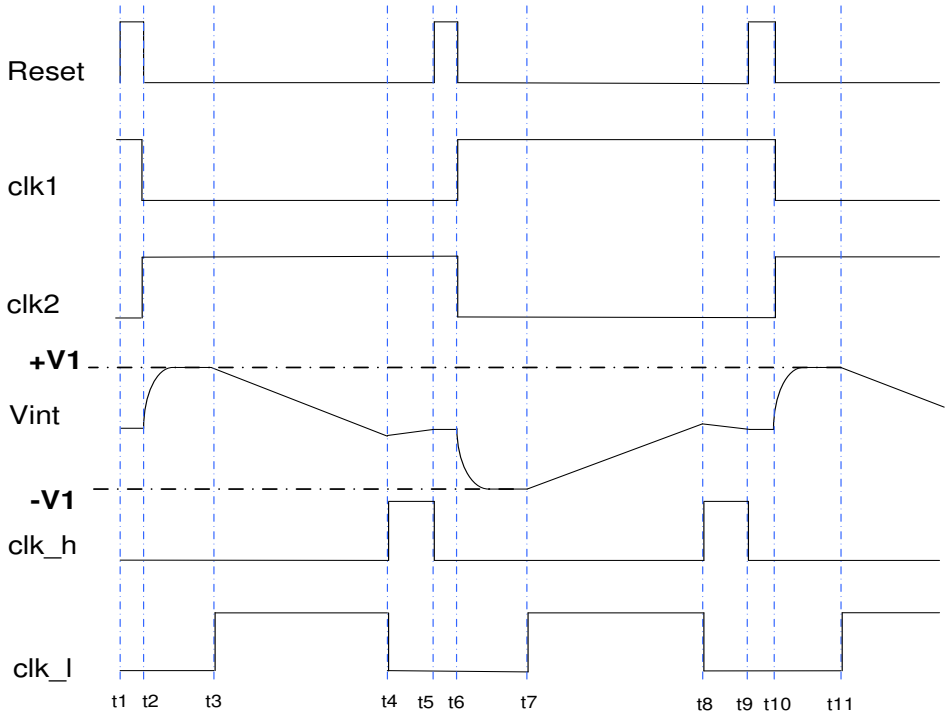

Figure 2-10 Timing diagram of mode 3

The operation of the circuit is as follows:

- $t_1 - t_2$: Switch Reset is closed to put the integrator in unity-gain. As a result, the output voltage of the integrator is set to "virtual ground".

- $t_2 - t_3$: Switch S_1 chooses ground. The unknown capacitor C_x is charged an accurate negative value of charge. Then the charge will be transferred to capacitor C_1. The whole system works as a charge amplifier during this period.

- $t_3 - t_4$: Switch S_2 selects voltages $+\mathrm{V}_{\mathrm{ref\_1}}$. The system starts to use coarse charge generator to discharge capacitor C_1. The whole system works as an integrator.

- $t_4 - t_5$: After the coarse charge generator pumps out an amount of charge from C_1 to bring the output voltage of the integrator first across V_b, the fine charge generator starts to work at the moment t_4. Unlike fine discharge operation in Mode 1 and Mode 2, this operation will stop when expelling all the charge from capacitor C_1.

- $t_6 - t_9$: During this time interval, the second half cycle of the measurement takes place, which repeats the similar sequences but with opposite polarity.

2.6 Conclusions

In this chapter, the architecture-level analysis and design of the read-out circuit have been demonstrated. At first, a former work [1] with high accuracy and excellent thermal stability has been briefly discussed. Followed by the operating principles of the front-end circuit, the discharge operation and the comparator and counting circuit have been introduced. To arrive at the requirements for the detection limits, the major error sources and digital filtering effect have been analyzed, including thermal noise, quantization noise, flicker noise and offset and comparator delay. Based on all these, three distinct measurement modes are discussed.

References

[1] R. Nojdelov, S. Nihtianov. “Capacitive-Sensor Interface With High Accuracy and Stability”, IEEE Transactions On Instrumentation And Measurement, Vol. 58, May 2009.

[2] R. Schreier, G. C. Temes, “Understanding Delta-Sigma Data Converters”, A John Wiley & Sons Inc., 2004

Chapter 3

Circuit-level Analysis and Design

In this chapter, circuit-level analysis and design of the interface circuit are presented in three parts: charge amplifier design, dynamic latch comparator design and switch design. After that, simulation results are given, with a conclusion in the end.

3.1 Op-Amp Design

Before designing the amplifier, the first thing to be done is to choose the most suitable topology for the Op-Amp according to the specifications. The specifications: open-loop gain, settling time and thermal noise of the Op-Amp, are calculated in section 3.1.1. Depending on these specifications, a class AB two stage Op-Amp topology is discussed in section 3.1.2.

3.1.1 Specifications

Open-loop Gain

Considering the charge amplifier as a non-ideal Op-Amp, it is shown in Figure 3-1.

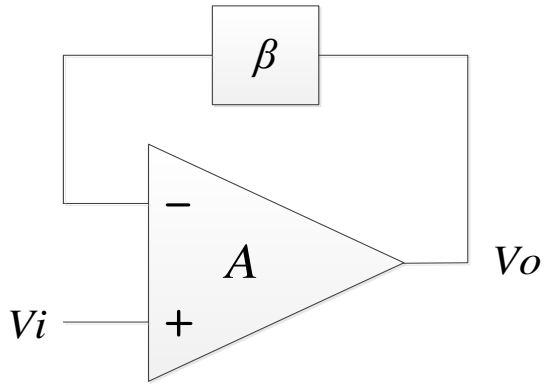

Figure 3-1 A Non-ideal Op-Amp with a Feedback

Its output voltage V_o is:

$$V_o = V_i \cdot \frac{1}{\beta}\left(1 - \frac{1/\beta}{A+1/\beta}\right), \quad (3\text{-}1)$$

where β is the feedback factor. The output voltage can be also formulated as:

$$V_o = V_{o,ideal} - \frac{1/\beta}{A+1/\beta} \cdot V_{o,ideal}, \quad (3\text{-}2)$$

where $V_{o,ideal}$ is the output voltage of an ideal Op-Amp.

In order to get 15-bit precision, the error part V_{err} caused by a non-infinite open-loop gain should be smaller than $\frac{V_{o,ideal}}{2^{15+1}}$, the error voltage V_{err} can be expressed as:

$$V_{err} = \frac{1/\beta}{A+1/\beta} \cdot V_{o,ideal}. \quad (3\text{-}3)$$

This means:

$$A \times \beta + 1 > 2^{15+1}. \quad (3\text{-}4)$$

Supporting the feedback factor β is 1, the equation can be written in another way:

$$A \geq 96.3dB. \quad (3\text{-}5)$$

Settling Time

There are two factors defining the value of the trans-conductance (g_m) of the amplifier: one is settling time, the other is thermal noise (as discussed in section 2.4, thermal noise is the main part of noise). Figure 3-2 shows that the settling time *t* should be smaller than 14μs in Measuring Mode 3, otherwise, the output voltage of the integrator will not settle with the required accuracy during the measurement time of one half cycle, which is 15μs.

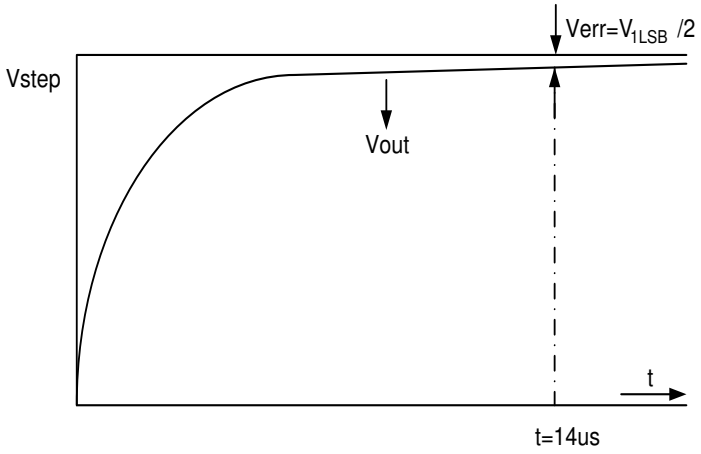

Figure 3-2 Slew rate

The output voltage of the Op-Amp can be expressed as:

$$V_{out} = V_{step}\left(1 - e^{-\frac{t}{\tau}}\right). \quad (3\text{-}6)$$

As Figure 3-2 shows, the error voltage V_{err} should not be larger than half of the Least Significant Bit voltage, which means:

$$V_{err} \leq \frac{V_{1LSB}}{2}, \quad (3\text{-}7)$$

where the error voltage V_{err} can be formulated as:

$$V_{err} = V_{step}e^{-\frac{t}{\tau}}, \quad (3\text{-}8)$$

where τ is the time constant of the Op-Amp, it can be written as:

$$\tau \leq \frac{t}{(N+1)ln2}. \quad (3\text{-}9)$$

The load capacitance of the charge amplifier is calculated in the following way:

$$C_{load} = C_1 \times \frac{C_x}{C_x + C_1}. \quad (3\text{-}10)$$

The feedback factor β is:

$$\beta = \frac{C_1}{C_x + C_1}. \quad (3\text{-}11)$$

The time constant τ is:

$$\tau = \frac{2\pi C_{load}}{\beta g_m} = \frac{2\pi C_x}{g_m}. \quad (3\text{-}12)$$

So the trans-conductance (g_m) of the amplifier can be formulated as:

$$g_m = \frac{2\pi C_x}{\tau}. \quad (3\text{-}13)$$

Thermal Noise

Since the main part of the thermal noise of this amplifier is affected by the trans-conductance of the input transistor pair, the formula of the input noise density is:

$$S_{in}^2 = \frac{2\times 4KT}{3\times g_m}. \quad (3\text{-}14)$$

Considering these two factors, the trans-conductance (g_m) of the amplifier should be chosen a proper value. Depending on the thermal noise level, the value of g_m should be 200μS.

3.1.2 Design Approach

Choice of Topology

Choosing a most suitable topology, which satisfies the specifications, is the first step before designing the Op-Amp. With reference of Table 2 [1], the two stage architecture is a solution to build the charge amplifier to get a large open-loop gain and a large swing.

Table 2 Comparison of various Op-Amp topologies

	Gain	Output Swing	Speed	Power	Noise
Telescopic	Medium	Medium	Highest	Low	Low
FoldedCas	Medium	Medium	High	Medium	Medium
Two-Stage	High	Highest	Low	Medium	Low
GainBoost	High	Medium	Medium	High	Medium

Two Stage Considerations

As Figure 3-3 depicts, Stage 1 has a high open-loop gain which should be above 70~80dB to provide enough gain to reduce the non-linearity effects. Therefore, a folded cascode topology is choosen as the first stage to provide high gain. For high swing considerations, the common source topology is usually used as the second stage. A single common source MOSFET can give a 14~40dB gain[2]. The total gain of the two-stage op amp should be enough to exceed 96.3dB.

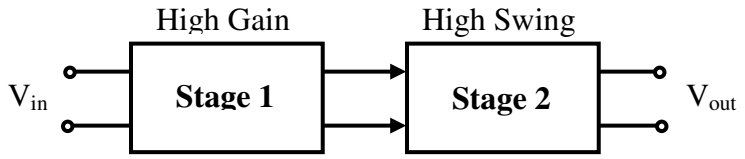

Figure 3-3 Two-stage Op-Amp

3.1.3 Operational Amplifier Design

1st Stage Amplifier Design

As mentioned in the analysis above, in the first stage, a relatively high gain is essential. One way to achieve this goal is by using telescopic topology. In order to alleviate the drawbacks of "telescopic" cascode Op-Amps, which have a limited output swing and difficulty in shorting the input and output, a "folded cascode" Op-Amp (Figure 3-4) can be utilized.

Compared with "telescopic" cascode, the overall voltage swing of a folded cascode op amp is slightly higher than that of a telescopic configuration, since the difference of the overdrive of the tail current source.

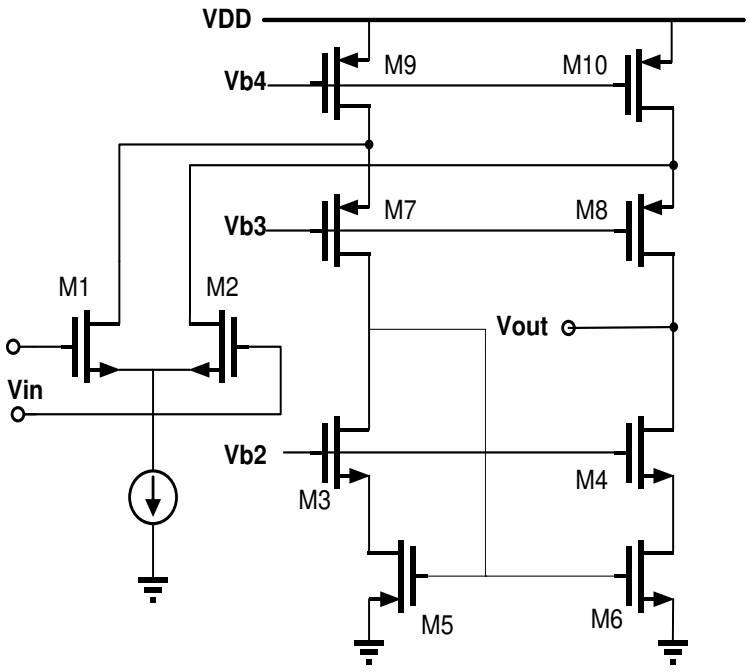

Figure 3-4 Folded cascode Op-Amp with cascode PMOS loads

From section 3.1.1, the trans-conductance g_m of the input pair of the 1st stage can be approximately known.

2nd Stage Amplifier Design

Moving to the next stage, as analysis above, this stage is mainly used for deriving a larger output voltage swing. In general, the second stage is typically configured as a simple common-source stage so as to allow maximum output swings.

In this type of design, the peak current swing never exceeds the DC biasing current. It means the power consumption must be really large when the second stage needs large quiescent current. For this reason, a Miller-compensated class AB, which has small quiescent currents but can deliver very large currents to the load, is shown in Figure 3-5.

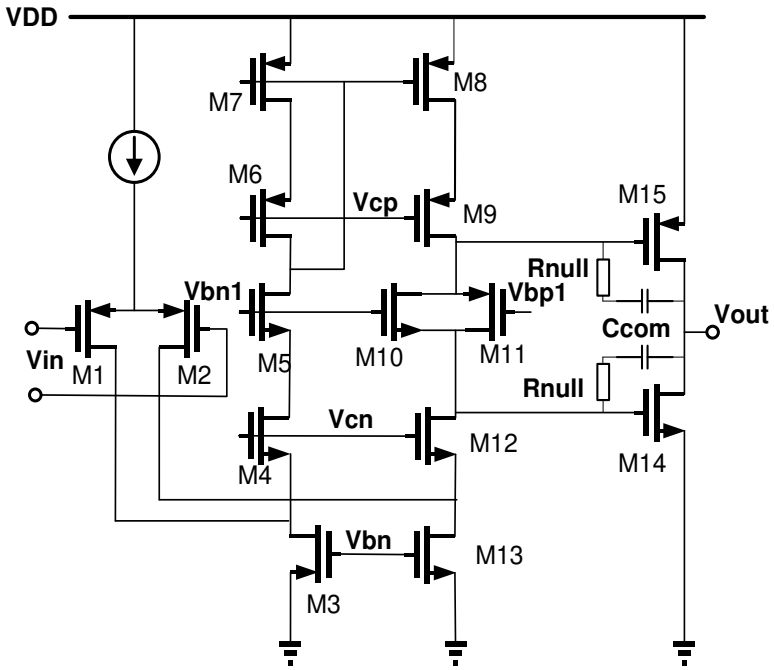

Figure 3-5 Two-stage Op-Amp employing folded-cascode in class AB

In this circuit, the compensation capacitance C_{com} is no longer directly connected between the output and input of the second stage. A small resistor R_{null} is inserted in series with C_{com}, which can also help to abolish the 2nd pole. The expression of the pole is now modified as shown.

$$f_{2nd} = \frac{1}{2\pi C_{com}(1/g_{m2} - R_{null})}, \quad (3\text{-}15)$$

where g_{m2} is the trans-conductance of the MOSFET in the second stage. It is clear that for a resistance R_{null} equal to $1/g_{m2}$, the pole is at infinity, in another word, it has vanished. However, it is not so easy to match a resistor to a $1/g_{m2}$ value. Therefore, we choose $R_{null} > 1/g_{m2}$, to turn this zero to a negative one, which will not cause Phase Margin problem. We simply position R_{null} between $1/g_{m2}$ and $1/3g_{m1}$, with preference to be closer to $1/3g_{m1}$, where g_{m1} is the trans-conductance of the input pair in the first stage [2].

As Figure 3-5 depicts, a pair of NMOS M_{10} and PMOS M_{11} is used to keep biasing voltage of the output stage around V_{th} to settle the whole circuit quickly.

3.2 Comparator Design

A comparator followed with the charge amplifier is used as a null detector. It will compare the output voltage of the Op-Amp with a reference voltage, which is "virtual ground" in this work. In order to get *N* bits resolution, the comparator should detect a voltage difference as small as V_{min} and respond during the propagation delay (Δt_d). The minimum voltage difference can be expressed as:

$$V_{min} < \frac{Q_{xmax}}{2^N \times C_1}. \quad (3\text{-}16)$$

As discussed in section 2.4.5, the best way to achieve high resolution with minimum conversion time is to keep the propagation delay of the comparator (Δt_d) smaller than the sampling time ($T_{sampling}$). Therefore, a fast dynamic latch comparator is designed in this thesis, which is shown in Figure 3-6. In this comparator, three distinct functions are employed: pre-amplification, positive feedback and the latches.

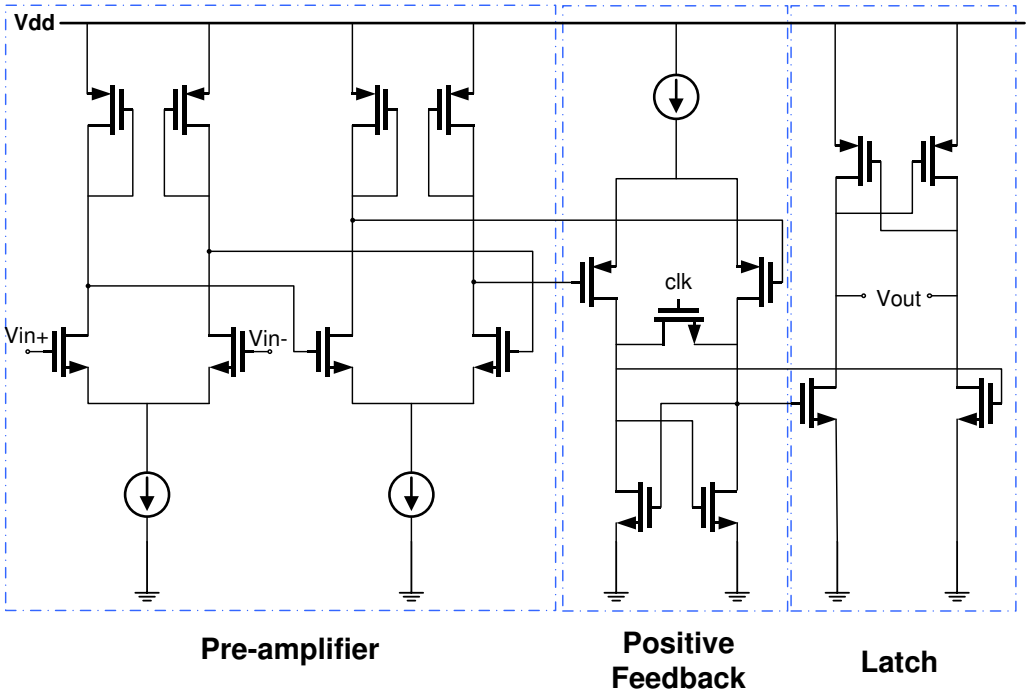

Figure 3-6 Comparator architecture

The first stage is designed for amplifying the input signal to a proper level to make the positive feedback stage work fast. Since this comparator is a fast comparator, the pre-amplifier stage is required to have a relatively large bandwidth. Therefore, a two-stage pre-amplifier is chosen instead of a "telescopic" cascode one. Another benefit of using pre-amplifier stage is to avoid "kick-back noise" effect, which is caused by large voltage variations at internal nodes of comparator [4].

The positive feedback stage is the core of the comparator since it defines the decision point. A NMOS transistor is used as a switch. The comparator works on the dropping edges of the clock.

Another positive feedback stage is used as a latch to convert the output of positive feedback to the logic levels.

3.3 Switch Design

So far, ideal switches with infinite off-resistance, zero on-resistance and no charge injection are assumed to be utilized. However, there are still some errors caused by non-ideal switches, like non-zero on-resistance and charge injection.

During the discharging phase, the on-resistance of switch S2 and S3 will cause a mismatch problem. As discussed in section 2.3.2, the capacitor C_1 will be discharged by a current $I_1 = \frac{\pm V_{ref\_1}}{R}$ in coarse discharge operation, and be discharged by a current $I_2 = \frac{\pm V_{ref\_h}}{R}$ in fine discharge operation. The current I_2 is 64 times smaller than the current I_1 of coarse charge generator.

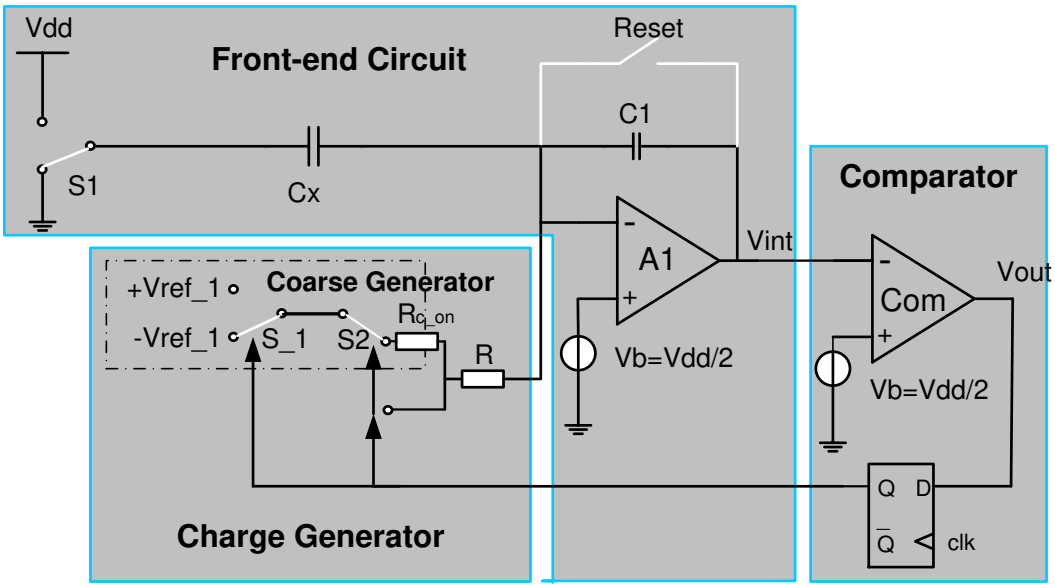

Figure 3-7 Coarse discharge operation

As Figure 3-7 depicts, considering the on-resistance of S2 and S_1 in coarse charge generator, the discharge current I_1 will change to I_1', which can be formulated as:

$$I_1' = \frac{\pm V_{ref\_1}}{R+R_{c\_on}}. \quad (3\text{-}17)$$

The current error ΔI_1 is:

$$\Delta I_1 = I_1 - I_1' = \frac{\pm V_{ref\_1} \times R_{c\_on}}{R(R+R_{c\_on})}. \quad (3\text{-}18)$$

In order to get N_1-bit resolution, the on-resistance $R_{c_on}$of S2 and S_1 should be:

$$|\Delta I_1| \times T_{sampling} < \frac{Q_{xmax}}{2^{N_1}}, \quad (3\text{-}19)$$

Expressed in another way as:

$$R_{c\_on} < \frac{Q_{xmax} \times R^2}{V_{ref\_1} \times T_{sampling} \times 2^{N_1} - Q_{xmax} \times R} \quad (3\text{-}20)$$

It is similar to the on-resistance R_{f_on} of S3 and S_h in fine charge generator, which can be expressed as:

$$R_{f\_on} < \frac{Q_{xmax} \times R^2}{V_{ref\_h} \times T_{sampling} \times 2^{N} - Q_{xmax} \times R} \quad (3\text{-}21)$$

A complementary PMOS-NMOS switch is chosen to be utilized as S2 and S3, because of its relatively stable on-resistance. Just as figure 3-8 shows, a NMOS transistor and a parallel connected PMOS transistor compensate each other's weak conductivity region. The overall on-resistance of the switch over the input voltage range is considerably more flat.

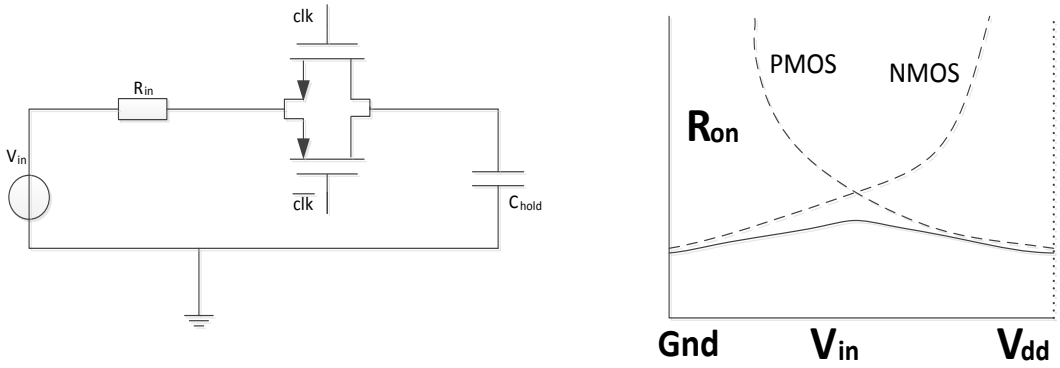

Figure 3-8 Complementary PMOS-NMOS switch [5]

3.4 Simulation Results

In this section, the simulation results of Op-Amp and comparator are shown. A 3.3V DC supply voltage source is used and the "virtual ground" is set to be 1.65V.

3.4.1 Op-Amp

In this section, simulation results of Op-Amp are presented in three parts: AC loop-gain, noise and settling time.

AC Loop-gain

As figure 3-9 demonstrates the loop-gain of this amplifier is approximately 150dB, the bandwidth is about 4.3MHz and its Phase Margin is 81.778°, which means this Op-Amp is stable.

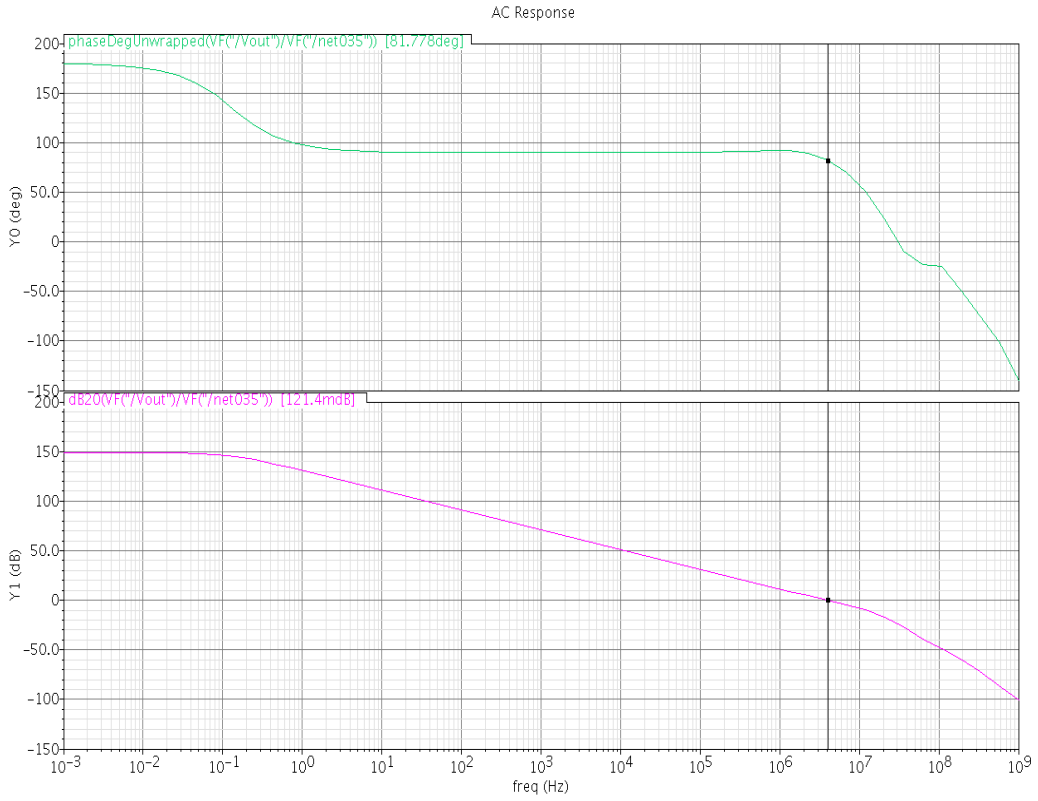

Figure 3-9 Loop-gain of Op-Amp

Noise

The total noise at the input of the Op-Amp including flicker noise and thermal noise is depicted in figure 3-10. By using chopping technique, the flicker noise can be compensated when the noise corner frequency is below the chopping frequency. In this design, the chopping frequency is about 40kHz. It can be seen that the noise corner is lower than 40kHz and the thermal noise at 40kHz is 16.06nV/√Hz.

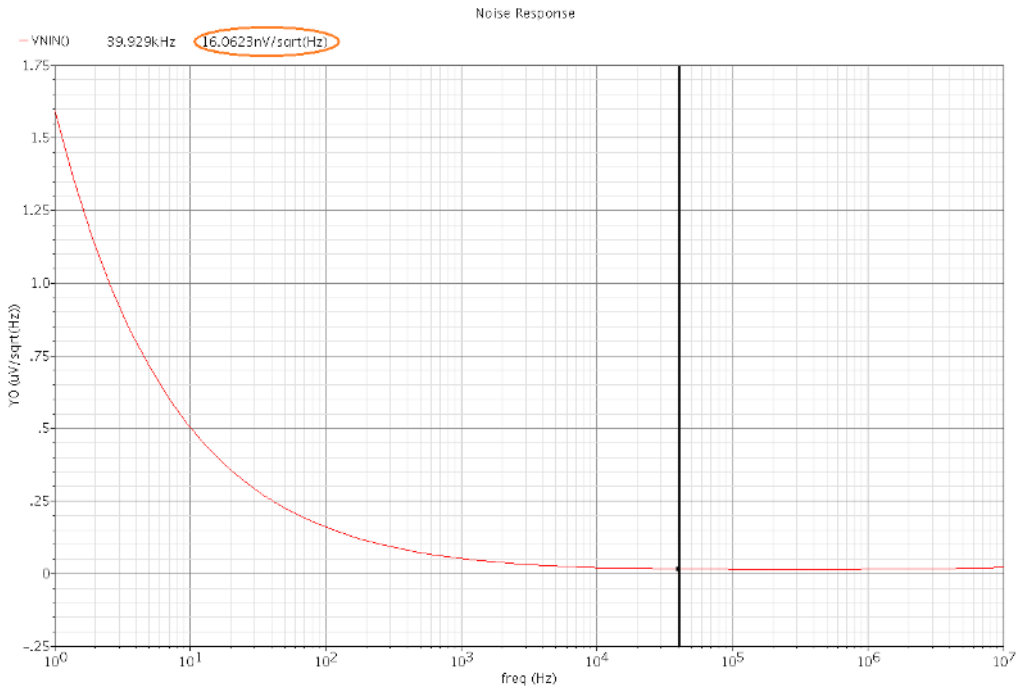

Figure 3-10 Equivalent input noise of the Op-Amp

Settling Time

In order to obtain the settling time *t* of Op-Amp, a 1.65V voltage step is applied. As Figure 3-11 depicts the Op-Amp can get a 15 bits precision after 7.0311μs which meets the specification (discussed in section 3.1.1). After 25μs, which is the

measurement time of one half cycle, the Op-Amp can totally settle down (44.5 bits) which is shown in Figure 3-12.

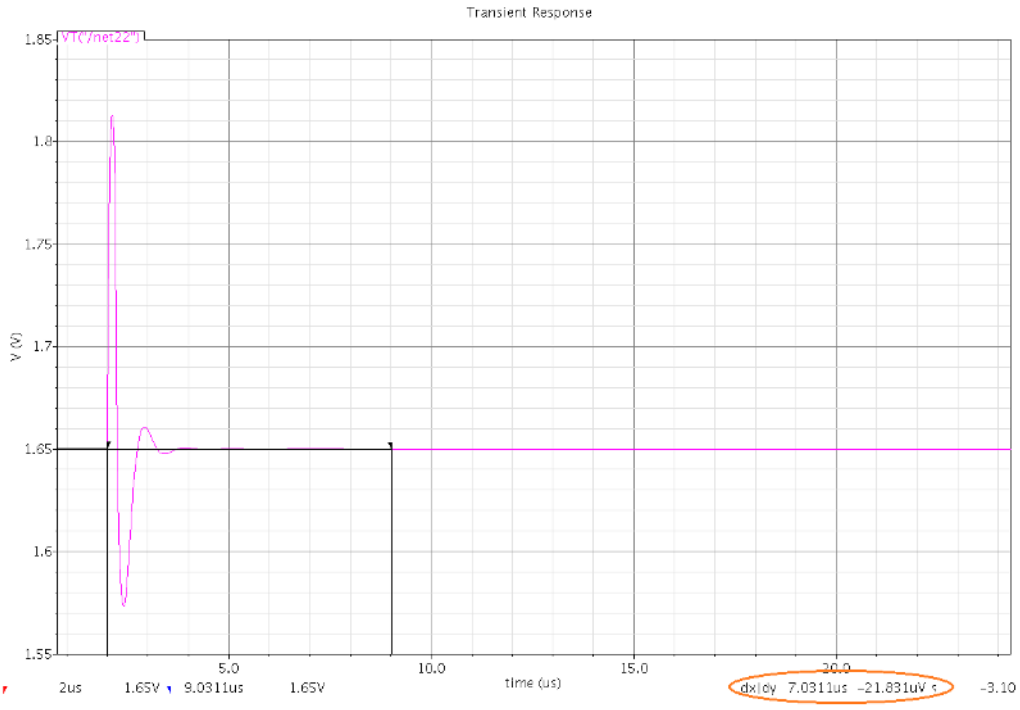

Figure 3-11 Settling time of Op-Amp

3.4.2 Comparator

As section 3.2 discussed, a fast dynamic latch comparator is designed. In order to get its propagation delay time, a 100μV voltage step source and a 25ns clock are offered. As figure 3-13 shows, the propagation delay time is 5.7ns.

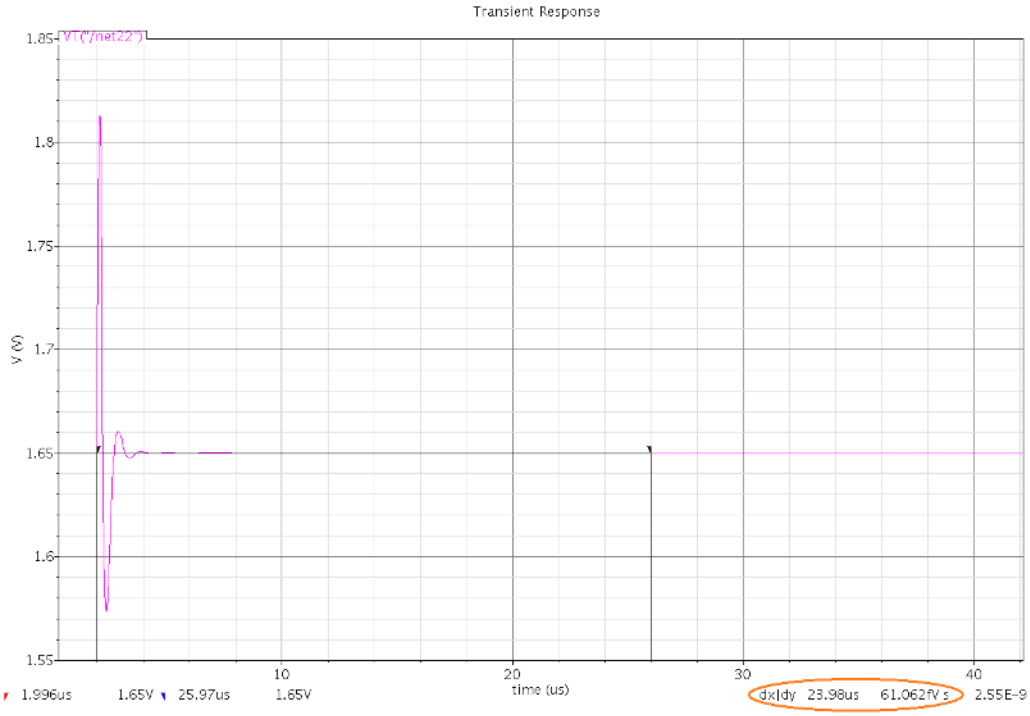

Figure 3-12 Settling time of Op-Amp

3.5 Conclusions

In this chapter, the circuit-level analysis and design of the interface circuit have been introduced. In Op-Amp design, all specifications are discussed and a proper approach is chosen due to these specifications. After this, a fast dynamic latch comparator and switches are introduced. In the end, simulation results are analyzed in two aspects: simulation results of the Op-Amp (AC loop-gain, noise and settling time) and the simulation result of the comparator.

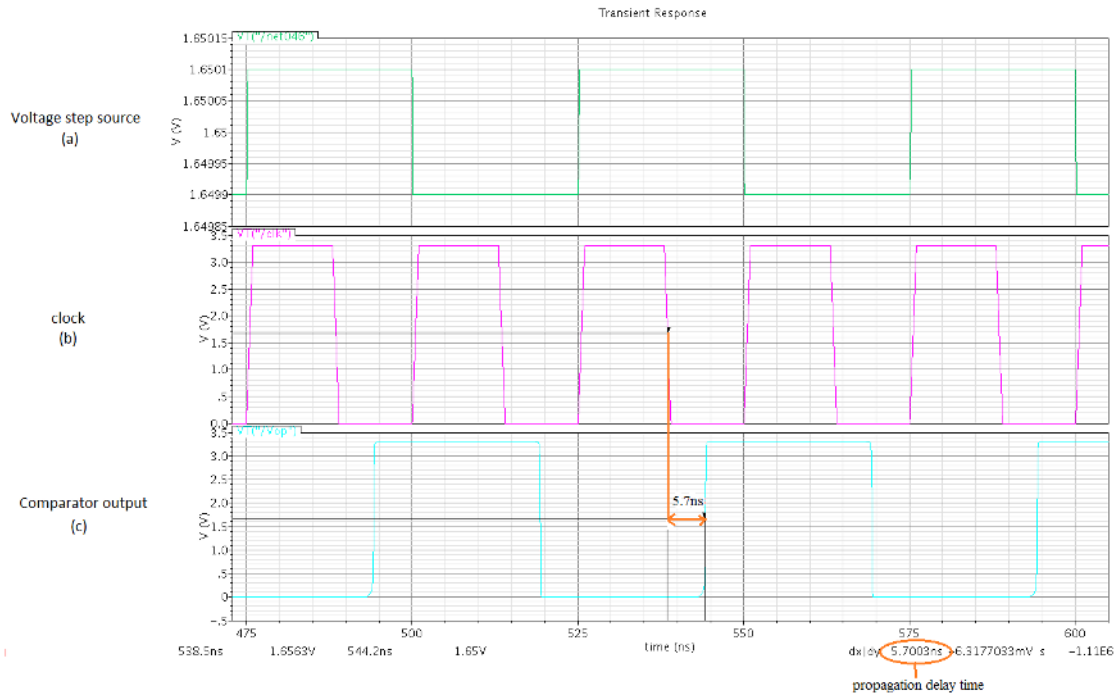

Figure 3-13 Simulation result of comparator

References

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[2] W. M. C. Sansen, "Analog Design Essentials", Spriger Inc., Edition 1, 2008

[3] Q. Fan, J. H. Huijsing, K. A. A. Makinwa, "A 21 nV/√Hz Chopper-Stabilized Multi-Path Current-Feedback Instrumentation Amplifier With 2 μV Offset", IEEE Journal of Solid-State Circuits, Vol. 47, February, 2012

[4] M. R. Nabavi, “Low-power high-performance integrated interface for eddy-current displacement sensors”, PhD thesis, Delft University Technology, August, 2012

[5] M. J. M. Pelgrom, “Analog-to-digital conversion”, Spriger Inc., Edition 1, 2010

Chapter 4

Measurement Results

In this chapter, the measurement results of the CDC based on Multi-Slope ADC interface chip are presented. First, the fabricated chip and the measurement setup, including the circuit layout, test board design and measurement equipment, are introduced. Next, performances regarding the Signal to Noise Ratio (SNR), temperature stability and power consumption are presented. In the end, conclusions of this chapter are drawn.

4.1 Fabricated chip

4.1.1 Circuit layout

A good analog layout plays a vital role in getting a satisfactory performance of the interface circuit. Figure 4-1 shows the chip layout with pad ring.

The distinct functional blocks in the layout are represented by the white dotted box surrounding it. Each box has a unique number from 1 to 5 corresponding to a unique functionality in the circuit, which is listed below:

1. Op-Amp circuit

2. Feedback capacitor

3. Dynamic comparator circuit

4. Digital circuits

5. Analog switches

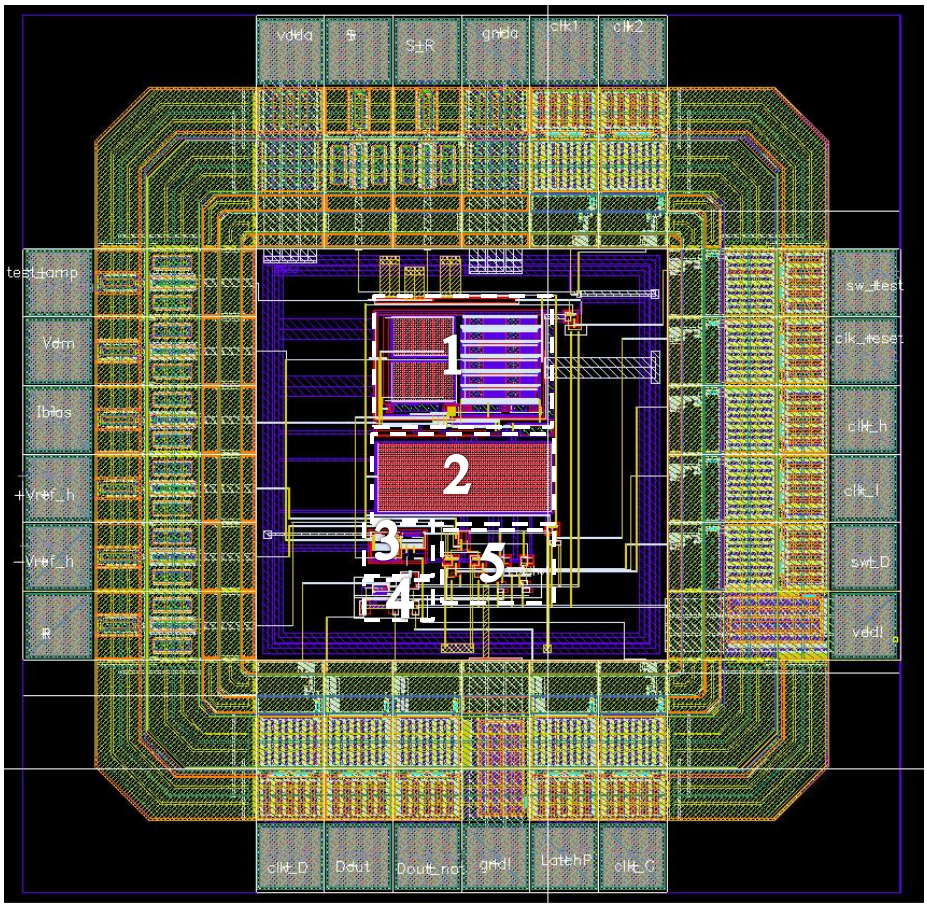


Figure 4-1 Chip layout with pad ring

4.1.2 Chip micrograph

The design is implemented in a 0.35-μm CMOS process, and the chip micrograph is shown in figure 4-2. The chip area is 1.28mm×1.28mm.

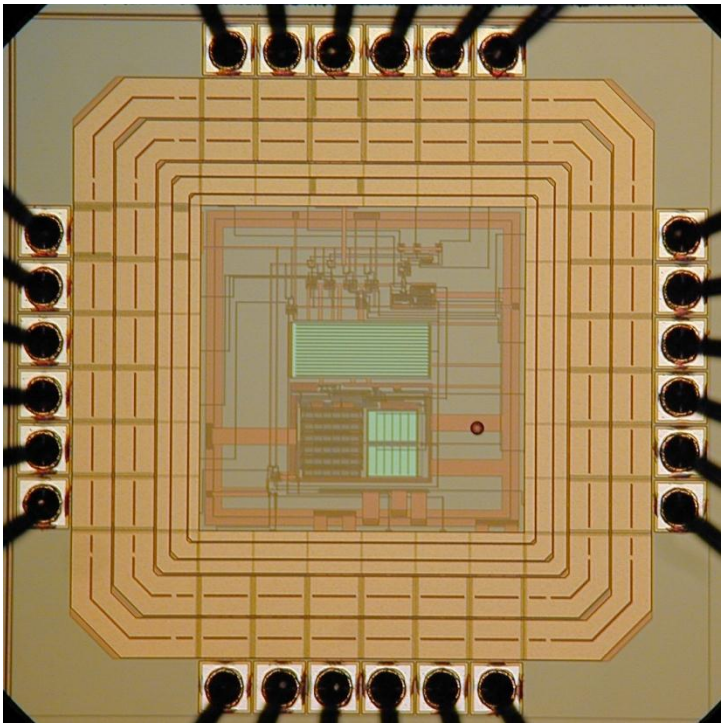


Figure 4-2 Chip micrograph

4.2 Measurement setup

4.2.1 Printed Circuit Board (PCB) Design

In order to perform the measurements, a PCB is designed and fabricated as a test board for the measurement. The PCB is designed by an experienced designer named Roumen Nojdelov. The test PCB is shown in Figure 4-3. The complete schematics are demonstrates in Appendix A.

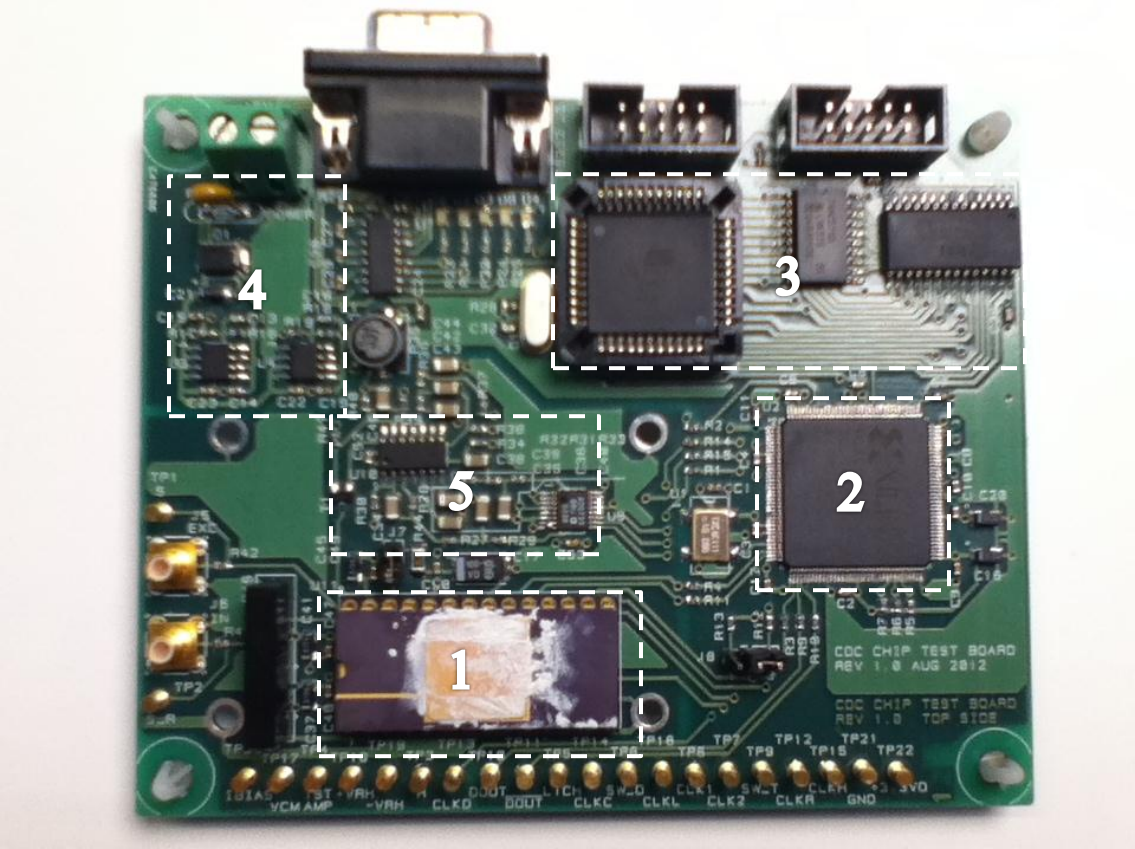


Figure 4-3 Photo of test board

The different functional blocks in the PCB are represented by the white dotted box surrounding it. Each box has a unique number from 1 to 5 corresponding to a unique functionality in the circuit, which is listed below:

1. Analog Part:

This is the main part of the thesis. It has been described in detail in Chapter 2 and Chapter 3. The chip layout with pad ring is showed in Figure 4-1.

2. Complex Programmable Logic Device (CPLD):

CPLD is used to generate different clock signals for the chip and count the integrator discharge cycles. Four counters are implemented in the CPLD:

Counter C_0: This counter counts clock cycles during the first half-cycle when the coarse discharging is enabled.

Counter C_1: This counter counts clock cycles during the second half-cycle when the coarse discharging is enabled.

Counter F_0: This counter counts clock cycles during the first half-cycle when the fine discharging is enabled.

Counter F_1: This counter counts clock cycles during the first half-cycle when the fine discharging is enabled.

3. Micro Control Unit (MCU):

The MCU is used for communication with the PC via RS 232.

4. Power Supply:

The external power supplies 5V DC voltage for the test board. Then Power Supply part generates 3.3V for all the chips.

5. Reference Voltage Generator:

The reference voltages $\pm V_{ref\_h}$ and Common mode voltage V_{cm} are generated from the analog power supply with Pulse Width Modulation (PWM), analog switches and low pass filters are used to achieve the necessary accuracy.

4.2.2 Equipment

Several equipment have been used to do the measurement. A photo including all the measurement equipment is shown is Figure 4-4.

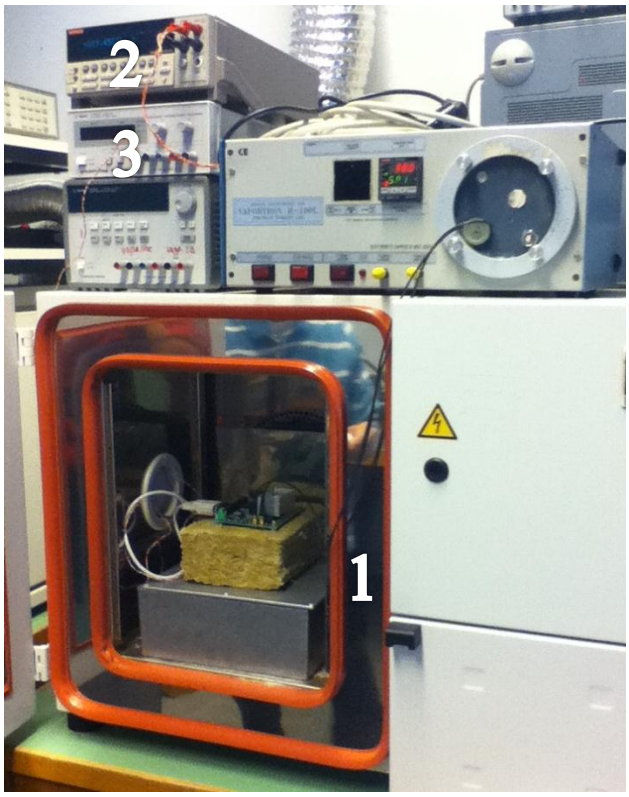


Figure 4-4 A photo of the measurement equipment

Equipment 1 to 3 are listed below:

1. Oven:

This oven is used for temperature stability measurement. The temperature can be monitored and controlled by computer.

2. Digital Multi-meter:

The digital multi-meter is used to measure the temperature of the chip.

3. Power Supply:

The power supply provides positive supply +5V and ground (gnd) for the test board.

4.3 Experimental Results

In this chapter, performances regarding: Signal to Noise Ratio (SNR), temperature stability and power consumption are tested. As discussed in section 2.5, three measuring modes are designed. In this section, all the measurements are made with Mode 2. Mode 3 is only used for testing purpose. Since it is impossible to find a capacitive sensor with proper value, a normal capacitor is used to emulate the sensor.

4.3.1 Signal to Noise Ratio

At first, the SNR for the test board is tested. Figure 4-5 shows the noise spectrum with conversion time 50μs. The achieved SNR is 112dB.

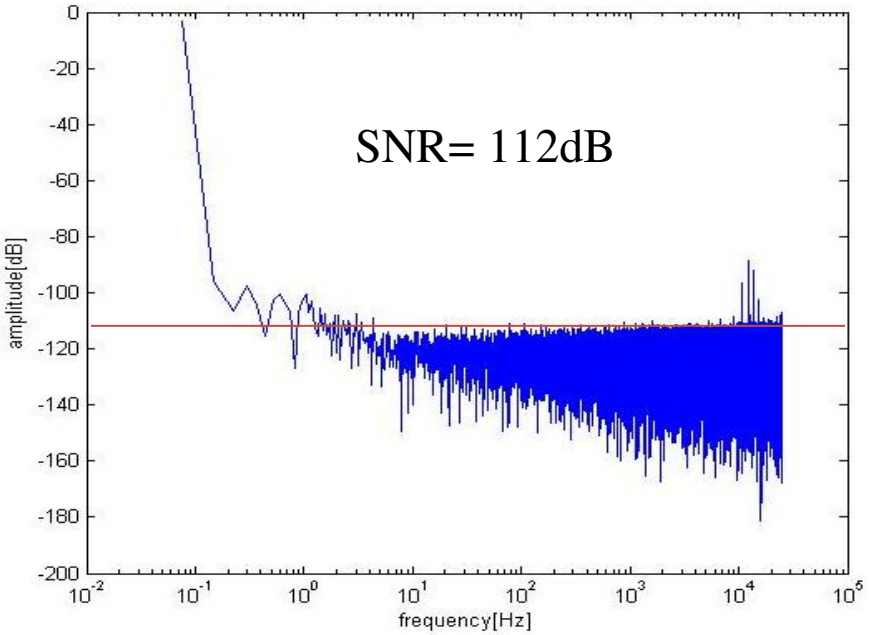


Figure 4-5 Noise spectrum with conversion time 50µs

4.3.2 Temperature Stability

The next experiment is focused on the temperature stability of the test board. As discussed in section 1.1.2, the capacitance to digital converter needs a good stability in a temperature varying environment. Firstly, the test board including the capacitive sensor is placed in the oven, where the temperature varies from 10℃ to 50℃. Figure 4-6 shows the measurement results.

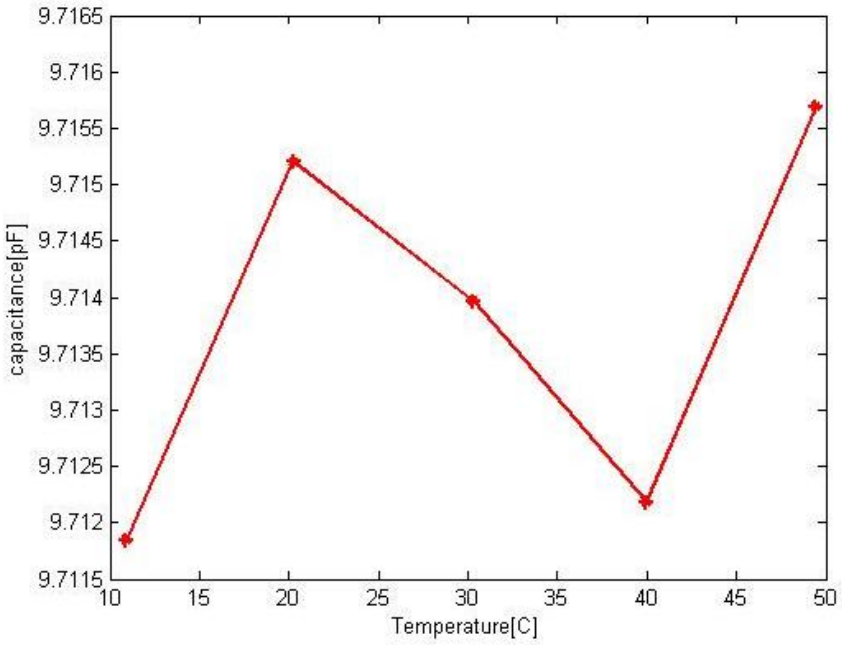


Figure 4-6 Thermal Stability of the CDC

Because the capacitive sensor is also placed in the oven, its value changes dependent on varying temperature. In order to know the temperature coefficient of the capacitive sensor, a reference test board is used in this measurement. This reference test board can reach 3.6ppm/℃ temperature coefficient [1]. Figure 4-7 shows the thermal stability of the capacitive sensor.

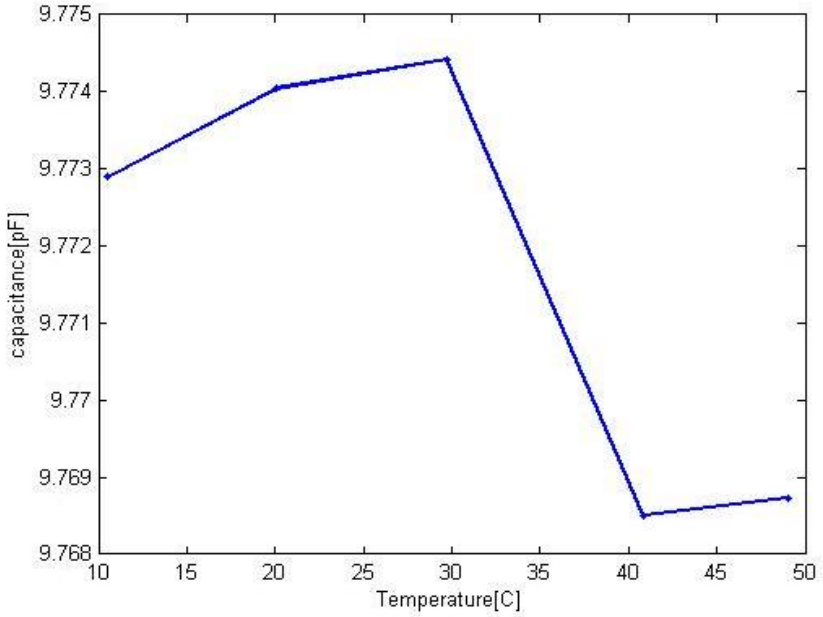


Figure 4-7 Thermal Stability of the capacitive sensor

Table 3 shows the temperature coefficient of the test board and capacitive sensor in a different temperature range.

Table 3 Temperature coefficient

Range	10~20℃	20~30℃	30~40℃	40~50℃
Test Board (with cap)	34.48 ppm/℃	-12.14 ppm/℃	-20.99 ppm/℃	38.18 ppm/℃
Cap Sensor	11.67 ppm/℃	4.09 ppm/℃	-60.36 ppm/℃	2.36 ppm/℃
Test Board (no cap)	22.81 ppm/℃	-16.23 ppm/℃	39.37 ppm/℃	35.82 ppm/℃

4.3.3 Power Consumption

The power consumption of the PCB is 0.2W and the power consumption of the analog part is less than 5mW (simulation result).

4.4 Conclusions

In this chapter, measurement results of the PCB are presented. First, fabricated chip, including circuit layout and chip micrograph, is presented. Next, the measurement setup is introduced in two parts: test board design and measurement equipment. After this, performances regarding to SNR, temperature stability and power consumption are presented. At last, the summarized measurement results and comparison to the expectations are demonstrated in Table 4.

Table 4 Performance summary and comparison

	Existing CDC	Expectations	Measurement Results
Power (analog part)	215mW	10mW	4.7mW
Power (PCB)	1.11W	0.5W	0.2W
Supply Voltage	±9V	3.3V	3.3V
Conversion Time	63.2us	50µs	50µs
Sensor Cap Range	1pF	10pF	10pF
Resolution	12 bits	15 bits	18.5 bits

References

[1] R. Nojdelov, R. Yang, X. Guo, S. Nihtianov. “Highly Stable Capacitance-to-Digital Converter with Improved Dynamic Range”, Sensing Technology (ICST), 2011 Fifth International Conference on, pp. 140-144, Nov. 2011.

Chapter 5

Conclusions

With the wide application of the capacitive sensor in the measurement of the relative position and the drift/vibration of the controlled objects, there is a requirement for an interface to obtain the capacitance of the sensor. As a kind of interface, CDC based on the multi-slope analog-to-digital conversion principle, has been optimized for low power consumption in this thesis.

5.1 General Conclusions

The following list summarizes the main findings of this thesis:

- Studies and analysis have been made in architecture-level, to investigate the design choice (Chapter 2). At first, a former work [1] with high accuracy and excellent thermal stability has been briefly discussed. Followed by the operating principles of the front-end circuit, the discharge operation and the comparator and counting circuit. To reach the requirements for the detection limits, the major error sources and digital filtering effect have been analyzed, including thermal noise, quantization noise, flicker noise and offset and comparator delay. Based on all these, three distinct measurement modes are discussed.

- The circuit-level analysis and design of the interface circuit have been introduced (Chapter 3). All specifications are discussed in Op-Amp design and a two-stage class AB Op-Amp employing folded-cascode is chosen due to these specifications. After this, a fast dynamic latch comparator with a two-stage pre-amplifier is presented. Because of its relatively stable on-resistance, complementary PMOS-NMOS switches are chosen in this work. In the end, simulation results are analyzed in two aspects: simulation results of Op-Amp (AC loop-gain, noise and settling time) and the simulation result of comparator.

- Measurement results of the PCB are presented (Chapter 4). After the layout design, a prototype chip has been fabricated in 0.35-µm CMOS technology. Measurement setup is introduced in two parts: test board design and measurement equipment. Performances regarding Signal to Noise Ratio (SNR), temperature stability and power consumption are tested. At first, the SNR for the PCB is tested with conversion time 50µs. Figure 4-5 shows the noise spectrum with conversion time 50µs. The achieved SNR is 90dB, which means it can reach 15 bits resolution. Temperature coefficient of the test board in a different temperature range is shown in Table 3. The power consumption of the test board is 0.2W, which is almost 6 times lower than the existing work (section 2.2).

5.2 Main Contributions

Compared with the existing work, the presented CDC has several advantages:

- By integrating all analog parts of the existing CDC [1], this work decreases the power consumption significantly.

- A high resolution, which is 18.5 bits, can be achieved with conversion time 50μs.

- This work has a relatively temperature stability.

5.3 Future work

There is always room for improvements and various things can be addressed in the future. The expected future work can be categorized into three aspects:

- Regarding the limited time, the measurements have not been done in the round. A long-term stability measurement is only one option. It is better to test the chip in many other ways to fully check its performance.

- It still needs to optimize the CDC to be insensitive to the parasitic capacitor. An active shielding technique can be used in the interface to compensate the effect of the parasitic capacitance of the PCB wire. The active shields are connected to a buffer voltage while using feed-forward [2].

- The temperature stability of this work needs to be improved. In my opinion, the reason caused the temperature drift is the charge injection of switches. The charge-injection can be partially compensated for by adding half-size dummy switches. The dummy switches are driven by a complementary clock signal and inject an amount of charge from the main switches [3].

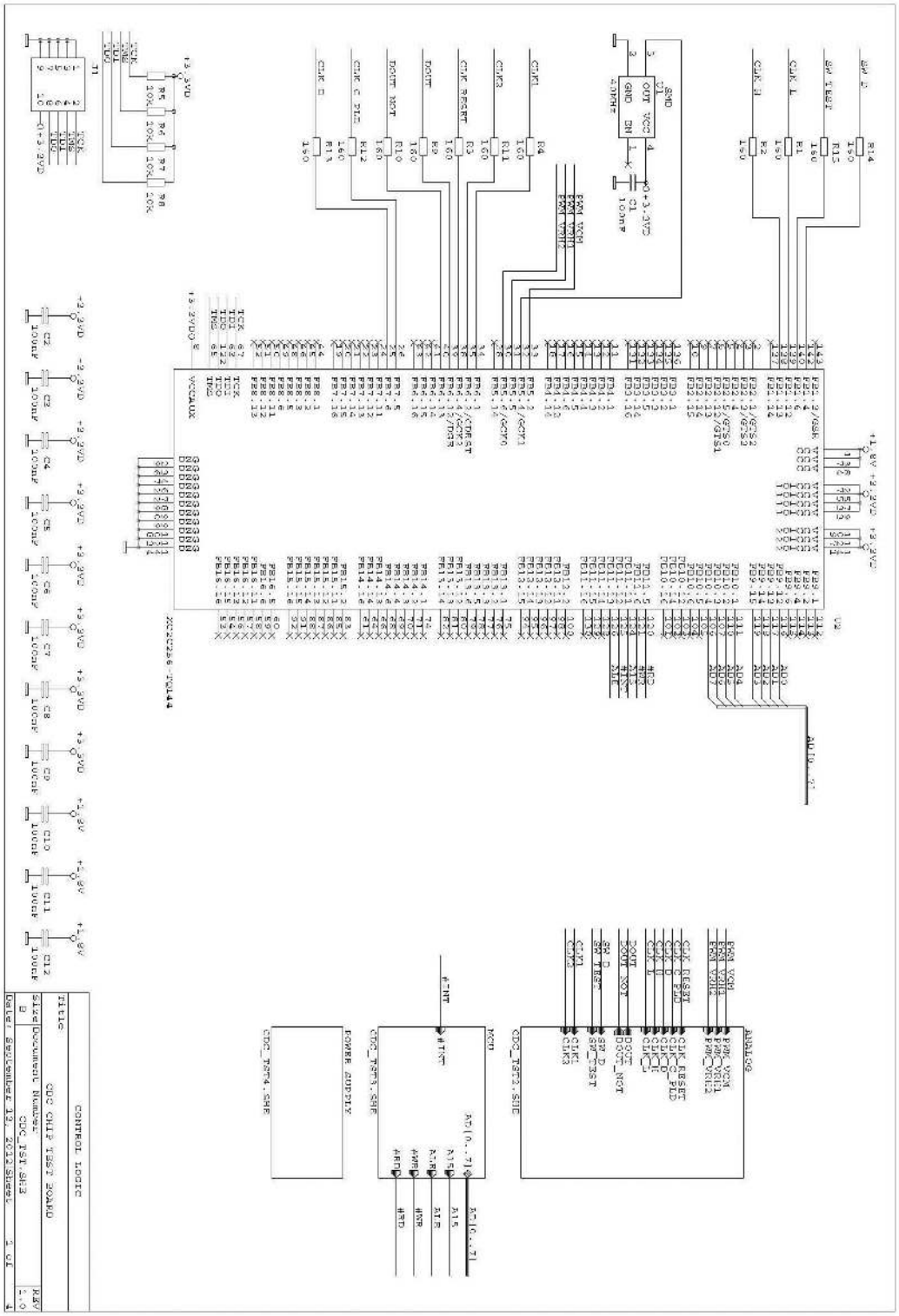
References

[1] R. Nojdelov, S. Nihtianov, “Capacitive-Sensor Interface With High Accuracy and Stability”, IEEE Transactions On Instrumentation And Measurement, Vol. 58, May 2009.

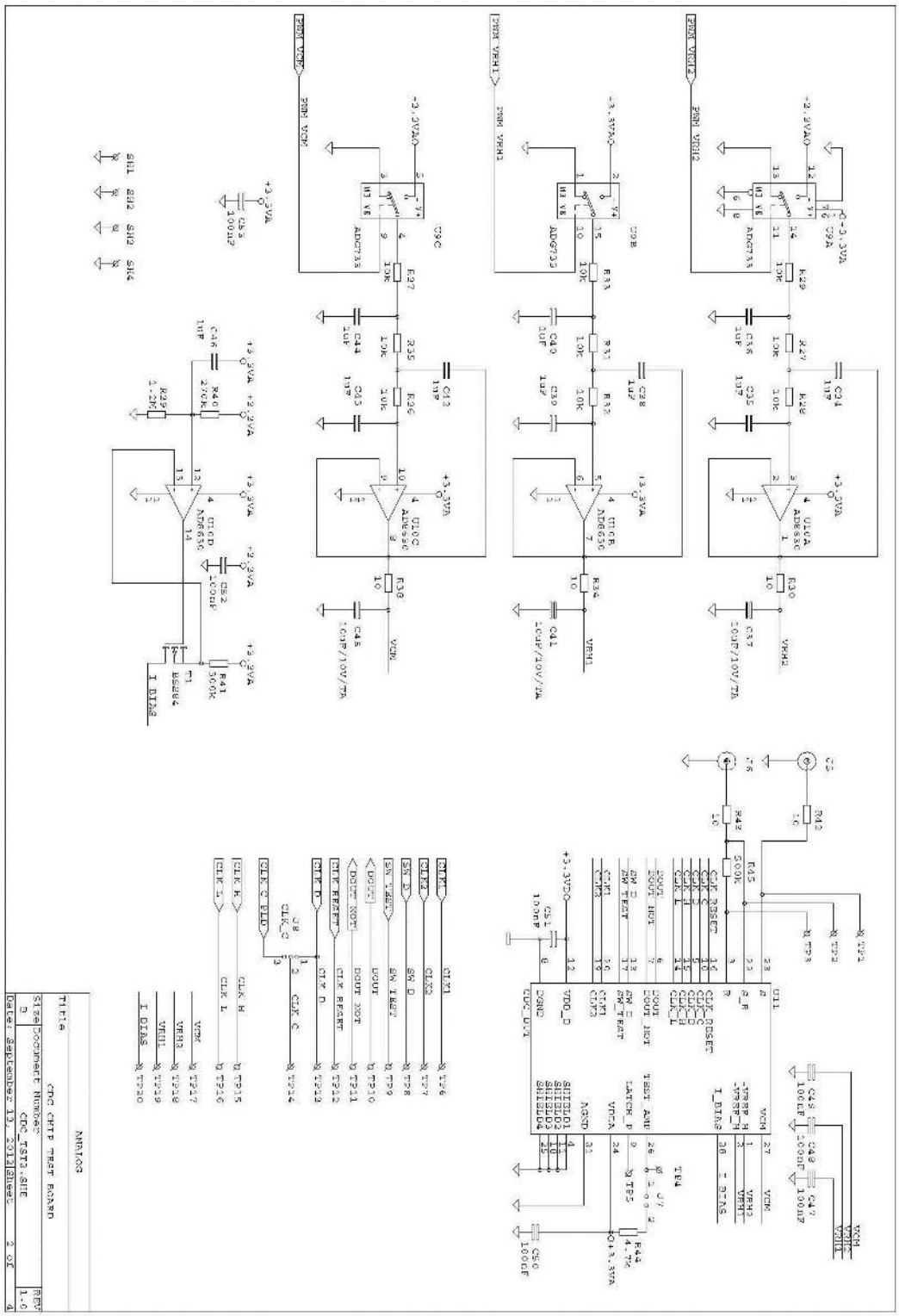
[2] Heidary, G. C. M. Meijer, “An integrated interface circuit with a capacitance-to-voltage converter as front-end for grounded capacitive sensors”, Measurement Science and Technology, Vol. 20, Nov. 2008

[3] G. Wegmann, E. A. Vittoz, F. Rahali, “Charge Injection in Analog MOS Switches”, IEEE Journal of Solid-State Circuits, Vol. 22, pp. 1091-1097, Dec,1987

Appendix A



Appendix A



Appendix A