Energy-Efficient Capacitive-Sensor Interfaces

Energy-Efficient Capacitive-Sensor Interfaces

Proefschrift

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus prof.dr.ir. K.C.A.M. Luyben,
voorzitter van het College voor Promoties,

in het openbaar te verdedigen
op dinsdag 11 juni 2013 om 12:30 uur

door

Zhichao TAN

Master of Engineering
Peking University, Beijing, China

geboren te Shaanxi, P. R. China

Dit proefschrift is goedgekeurd door de promotor:

Prof. dr. ir. G. C. M. Meijer

Copromotor:

Dr. ir. M. A. P. Pertijs

Samenstelling promotiecommissie:

Rector Magnificus,	voorzitter
Prof. dr. ir. G. C. M. Meijer,	Technische Universiteit Delft, promotor
Dr. ir. M. A. P. Pertijs,	Technische Universiteit Delft, copromotor
Prof. dr. K. A. A. Makinwa,	Technische Universiteit Delft
Prof. dr. W. M. C. Sansen,	Katholieke Universiteit Leuven
Prof. ir. A. J. M. van Tuijl,	Uinversiteit Twente
Prof. dr. ir. A. H. M. van Roermund,	Technische Universiteit Eindhoven
Dr. Y. Chae,	Yonsei University
Prof. dr. P. J. French,	Technische Universiteit Delft, reservelid

Printed by Ipskamp Drukkers B.V., Enschede

ISBN: 978-94-6186-165-8

Cover Design: Amber Jiawen

Printed in the Netherlands

To my beloved parents

致我亲爱的父母亲

Table of Contents

Chapter 1

Introduction

This thesis describes the theory, design and realization of energy-efficient capacitive-sensor interfaces that are dedicated to energy-constrained applications [1,2]. The goal of this work is to explore energy-efficient capacitive-sensor interface design techniques both at the system and the circuit level.

In this chapter, the motivation and objectives of this work are described, and an overview of the prior art is given. At the end of this chapter, the highlights and structure of the thesis are presented.

1.1 Motivation

Capacitive sensors are based on the modulation of electrical capacitance by a physical or chemical parameter of interest. This principle is widely used, for instance, in pressure sensors, liquid-level gauges, accelerometers and humidity sensors [1]. Merging a capacitive sensing element, an analog interface circuit, an analog-to-digital converter and a bus interface into one single chip results in a smart capacitive sensor [1]. This type of sensor is widely used in emerging sensing applications, such as battery-powered implant devices in medical care applications or wireless environmental monitoring applications [2]. In these types of applications, the energy consumption of the smart capacitive sensor has increasingly become a more limiting factor, because the systems usually only contain a low volume

battery or rely on energy harvesting, restricting the energy available for sensors.

A good example of a high-volume application that requires energy-efficient smart sensors is the monitoring of perishable food products, in which the use of RFID technology enables wireless measurement of key parameters such as temperature, humidity, and CO_2 concentration at various stages in the supply chain [2,3]. The information thus obtained enables a better prediction of shelf life and a significant reduction in the waste caused by spoilage [2,3]. Such a solution, however, is only economically viable if the tags can be produced in large volumes at very low cost. This calls for the use of both CMOS-compatible sensors that can be co-integrated with RFID circuitry, and low-cost printed batteries, or even no batteries at all (passive RFID). The availability of energy-efficient sensors is a key requirement for the realization of such an application.

A capacitive sensor usually includes a sensing element and an interface circuit which converts capacitance values into the digital domain. Thus, a modern capacitive-sensor interface usually refers to a capacitance-to-digital-converter (CDC), which is illustrated in Fig. 1. Since capacitive sensing elements do not consume static power, they are very suitable for use in low-power and energy-constrained applications. However, the energy consumption of this interface circuit typically dominates the overall energy consumption of the capacitive sensor. Hence, for such applications, an energy-efficient capacitive-sensor interface is an essential building block.

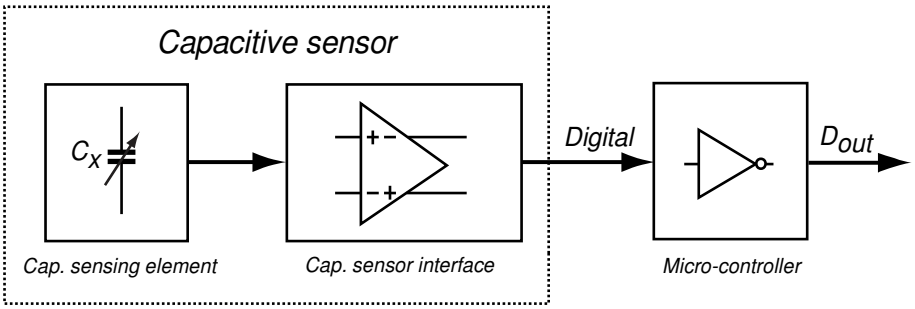


Figure 1.1: System diagram of a typical capacitive-sensor system.

This thesis will focus on interface circuits for capacitive sensor that are tailored for applications that require a high resolution (> 10bits). Several new techniques to improve the energy efficiency of capacitive-sensor interfaces will be introduced. Three prototypes based on both delta-sigma modulation and period modulation will be presented to demonstrate the effectiveness of these techniques. These prototypes achieve the highest energy efficiency reported to date for these types of interfaces.

1.2 Background and Challenges

When quantifying and comparing the energy efficiency of different capacitive-sensor interfaces, it is important to take into account that energy consumption can typically be traded for performance metrics such as resolution, accuracy and speed. Different applications may require different levels of performance, and hence a direct comparison of the energy consumed by capacitive-sensor interfaces designed for different applications makes no sense. To enable a quantitative comparison of different designs, one option is to normalize the energy consumption in relation to the performance using a so-called figure-of-merit (FoM), which takes the energy performance trade-offs into account.

In this work, a FoM is adopted that is similar to the Walden FoM often used for comparing the efficiency of general-purpose analog-to-digital converters (ADCs) [4]. This approach makes sense, since many capacitive-sensor interfaces are structurally very similar to ADCs. This FoM relates the energy consumption per measurement (E_{meas}) to the interface's effective number of bits (ENOB):

$$\mathrm{FoM} = \frac{E_{meas}}{2^{\mathrm{ENOB}}} \quad . \tag{1-1}$$

This FoM normalizes the energy consumption by dividing energy consumption by the effective number of conversion steps. The ENOB is defined as:

$$\mathrm{ENOB} = \frac{\mathrm{SNR}_{\mathrm{dB}} - 1.76}{6.02} \quad , \tag{1-2}$$

which expresses the signal-to-noise ratio (SNR) in terms of the SNR of an ideal ADC with a output length of the ENOB bits. The SNR, in units of dB, is defined in the following equation:

$$\mathrm{SNR}_{\mathrm{dB}} = 20\log_{10}\left(\frac{C_{range}}{C_{resoluion}}\right) \quad , \tag{1-3}$$

in which C_{range} is the input range of the capacitive-sensor interface and $C_{resolution}$ is capacitance resolution of the interface.

TABLE I. PRIOR ART OF ENERGY-EFFICIENT OR LOW-POWER CAPACITIVE-SENSOR INTERFACES.

	Type	Tech.	Supply voltage	Current cons.	Meas. time	Capacitance range	ENOB	FoM
[5]	SAR	0.18μm	1.4V	169μA	3.8μs	3pF	6.8bit	7.9pJ/step
[6]	PM	0.7μm	5V	1mA	1s	5.8pF	20bit	4.7nJ/step
[7]	PWM	0.32μm	3V	28μA	33μs	0.5pF~0.76pF	8bits	10pJ/step
[8]	ΔΣ	0.35μm	1.8V	460μA	0.025ms	n.a.	10bit	17pJ/step

Table I gives a survey of the prior art capacitive-sensor interfaces up to the year of 2008 when this thesis work started. The interfaces are based on four commonly used architectures: successive approximation register [5], period modulation [6], pulse-width modulation [7], and delta-sigma modulation [8]. These interfaces achieve at best a FoM of 10pJ/step. State-of-the-art voltage-input ADCs, in contrast, achieve a FoM well below 5fJ/step [9], with average designs reaching well below 1 pJ/step. This shows that capacitive-sensor interfaces, in spite of their similarity to ADCs, are at least one order of magnitude less energy efficient.

One practical reason for the efficiency gap between general-purpose ADCs and capacitive-sensor interfaces is that capacitive sensors are associated with a certain parasitic capacitance C_p which also needs to be charged and discharged during readout, even though the parasitic capacitor does not contribute any signal. Moreover, for many practical capacitive sensors, only a relatively small variation ΔC_x on a much larger baseline capacitance C_x carries information about the measurand, which also decreases the achievable signal-to-noise ratio [10]. An analysis of these effects will be presented in Chapter 2. However, even when taking these effects into account, a gap remains, indicating that there is room for improvement. In the rest of this thesis, system and circuit design techniques for improving the energy efficiency of the capacitive-sensor interface will be presented, and prototype designs will be presented to verify the effectiveness of the proposed approaches.

1.3 Organization of the Thesis

The remainder of this thesis has been divided into four chapters.

Chapter 2 gives an overview of energy-efficient capacitive-sensor interfaces. It begins by addressing capacitive sensing elements. This is followed by a discussion of the various architectures of capacitive-sensor interfaces. Then, system-level and circuit-level techniques for improving the energy efficiency of capacitive-sensor interface are presented in detail.

Chapter 3 presents energy-efficient capacitive-sensor interfaces based on period modulation. The operation principle of such interfaces is discussed in detail. A prototype is then presented in which the system-level techniques proposed in Chapter 2 are employed to improve energy efficiency by two orders of magnitude compared to prior interfaces based on period modulation.

Chapter 4 presents energy-efficient capacitive-sensor interfaces based on delta-sigma modulation. Two prototypes are described that are tailored for the readout of a capacitive humidity sensor. These prototypes demonstrate the use of both circuit- and system-level techniques. The second prototype

achieves a figure-of-merit of 1.4pJ/step, which is state-of-the-art among all delta-sigma based capacitive-sensor interfaces reported to date.

Chapter 5 concludes the thesis. The benchmark of the proposed designs in this thesis is presented. The original contributions and main findings of this thesis are also highlighted.

1.4 References

[1] L. K. Baxter, *Capacitive Sensors: Design and Applications*. New York: IEEE Press, 1997.

[2] G. C. M. Meijer, *Smart Sensor Systems*. Chichester, UK: Wiley, 2008.

[3] E. Abad, F. Palacio, M. Nuin, A. González de Zárate, A. Juarros, J.M. Gómez, S. Marco, "RFID smart tag for traceability and cold chain monitoring of foods: Demonstration in an intercontinental fresh fish logistic chain," Journal of Food Engineering, vol. 93, pp. 394-399, Aug. 2009.

[4] R. H. Walden, "Analog-to-digital converter survey and analysis," *IEEE Journal on Selected Areas in Communications*, vol. 17, pp. 539-550, Apr. 1999.

[5] K. Tanaka et al., "A 0.026mm^2 capacitance-to-digital converter for biotelemetry applications using a charge redistribution technique," in *Proc. IEEE Asian Solid-State Circuits Conference (A-SSCC)*, Nov. 2007, pp. 244-247.

[6] A. Heidary and G. C. M. Meijer, "Features and design constraints for an optimized SC front-end circuit for capacitive sensors with a wide dynamic range," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 7, pp. 1609-1616, July 2008.

[7] P. Bruschi, N. Nizza and M. Dei, "A low-power capacitance to pulse width converter for MEMS interfacing," in *Proc. European Solid-State Circuits Conference (ESSCIRC)*, Sept. 2008, pp. 446-449.

[8] S. A. Jawed et al., “A 828μW 1.8V 80dB dynamic range readout interface for a MEMS capacitive microphone,” in *Proc. European Solid-State Circuits Conference (ESSCIRC)*, Sept. 2008, pp. 442-445.

[9] M. van Elzakker, E. van Tuijl, P. Geraedts, D. Schinkel, E. Klumperlink, B. Nauta, “A 1.9μW 4.4fJ/conversion-step 10b 1MS/s charge-redistribution ADC,” in *International Solid-State Circuits Conference Dig. Tech. Papers*, pp. 244-245, 2008.

[10] M. A. P. Pertijs and Z. Tan, “Energy-efficient capacitive sensor interfaces,” in *Analog Circuit Design*, A. Baschirotto, A. H. M. van Roermund and M. Steyaert, Eds. New York: Springer, 2012, pp. 129-147.

Chapter 2

Energy-Efficient Capacitive-Sensor Interfaces: An Overview

2.1 Introduction

Capacitive sensors are widely used, for instance, in pressure sensors, liquid-level gauges, accelerometers and humidity sensors [1]. Since capacitive sensors do not consume static power, they are very suitable for use in low-power, energy-constrained applications [2]. In such applications, however, the energy consumption of the capacitive sensor will be dominated by that of the interface circuit, which converts capacitance values to the digital domain. Hence, for such applications, an energy-efficient capacitive-sensor interface is an essential building block. This chapter will provide an overview and detailed discussion of the interface circuit, which is dedicated to high-resolution and high-accuracy applications, along with the design-based period modulation (Chapter 3) and delta-sigma modulation (Chapter 4).

2.2 Capacitive Sensing Elements

2.2.1 Classification of Capacitive Sensing Elements

The simple capacitive sensor is a parallel-plate capacitor which comprises two metal plates with area A and distance d. When d is much smaller than the plate dimensions, its capacitance is given by following equation:

$$C = \varepsilon \frac{A}{d} \quad , \tag{2-1}$$

where ε is the dielectric constant of the material between the two electrodes. By modulating one of the three parameters in this equation by a measurand of interest, a capacitive sensor is obtained. Capacitive sensors can thus be classified based on the parameter that is modulated. For modulation of distance (d), the sensor has fixed values for A and ε, and the measurand modifies the distance. This type of sensor finds application in displacement sensors, pressure sensors, touch screens, etc. [1]. For modulation of area (A), the sensor has fixed values for ε and d, and the measurand modifies the area. This type of sensor finds application in angular detectors [2]. Lastly, for modulation of the dielectric constant (ε), the sensor has fixed values for d and A, and the measurand modifies the dielectric constant. This type of sensor finds application in humidity sensors, gas sensors, DNA sensors, etc. [2].

2.2.2 Modeling of Capacitive Sensor Elements

The characteristics of capacitive sensing elements can be quite different from one application to another. To better understand the sensing element, an electrical model is needed. Figure 2.1 shows an example of such a model [3]. Besides the sensing element itself, it also includes a parasitic shunt resistor R_x and two parasitic capacitors C_{p1} and C_{p2} at the two terminals of the sensing element. The parasitic capacitors are particularly important for the energy efficiency of a capacitive-sensor system, as they tend to increase the energy consumption. Minimizing them, e.g. by co-integrating the sensor

and interface circuit on a single chip or in a single package, can be an important way to improve energy efficiency.

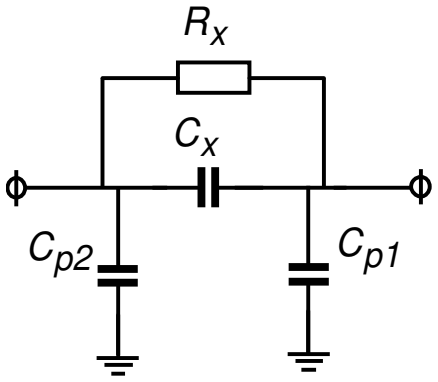


Figure 2.1: Electrical model of the capacitive sensing element.

The model should also describe how the measurand modulates C_x. Often, only a small fraction of C_x varies. To model this, we define the mean, or baseline, capacitance C_0 and the modulation index α as [3]:

$$C_0 = \frac{C_{x,\min} + C_{x,\max}}{2} \tag{2-2}$$

$$\alpha = \frac{C_{x,\max} - C_{x,\min}}{C_0} \quad , \tag{2-3}$$

where $C_{x,max}$ and $C_{x,min}$ are the maximum and minimum capacitance for the range of measurand values of interest. In most applications, α, which expresses the capacitance variation relative to the baseline value, is only around 0.1. For a given energy per measurement, a lower value of α tends to lead to a lower signal-to-noise ratio (SNR). Conversely, to obtain a given SNR, more energy is needed for lower values of α. Hence, this is another important parameter that should be optimized for energy efficiency.

2.3 Capacitive-Sensor Interfacing Approaches

The measuring of capacitors involves either measuring the charge displacement associated with a change in the voltage across the capacitor, or measuring voltage resulting from a given amount of charge on the capacitor. The electrical voltage or current signal which charges or discharges the capacitor can be any type of waveform. In most measurement applications the excitation signals have a sinusoidal or a square-wave shape [4].

Capacitive-sensor interfaces employing sinusoidal excitation need to generate a sinusoidal driving voltage or current, which complicates the interface circuit design significantly. Thus achieving the requirements of sine-wave excitation can be rather costly, and the extra sinusoidal-generated blocks make the whole system power hungry [4]. On the other hand, square-wave excitation is usually implemented with switches which can be readily implemented in CMOS technology. Moreover, with fewer driving building blocks, the complexity and power consumption of switched-capacitor (SC) circuits can be lower than the interfacing approach based on sinusoidal input. Therefore, this thesis will only focus on the switched-capacitor technique, which is essentially a square-wave excitation approach.

For various types of interfaces, Fig. 2.2 shows a survey of how much energy is used per measurement versus the effective number of bits (ENOB) [5]. This survey includes interfaces based on successive approximation register (SAR), delta-sigma modulation (DS), pulse-width modulation (PWM) and period-modulation (PM). Since many of the capacitive-sensor interfaces included in the survey are structurally very similar to voltage-input ADCs, it is instructive to compare their energy efficiencies. The dotted line is the figure-of-merit (FoM) of 1pJ/step. State-of-the-art voltage-input ADCs achieve FoMs as low as 10fJ/step, with average designs reaching below 1pJ/step. In contrast, most of the capacitive-sensor interfaces included fail to achieve 1pJ/step. This shows that capacitive-sensor interfaces, in spite of their similarity to ADCs, are at least one order of magnitude less energy efficient. Figure 2.2 also clearly shows that the different types of interfaces cover a resolution range from 6 bits to 20 bits. The SAR- and PWM-based designs cover the low end of the resolution range. The delta-sigma-based

designs show high flexibility with the resolution ranging from 6 bits to 16 bits. The period-modulation based designs, on the other hand, can achieve high resolution from 15 bits to 20 bits. Since the focus of this thesis is mainly on high-resolution, high-accuracy applications, the design-based period modulation (Chapter 3) and delta-sigma modulation (Chapter 4) will be discussed in great detail in this thesis.

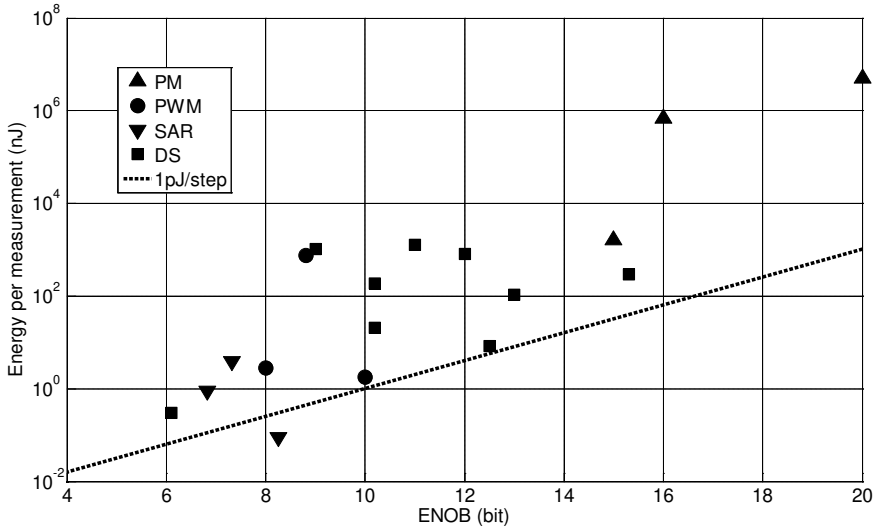


Figure 2.2: Survey of the energy consumption per measurement for various capacitive-sensor interfaces according to [5].

2.3.1 Capacitive-Sensor Interfaces Using Period Modulation

Interfaces using period modulation are essentially relaxation oscillators that convert the sensor's capacitance into a period of time which can easily be digitized using a digital counter, e.g. with a microcontroller [2]. An attractive feature of these interfaces is that they are operated asynchronously and thus do not require a clock signal. This can be an important advantage in applications where the interface is located close to the sensor and is connected using a limited number of wires to a remote microcontroller. Figure 2.3 shows a block diagram of an interface circuit based on period modulation. The sensing capacitor C_x is inserted into a relaxation oscillator.

The changing capacitance changes the length of the oscillator period, which is a measure of C_x and can be captured by a time-to-digital converter.

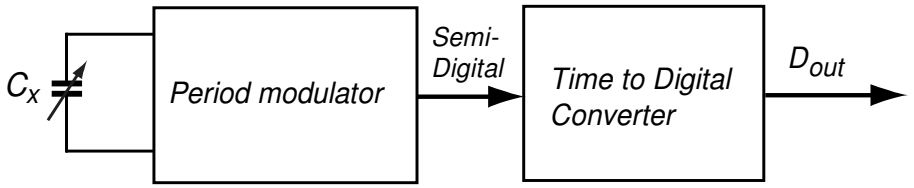


Figure 2.3: Interface using time period modulation.

In this type of converter, the period can be digitized by counting its duration in terms of the clock cycles of a faster reference clock. For an *N*-bit resolution requirement, the counter frequency should obey the following equation [4, 6]:

$$f_{clk} \geq 2^N \times f_{out} \quad , \tag{2-4}$$

where f_{out} is the output frequency of the period modulator which is inverse to the time interval, and f_{clk} is the required clock frequency.

> *Example 2.1:* If the period time is 100μs and 13-bit resolution is required, then the reference clock frequency should be higher than 80MHz [4].

In Chapter 3, it will be shown that interfaces using period modulation can be very flexible and energy efficient.

2.3.2 Capacitive-Sensor Interfaces Using Delta-Sigma Modulation

Figure 2.4 shows a block diagram of an interface using delta-sigma modulation. A delta-sigma modulator transfers the sensor capacitance into a bit-stream which is a pure digital signal. The information of interest is modulated into the bit-stream density of the bit-stream, which is demodulated by the decimation filter. Chapter 4 will present capacitive-sensor interfaces using delta-sigma modulation. It will be shown that such

interfaces can achieve high resolution which ranges from 12 bits to 21 bits while achieving a high energy efficiency which can be as low as 1pJ/step. This explains why these interfaces are rather popular nowadays [5].

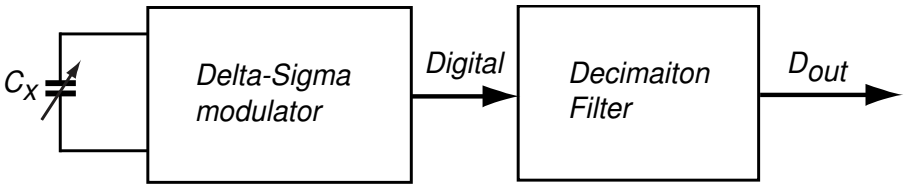


Figure 2.4: Interface using delta-sigma modulation.

2.4 Energy-Efficient System-Level Techniques

In this section, the system-level techniques for improving the energy efficiency of capacitive-sensor interface will be discussed. It will be shown in the rest of the thesis (Chapters 3 and 4) that designs using these techniques can achieve state-of-the-art energy efficiency within their respective categories.

2.4.1 Charge Balancing

Charge balancing is a technique to integrate the charge of an unknown sensing capacitor together with that of a reference capacitor, so that both charges are in balance with each other. After the subtraction of both charges and integration of the residue, the final averaged charge becomes zero. Figure 2.5 shows the core part of an interface using a delta-sigma modulator with a single-bit quantizer. The sensor capacitance C_x is embedded as the sampling capacitor of the loop filter. In every clock cycle, a charge proportional to C_x is integrated in addition to a charge proportional to C_{ref}, the polarity of which depends on the bit-stream output *bs*. The negative feedback in the modulator ensures that the former charge is balanced by the latter, resulting in a zero average charge flowing into the loop filter. When the ratio of the number of HIGH bits and the total number of bits (which is the HIGH + LOW bits) amounts to μ ($0 \leq \mu \leq 1$), then the bit-density of the bit-stream becomes:

$$NC_x - \mu NC_{ref} + (1-\mu)NC_{ref} = 0 \quad . \tag{2-5}$$

Solving μ gives:

$$\mu = \frac{C_x}{2C_{ref}} + \frac{1}{2} \quad , \tag{2-6}$$

which is the desired ratiometric function of C_x. As C_{ref} is assumed to be constant, C_x can be precisely expressed by the bit-stream density μ, which is accurately generated in the delta-sigma modulator.

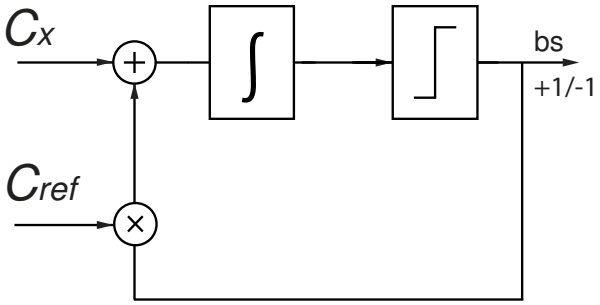


Figure 2.5: Charge balancing of first-order delta-sigma modulator.

2.4.2 Auto-Calibration

Auto-calibration can be used to reduce the effects of systematic errors and low-frequency noise [4]. Figure 2.6 shows an auto-calibration concept that in principle can be applied to any capacitive-sensor interface [7]. At the input of the interface, a multiplexer is added which selects one of three capacitors: a sensor capacitor C_x, a reference capacitor C_{ref}, or an offset capacitor C_{off}. When no explicit offset capacitor C_{off} is used, the associated terminals of the multiplexer are left floating. In this case, when C_{off} is selected, the input capacitance amounts to the sum of the parasitic capacitances and the offset of the capacitive-sensor interface. The capacitive-sensor interface is assumed to provide a digital output D_{out} which is a linear function of the capacitor C_i applied to its input:

$$D_{out} = aC_i + b \ . \tag{2-7}$$

Often the coefficients a and b are poorly defined, e.g. subject to device-to-device variation, long-term drift, power-supply variations, etc. If the multiplexer is employed, so that successively (C_x+ C_{off}), (C_{ref} + C_{off}) and C_{off} are digitized, in the final result M, the uncertainty due to a and b can be eliminated by means of the following digital post-processing:

$$M = \frac{D_{out,Cx+Coff} - D_{out,Coff}}{D_{out,Cref+Coff} - D_{out,Coff}} = \frac{C_x}{C_{ref}} \quad . \tag{2-8}$$

Herewith, it is assumed that the coefficients a and b, although being poorly defined, do not change during the time needed for the three successive conversions. Thus, C_x is measured ratiometrically with respect to C_{ref} and differentially with respect to the offset C_{off}, and a measurement result M is obtained which is independent of a, b and C_{off}.

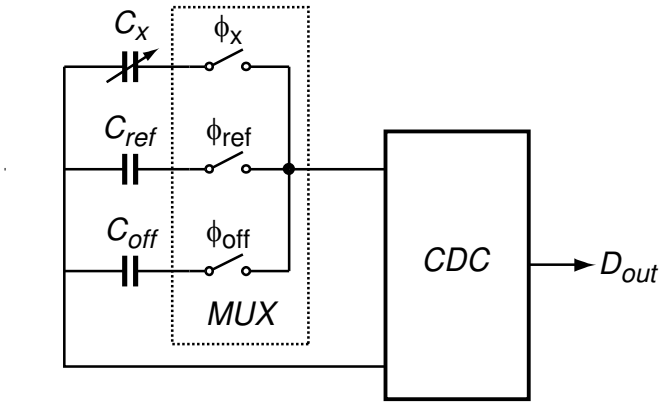


Figure 2.6: Capacitive-sensor interface with auto-calibration.

This auto-calibration approach comes at the cost of the extra energy consumed by the conversions of C_{off} and C_{ref}. In return, it strongly relaxes the offset- and gain-accuracy requirements of the capacitive-sensor interface. In some cases this can be translated into a significant reduction in energy consumption. In interfaces based on period modulation, for instance, the

propagation delay of the comparator introduces a poorly defined offset error. Without auto-calibration, the error needs to be reduced to a level that fulfills the overall accuracy requirements of the interface. By means of auto-calibration, the error is canceled, so that a slow, but energy-efficient comparator can be used [7].

2.4.3 Baseline Compensation and Zooming

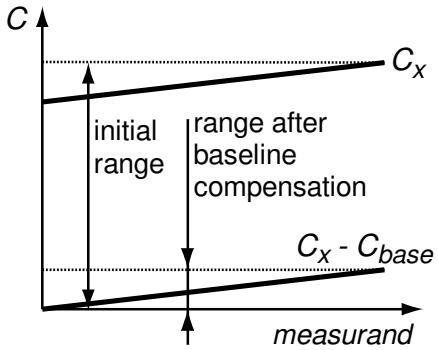
As addressed in Eqs. (2-2) and (2-3), the response of sensing capacitors to the measurand is often small compared to their baseline value. Directly using an interface-read capacitive sensor will lead to a waste of the dynamic range of the interface, which also has an unnecessarily high oversampling ratio and measurement time. In capacitive-sensor interfaces, employing methods to reduce the oversampling ratio can help to improve energy efficiency. For capacitive-sensor interfaces based on delta-sigma modulation, for example, this can be done by using higher-order loop filters, multi-bit feedback or cascaded architectures [8].

In this section we discuss an alternative approach that is based on preventing baseline or offset capacitance from consuming part of the input-capacitance range of capacitive-sensor interfaces. The same resolution of the sensor system can be maintained while reducing the range of the interface, which leads to a reduction in the required degree of oversampling, and hence, at least in principle, a reduced energy consumption. This concept is illustrated in Fig. 2.7(a).

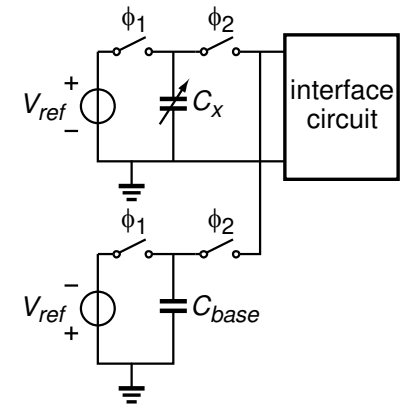
A straightforward implementation of this approach is shown in Fig. 2.7(b): a compensation capacitor C_{base} is driven with a voltage of opposite polarity as that of the sensor capacitor, so that the effective charge delivered to the interface is proportional to $(C_x - C_{base})$. This approach can be applied both to interfaces based on charge balancing, e.g. delta-sigma capacitive-sensor interfaces [9,10,11] as well as to interfaces based on charge redistribution, e.g. SAR capacitive-sensor interfaces [12]. While this approach relaxes the resolution requirements of the capacitive-sensor interface, it does increase thermal noise because the noise charge sampled on C_{base} adds to that sampled on C_x. Moreover, charging and discharging C_{base} consumes extra

energy. In this sense, C_{base} plays a similar role to that of the parasitic capacitance C_p. Nevertheless, it still makes sense to add this capacitor, as long as these drawbacks do not overshadow the energy reduction associated with the lower oversampling ratio.

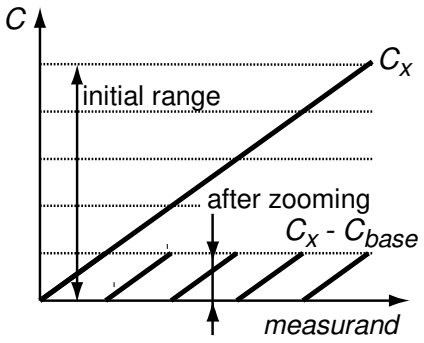
If the baseline value is an invariable part of the sensor capacitance, a fixed compensation capacitor can be used, or a capacitor that is adjusted once after fabrication [9]. The baseline-compensation concept can also be extended by adjusting the compensation capacitor dynamically to track variations in the sensor capacitance [10,11]. This leads to a two-step conversion process that is sometimes referred to as zooming (Fig. 2.7(c)) [11]. In the first step, C_{base} is adjusted to approximate C_x. In the second step, $(C_x - C_{base})$ is digitized. Depending on how fast C_x changes, it may not be necessary to repeat the first step for every measurement. Typically, a successive approximation algorithm is used in the first step, while the second step may consist of a SAR conversion or a conversion based on delta-sigma modulation. The resolution requirement of the second step is relaxed by the number of sub-ranges that can be distinguished in the first step.



(a)



(b)



(c)

Figure 2.7: Compensation for baseline capacitance: (a) principle; (b) implementation using a baseline-compensation capacitor; (c) extension to zooming.

In the capacitive-sensor interface based on zooming, the limited linearity of the adjustable compensation capacitor may cause discontinuities in the digital output as the sensor capacitance moves from one sub-range to the next. This problem can be addressed by introducing some overlap between the sub-ranges so that C_x can be measured in two adjacent sub-ranges when it moves from one sub-range to the next, allowing the discontinuity to be digitally corrected. An alternative is to employ an auto-calibration approach in which the capacitive-sensor interface itself is used to accurately measure

C_{base} [11]. While such an auto-calibration step may be relatively energy-hungry due to the high resolution required, it need not be performed for every measurement, and thus need not dominate the system's energy consumption.

2.4.4 System-Level Chopping Technique

Most capacitive-sensor signals are low-frequency signals. Many interfering signals such as offset, 1/*f* noise, and mains-supply interferences are also located at low frequencies and may therefore corrupt the sensor signal [4]. The chopping technique can separate the sensor signal from the undesired signals mentioned above. The sensor signal is modulated to a higher frequency so that it can be processed without being affected by 1/*f* noise, offset and supply interference. After processing, the wanted signal can be demodulated back to the baseband.

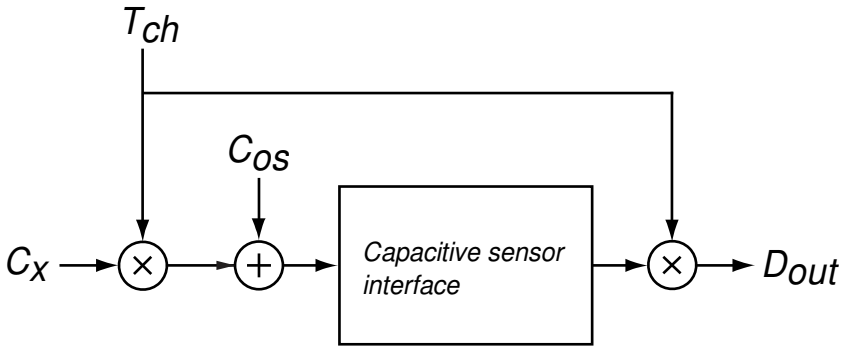


Figure 2.8: System chopping technique.

Figure 2.8 shows how the chopping technique can be applied to a capacitive-sensor interface at the system level. At both the input and output of the interface processing chain, chopper switches have been added which reverse the signal polarity. From this, we can obtain two outputs. Averaging these two outputs will eliminate the effect of C_{os}.

2.5 Circuit-Level Considerations

The capacitive-sensor interfaces proposed in this thesis are all implemented using switch-capacitor (SC) circuits, since this naturally allows the sensing capacitor to be used as the sampling capacitor of the front-end. The power consumption of a SC implementation is usually dominated by the OTAs used to establish the charge transfer. Therefore, the design of an energy-efficient OTA implementation provides the key for improving the overall energy efficiency of a SC-based interface. In this section, we will discuss some low-power circuit-design techniques which can improve the energy efficiency of capacitive-sensor interfaces.

2.5.1 Analysis of Current Consumption

Figure 2.9 shows the circuit model of an integrator that is controlled by a two-phase non-overlapping clock. The input capacitor C_{in} can represent the sensing capacitor C_x. During phase φ_1, C_{in} is charged to a reference voltage V_{ref} and during phase φ_2, the resulting charge is transferred to the integration capacitor C_{int}. This transfer will be typically associated with exponential settling behavior. Figure 2.10(a) shows the circuit model of the settling phase and Fig. 2.10(b) shows a typical waveform at the integrator's output. To ensure accurate settling, the clock period φ_2 has to be long enough compared to the time constant of the charge-transfer process.

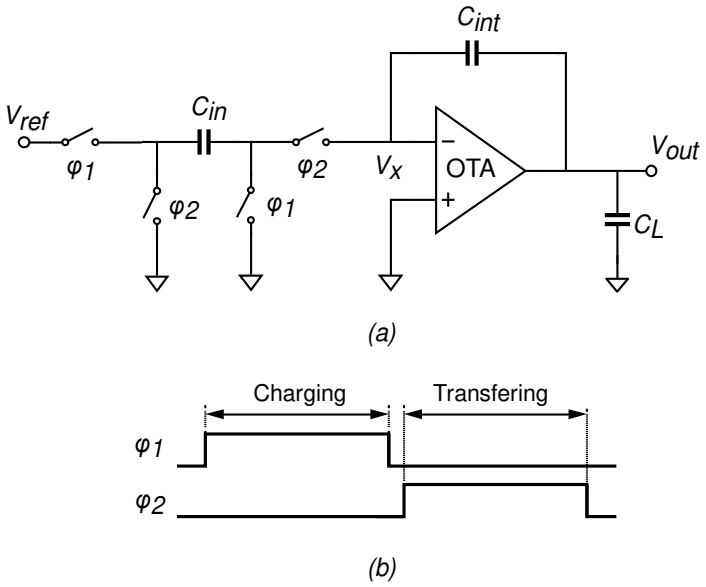


Figure 2.9: Circuit model of the first integrator in the delta-sigma modulator.

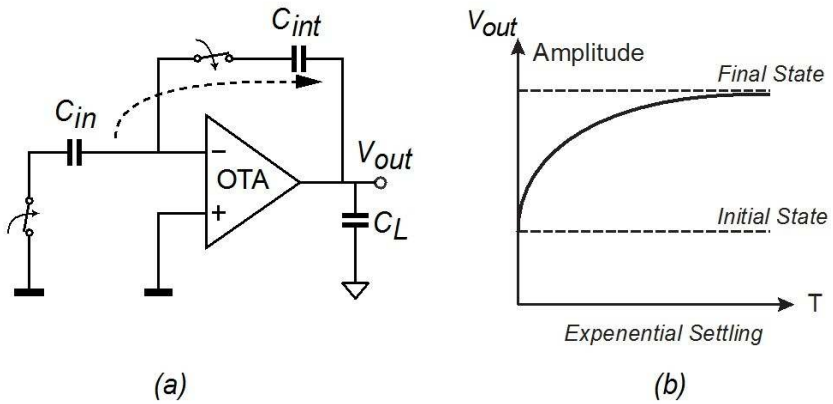


Figure 2.10: Circuit model of the integrator in the settling phase.

If the circuit is a one-pole system, then its transfer function can be described as:

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{G_o}{1 + s\tau} \quad , \tag{2-9}$$

where the G_o equals

$$G_o = \frac{1}{\beta + 1/A_o} \approx \frac{1}{\beta} = 1 + \frac{C_{in}}{C_{\text{int}}} \quad , \tag{2-10}$$

in which A_o is the DC gain of the OTA in the integrator. The time constant τ is defined by following equation:

$$\tau = \frac{C_o}{\beta g_m} \quad , \tag{2-11}$$

where g_m is the transconductance of the OTA. The capacitance C_o depends on the implementation of the OTA. For a single-stage OTA, C_o is

$$C_o = \frac{C_{\text{int}} C_{in}}{C_{\text{int}} + C_{in}} + C_L \quad , \tag{2-12}$$

where C_L is load capacitor. To achieve enough accuracy, the settling time has to satisfy the condition:

$$\frac{T_{clk}}{2} \geq (m+1)\tau \ln 2 \quad , \tag{2-13}$$

where m is the target accuracy of the system in bits. Substitution of (2-11) and (2-12) in (2.13) yields:

$$g_m \geq 2 \ln 2 \frac{(m+1)}{T_{clk}} (C_{in} + C_L + \frac{C_{in} C_L}{C_{\text{int}}}) \quad . \tag{2-14}$$

This condition reveals the minimum transconductance of the OTA used in the integrator for a clock period under certain loading conditions and resolution requirements.

For many OTA implementations, the transconductance directly dictates the supply current and hence the energy consumption. We define the current-efficiency factor γ of an OTA implementation as follows:

$$\gamma = \frac{g_m}{I_{tot}} \quad , \tag{2-15}$$

where I_{tot} is the total current consumption of the OTA, which directly links with the transconductance requirement. An energy-efficient design starts with minimizing the g_m requirement for the given specifications based on Eq. (2-14) and then finding the OTA structure that has the highest current-efficiency factor γ. The latter will be addressed in the following section.

2.5.2 Conventional OTA Topologies

This section reviews several OTA topologies and their current-efficiency factor γ (Eq. (2-15)).

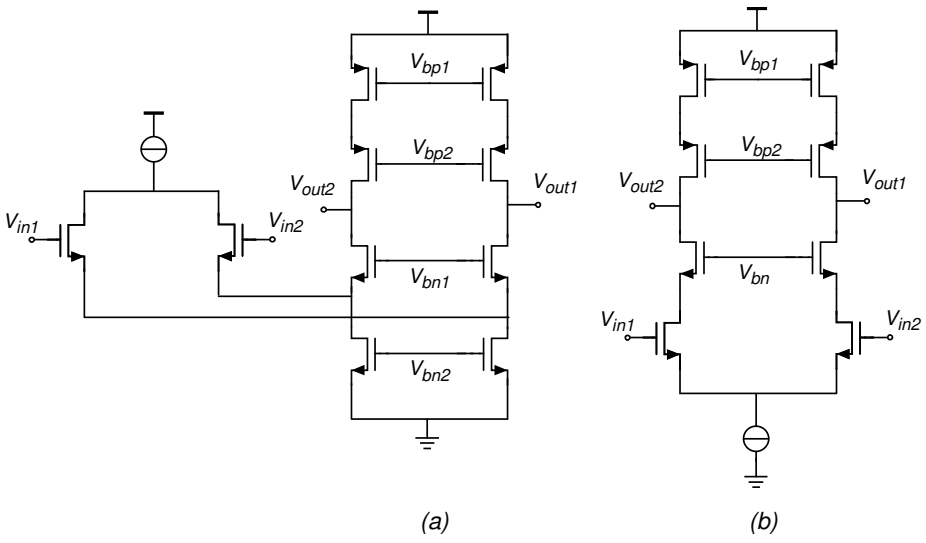


Figure 2.11: Two commonly used OTA structures: (a) folded-cascode OTA; (b) telescopic OTA.

The first topology reviewed is the frequently used folded-cascode OTA, which is shown in Fig. 2.11(a). It provides a reasonable output swing and high DC gain, which make this structure quite popular. Assuming that the input transistors as well as the cascode transistors are biased at a current I_d, the total current consumption is $4I_d$. If the associated transconductance equals g_{m0}, the current-efficiency factor γ_{FC} of this OTA is:

$$\gamma_{FC} = \frac{g_{m0}}{4I_d} \quad . \tag{2-16}$$

The second topology is the telescopic OTA, which is shown in Fig. 2.11(b). With only two currents legs, the total current consumption decreases to $2I_d$. As compared to the OTA of Fig 2.11(a), this boosts the current-efficiency factor by a factor of two so that:

$$\gamma_{TE} = \frac{g_{m0}}{2I_d} \quad . \tag{2-17}$$

This improved current efficiency comes at the price of a lower output swing, which is due to the headroom requirement of the tail current at the bottom [13].

2.5.3 Inverter-Based OTA

An inverter-based SC circuit outperforms the designs based on conventional OTAs in terms of current efficiency since both the PMOS and NMOS transistor of an inverter contribute transconductance while sharing the same supply current [14,15,16]. Figure 2.12 shows a differential version of an inverter-based OTA. If we assume that the PMOS and the NMOS have the same transconductance g_{m0}, the current-efficiency factor γ of Fig. 2.12 is:

$$\gamma_{INV} = \frac{2g_{m0}}{2I_d} = \frac{g_{m0}}{I_d} \quad . \tag{2-18}$$

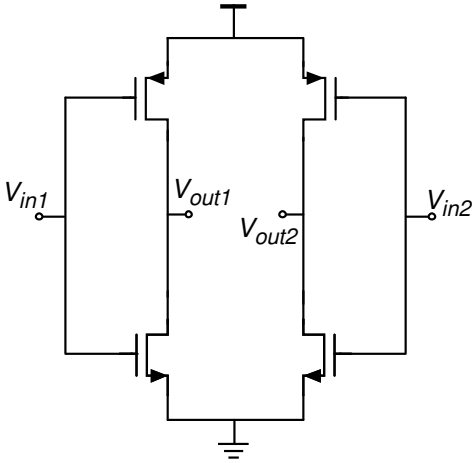


Figure 2.12: Inverter used as an OTA.

As a result, the intrinsic current efficiency of an inverter-based OTA is two times higher than that of a telescopic OTA and four times higher than that of a folded-cascode OTA. The inverter-based capacitive-sensor interface will be presented in Chapter 4.

2.6 Conclusions

An overview of energy-efficient capacitive-sensor interfaces has been presented in this chapter. In the case of a simple parallel-plate capacitor, a capacitive sensing element can be realized by making the capacitor's area (A), distance (d) or dielectric constant (ε) dependent on a physical or chemical parameter of interest.

This chapter has presented the system-level techniques that can be applied to design energy-efficient capacitive-sensor interfaces. Auto-calibration can be used to reduce the effects of systematic errors and low-frequency noise. Although this technique comes at the cost of an increase in energy consumed by the conversions of C_{off} and C_{ref}, in return, it strongly relaxes the offset- and gain-accuracy requirements of the capacitive-sensor interface. In some cases this can be translated into a significant reduction in energy consumption [7]. The baseline-compensation technique can cancel the effect

of unchanged baseline capacitance in order to use the dynamic range of the interface more efficiently, which in some cases may also save energy. The system-level chopping technique can separate the sensor signal from undesired interfering signals by modulating the sensor signal to a higher frequency, so that it can be processed to eliminate the 1/*f* noise, offset and supply interference.

Several low-power circuit-design techniques for capacitive-sensor interfaces have also been presented in this chapter. Since many capacitive-sensor interfaces are based on a switch-capacitor implementation, the OTA is used to transfer charge from the sensor capacitor to an integration capacitor for further processing. An analysis of the energy consumption of such circuit has been presented and a settling behavior analysis of switch-capacitor circuits revealed the minimum current consumption of the OTA used in the integrator for a clock period under certain loading conditions and resolution requirements. Several OTA structures have been reviewed along with their energy efficiency. It has been concluded that structures with fewer current legs have better energy efficiency. Finally, inverter-based SC circuits have been presented. The inverter-based OTA outperforms designs based on conventional OTAs since both the PMOS and NMOS transistor of an inverter contribute transconductance while sharing the same supply current.

The next chapter will discuss energy-efficient capacitive-sensor interfaces using period modulation.

2.7 References

[1] L. K. Baxter, *Capacitive Sensors: Design and Applications*. New York: IEEE Press, 1997.

[2] G. C. M. Meijer, *Smart Sensor Systems*. Chichester, UK: Wiley, 2008.

[3] W. Bracke, R. Puers and C. Van Hoof, *Ultra Low Power Capacitive Sensor Interfaces*. Dordrecht, the Netherlands: Springer, 2007.

[4] A. Heidary, “A low-cost universal integrated interface for capacitive sensors,” Ph.D. dissertation, Delft University of Technology, Delft, the Netherlands, 2011.

[5] M. A. P. Pertijs and Z. Tan, “Energy-efficient capacitive sensor interfaces,” in *Analog Circuit Design*, A. Baschirotto, A. H. M. van Roermund and M. Steyaert, Eds. New York: Springer, 2012, pp. 129-147.

[6] G. C. M. Meijer, “Interface electronics and measurement techniques for smart sensor systems,” in *Smart Sensor Systems*, G. C. M. Meijer, Ed. Chichester, UK: Wiley, 2008, pp. 23-54.

[7] Z. Tan, S. Heidary, G. C. M. Meijer and M. A. P. Pertijs “An energy-efficient 15-bit capacitive-sensor interface based on period modulation,” *IEEE Journal of Solid-State Circuits*, pp. 1703-1711, July 2012.

[8] S. R. Norsworthy, R. Schreier and G. C. Temes, Eds., *Delta-Sigma Data Converters: Theory, Design and Simulation*. Piscataway, NJ: IEEE Press, 1997.

[9] Z. Tan, R. Daamen, A. Humbert, K. Souri, Y. Chae, Y. V. Ponomarev and M. A. P. Pertijs, “A 1.8V 11μW CMOS smart humidity sensor for RFID sensing applications,” in *Proc. A-SSCC*, 2011, pp. 105-108.

[10] D.-Y. Shin, H. Lee and S. Kim, “A delta-sigma interface circuit for capacitive sensors with an automatically calibrated zero point,” *IEEE Trans. Circuits and Systems II*, vol. 58, no. 2, pp. 90-94, Feb. 2011.

[11] S. Xia, K. A. A. Makinwa and S. Nihtianov, “A capacitance-to-digital converter for displacement sensing with 17b resolution and 20μs conversion time,” in *ISSCC Dig. Tech. Papers*, 2012, pp.197-198.

[12] K. Tanaka et al., “A 0.026mm^2 capacitance-to-digital converter for biotelemetry applications using a charge redistribution technique,” in *Proc. A-SSCC*, Nov. 2007, pp. 244-247.

[13] W. M. C. Sansen, Analog design essentials. The Netherlands: Springer, 2008.

[14] B. Nauta, “A CMOS transconductance-C filter technique for very high frequencies,” *IEEE Journal of Solid-State Circuits*, vol. 27, no. 2, pp. 142-153, Feb. 1992.

[15] J. H. Huijsing, K. De Langen, R. Hogervorst and R. G. H. Eschauzier, “Low-voltage low-power opamp based amplifiers,” *Journal of Analog Integrated Circuits and Signal Processing*, vol. 8, no. 1, pp. 49-67, July 1995.

[16] Y. Chae and G. Han, “Low voltage, low power, inverter-based switched-capacitor delta-sigma modulator,” *IEEE Journal of Solid-State Circuits*, vol. 44, no. 2, pp. 458-472, Feb. 2009.

Chapter 3

Energy-Efficient Capacitive-Sensor Interface using Period Modulation

This chapter discusses the system design and circuit implantation of the energy-efficient capacitive-sensor interface using period modulation. After the operating principle is discussed, the system-level techniques for the energy-efficient design are addressed in detail. The system stability requirement and the design trade-offs are also analyzed, followed by the circuit implementation and measurement results.

3.1 Introduction

Interfaces based on period-modulation are essentially relaxation oscillators that convert the sensor's capacitance into a period time, which can then be easily digitized using a digital counter, e.g. in a microcontroller [1,2,3]. An attractive feature of these interfaces is that they are operated asynchronously and thus do not require a clock signal. This can offer an important advantage in applications where the interface is located close to the sensor and is

connected using a limited number of wires to a remote microcontroller. Moreover, period-modulation-based capacitive-sensor interfaces can be quite flexible, in that resolution can be easily traded for measurement time by measuring the duration of multiple output periods using a simple digital divider [4,5]. Furthermore, they can be designed to handle a very large input capacitance range with high resolution [6,7]. However, compared with alternative approaches based on delta-sigma modulation [8-14] or capacitance-to-pulse-duration conversion [15,16], prior period-modulation-based interfaces [5,7] are much less energy-efficient. With supply currents in the mA range, these interfaces are not suitable for use in energy-constrained applications, such as wireless-sensor networks or autonomous sensor systems.

This chapter describes an energy-efficient period-modulation-based capacitive-sensor interface [8]. This interface employs a combination of negative-feedback loops [6,7], time-domain chopping and three-signal auto-calibration techniques [2,3] to enable the use of simple, energy-efficient analog building blocks. It is shown that the energy consumption of the resulting interface is limited by its ability to operate in the presence of parasitic capacitors around the sensor capacitor. While maintaining the ability to handle parasitic capacitors up to five times larger than the sensor capacitance, the proposed interface consumes almost two orders of magnitude less energy than those reported in previous work [5,7].

3.2 Operating Principle

3.2.1 Capacitance-to-Time Conversion

Capacitive-sensor interfaces based on period modulation perform a capacitance-to-time conversion [3]. Figure 3.1 illustrates how this conversion is performed in the interface presented in this chapter. During phase φ_1 of a two-phase non-overlapping clock, the sensor capacitance C_x is connected between the supply voltage V_{dd} and a mid-supply common-mode reference V_{cm}. During the subsequent phase φ_2, it is connected between V_{ss} and the virtual ground of an active integrator, which is also biased at V_{cm}. As a result, a charge $V_{dd}C_x$ is transferred to the integration capacitor C_{int},

causing the output voltage V_{int} of the integrator to step up. A constant integration current I_{int} then removes the charge from C_{int}, bringing V_{int} back to its original level. A comparator at the output of the integrator detects when this happens. The time interval T_{msm} that passes from the start of phase φ_2 until V_{int} crosses the comparator's threshold is then proportional to C_x:

$$T_{msm} = \frac{V_{dd}}{I_{\text{int}}} C_x \quad . \tag{3-1}$$

This time interval can therefore be used as a measure of C_x and can be digitized by counting its duration in terms of the clock cycles of a faster reference clock. This digitization can be easily performed, for instance, by a counter in a microcontroller.

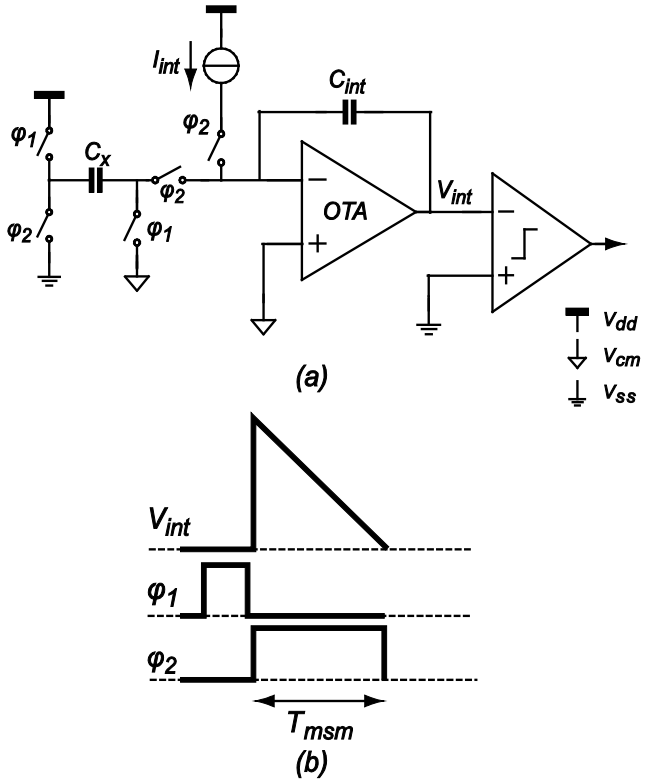


Figure 3.1: Operating principle of capacitance-to-time conversion: (a) simplified circuit diagram; (b) associated waveforms.

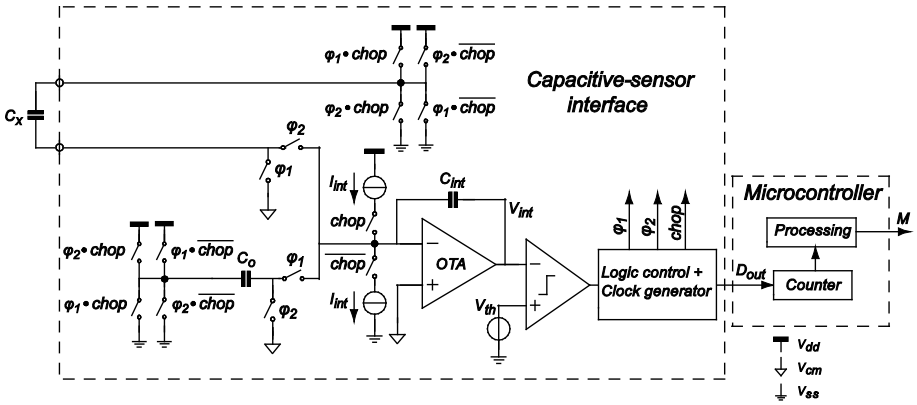


Figure 3.2: Block diagram of a period-modulator-based capacitive-sensor interface.

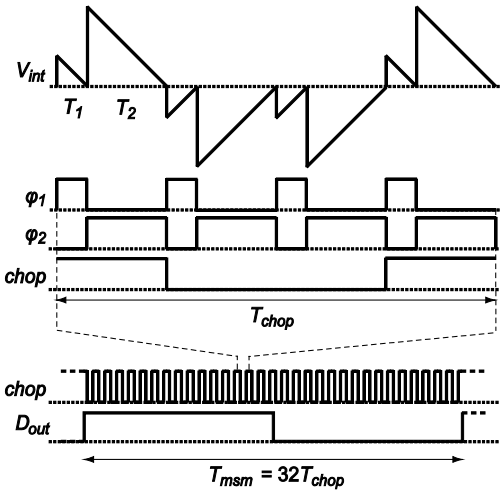


Figure 3.3: Timing diagram of the interface shown in Fig. 3.2.

Figure 3.2 shows how this basic principle can be applied in an asynchronously operating relaxation oscillator that self-generates the non-overlapping clock phases φ_1 and φ_2 [3]. Figure 3.3 shows the associated waveforms. In addition to the clock phases φ_1 and φ_2, the interface also self-generates a control signal chop, which will be discussed in more detail shortly. For now, we will assume that CHOP is HIGH. The switched-capacitor branch containing the sensor capacitor C_x then operates as before, giving rise to an output period T_2 proportional to C_x. Meanwhile, a small auxiliary capacitor C_0 is charged to the supply voltage. After the threshold

crossing, when phase φ_1 is high, the charge on C_0 is then transferred to the integrator capacitor C_{int} and removed by I_{int}, giving rise to a short output period T_1 proportional to C_0. This period, in turn, is used to charge C_x again, giving rise to a continuous oscillation with a period $T_1 + T_2$ proportional to $C_x + C_0$.

3.2.2 Chopping

To eliminate errors due to the low-frequency noise and offset of the interface circuit, the polarity of the integrated charge is periodically reversed in successive clock cycles under the control of the chop signal. This is done by switching capacitors C_x and C_0 from V_{dd} to V_{ss} when CHOP is HIGH, and switching them from V_{ss} to V_{dd} when CHOP is LOW. At the same time, the integration current I_{int} is switched between sourcing when CHOP is HIGH and sinking when CHOP is LOW, as shown in Fig. 3.2. One chopping cycle T_{chop} consists of four clock cycles in which the CHOP signal changes state twice. This chopping operation strongly suppresses the effects of the low-frequency noise of the integrator and the comparator, since the associated time errors change polarity in successive clock cycles and thus average out in the duration T_{chop} of a complete chopping period [2,3]. A complete measurement, in turn, consists of several successive chopping periods. In the present design, a total of 32 chopping periods are used, leading to a measurement-time period T_{msm} equal to:

$$T_{msm} = 32T_{chop} = 128\frac{V_{dd}}{I_{\text{int}}}(C_x + C_0) = aC_x + b \quad , \qquad (3\text{-}2)$$

which is a linear function of C_x.

3.2.3 Auto-Calibration

The gain and offset coefficients a and b in Eq. (3-2) are poorly defined, as they are affected by process variability and various circuit non-idealities, such as comparator delay, supply-voltage variations, component tolerances and their temperature dependencies. Therefore, the period time T_{msm} cannot be readily used to digitize C_x accurately. An auto-calibration technique is

applied to eliminate the uncertainty due to a and b [3]. As shown in Fig. 3.4, a multiplexer is added to the interface allowing either an offset capacitor C_{off}, a reference capacitor C_{ref}, or the sensor capacitor C_x to be measured. Thus, three consecutive measurements are performed, yielding three period times T_{off}, T_{ref}, and T_x, respectively. This sequence of three measurements repeats continuously, allowing the three period times to be measured by a digital counter using a single-wire interface. To allow this counter to identify which period is which, the control logic that generates the output signal produces two (short) output periods during time interval T_{off}, as illustrated in Fig. 3.4 [3]. Thus, it can be distinguished from time periods T_{ref} and T_x, during which only a single, typically much longer output period is generated. A digital representation M of C_x, independent of a and b, can then be obtained by performing the following calculation in digital post-processing:

$$M = \frac{T_x - T_{off}}{T_{ref} - T_{off}} = \frac{C_x}{C_{ref}} \quad . \tag{3-3}$$

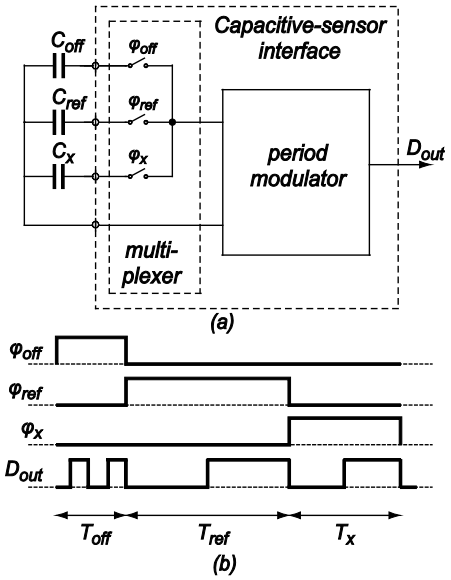


Figure 3.4: Period-modulation-based interface employing three signal-auto-calibration: (a) circuit diagram; (b) associated timing diagram.

This approach only requires the period modulator to be linear, i.e. the coefficients a and b to be independent of C_x and stable throughout the auto-calibration sequence. Since in M, this auto-calibration technique eliminates the effects of comparator delay, a low-speed energy-efficient comparator can be used, as long as its delay time does not become excessive compared to the clock period.

3.3 Output Swing Reduction

3.3.1 Period Modulator with Negative Feedback

The energy consumption of the interface is dominated by the OTA in the integrator, whose transconductance needs to be large enough to guarantee accurate charge transfer, as addressed in Chapter 2. To obtain this transconductance at a minimum supply current, a current-efficient OTA implementation is required. In this work, a simple cascoded telescopic OTA is used which outperforms the more frequently used folded-cascode OTA in current-efficiency, but at the expense of a smaller output-voltage swing.

In the interface of Fig. 3.2, the voltage swing at the output of the integrator is determined by the voltage step associated with charge transfer from C_x to C_{int}. Therefore, to reduce the output swing for a given value of C_x, a larger integration capacitor can be used. This solution, however, increases the load of the integrator, thus increasing the required transconductance. Moreover, it also increases the die size, in particular when large sensor capacitances need to be handled, since the integration capacitor will have to be larger than the sensor capacitance to keep the output swing within the supply rails.

To reduce the swing at the integrator's output without using a large integration capacitor, we employ negative feedback loops that regulate the charge transfer from C_x to C_{int} [7].

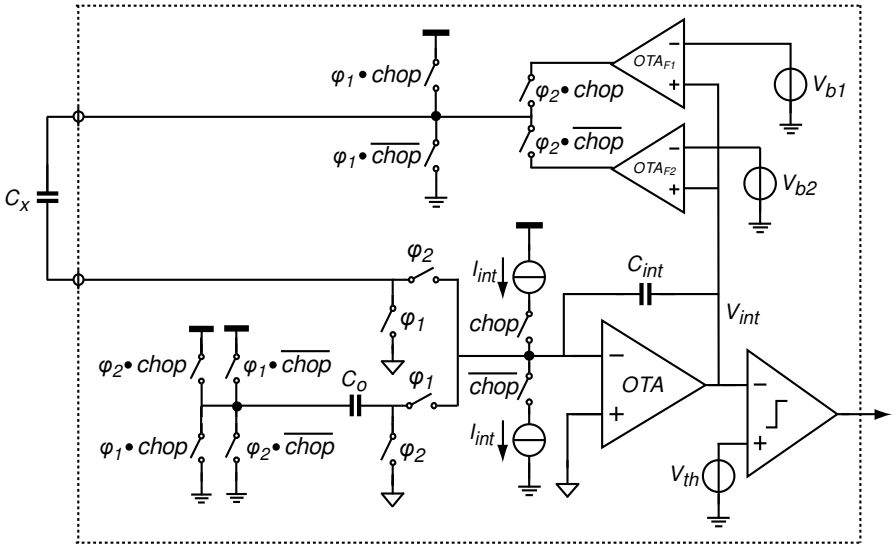


Figure 3.5: Block diagram of the period-modulator-based capacitive-sensor interface with negative feedback.

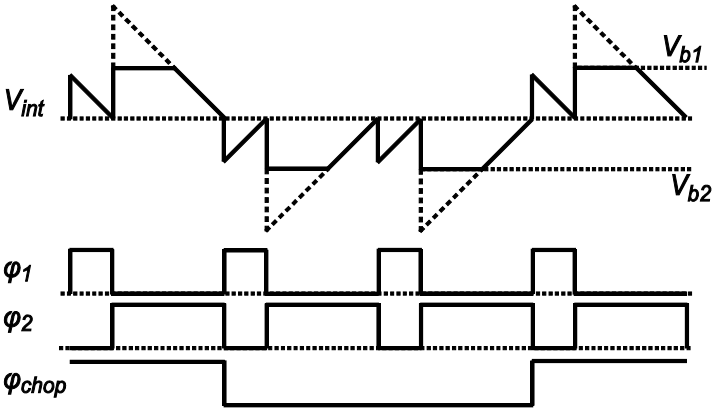


Figure 3.6: Timing diagram of the interface with the negative feedback shown in Fig. 3.5.

Figure 3.5[1] shows how this has been implemented (omitting the input multiplexer used for auto-calibration for simplicity). The switches that

[1] Initially, this technique was introduced in [6] as a way to extend the dynamic range of the interface circuit. Later on, in [7] the favorable noise properties of this circuit

connect C_x to V_{ss} and V_{dd} have been replaced by two feedback OTAs: OTA_{F1} and OTA_{F2}. Figure 3.6 shows their effect on the waveforms in the modulator. Depending on the chop signal, either OTA_{F1} or OTA_{F2} drives C_x during phase φ_2. We will refer to this OTA as OTA_F. Initially, the current provided by OTA_F is larger than I_{int}, causing the output of the integrator to increase. When the output of the integrator reaches the control voltage V_b, however, the current provided by OTA_F becomes equal to I_{int}, causing the output of the integrator to saturate at V_b. This situation continues until C_x is almost fully discharged. Then, the output of the integrator and the current of OTA_F go down, while I_{int} continues to remove the remaining charge stored in C_{int} until the integrator's output reaches the threshold level of the comparator. Since no charge is lost during this whole operation, the final amount of charge which is transferred from C_x to the integrator is not affected by these feedback loops. Thus, accurate capacitance-to-time conversion is maintained, i.e. Eq. (3-1) still holds. The control voltages V_{b1} and V_{b2}, which determine the high and low levels at which the integrator's output saturates, are chosen to fit the limited output swing of the telescopic OTA.

3.3.2 Design Trade-offs

The negative feedback loops employed to limit the integrator output swing are not unconditionally stable: the presence of parasitic capacitors from the terminals of the sensing capacitor to ground can give rise to instability [7] or can prevent the interfaces from oscillating, as will be explained below. This leads to a trade-off between power consumption and the ability to handle parasitic capacitances.

Figure 3.7 shows a simplified representation of the interface connected to a sensor with parasitic capacitors when phase φ_2 is HIGH[2]. In practice, the parasitic capacitors C_{p1} and C_{p2} can typically be assumed to be constant, while the sensor capacitance C_x varies across a certain range from $C_{x,min}$ to

---

were pointed out. In this thesis it will be shown that this remarkable circuit also has attractive features which lower power consumption.

[2] We assume that when φ is HIGH, the corresponding switches are conductive (closed), while when φ is LOW, these switches are non-conductive (opened).

$C_{x,max}$. When C_{p2} is significantly larger than $C_{x,min}$, a substantial part of the current provided by OTA_F is absorbed by C_{p2}. Assuming OTA_F has a transconductance g_{mF}, it provides a current $g_{mF} \cdot (V_b - V_{th})$ at the start of phase φ_2. A fraction $C_x / (C_x + C_{p2})$ of this current flows into C_x. To ensure proper operation of the interface, this fraction should be larger than the integration current I_{int}. Otherwise, insufficient current is available to transfer charge to the integration capacitor, which will stop the oscillation. This leads to the following minimum transconductance requirement for the feedback OTAs:

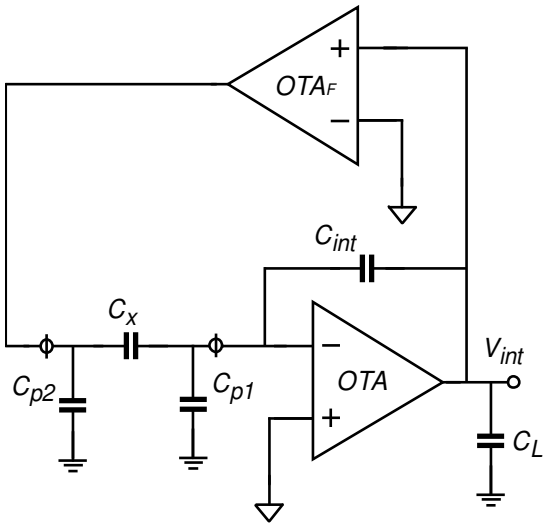


Figure 3.7: Simplified circuit diagram of the interface during phase φ_2.

$$g_{mF} > \frac{I_{\text{int}}\left(C_{x,min} + C_{p2}\right)}{\left(V_b - V_{th}\right)C_{x,min}} \qquad \text{(3-4)}$$

This equation shows that to handle parasitic capacitance at the drive side of the sensor capacitor, a larger feedback transconductance is required.

The feedback loop consisting of OTA_F, the sensor and the integrator is not unconditionally stable: the transconductance g_m of the integrator's OTA should be large enough to provide enough phase margin. Taking again the

current division between C_x and C_{p2} into account, the unity-gain frequency of this loop equals:

$$\omega_0 = \frac{g_{mF} C_x}{C_{int}\left(C_x + C_{p2}\right)} \quad . \tag{3-5}$$

Assuming the load capacitance of the integrator (which is dominated by the input capacitance of the comparator) is negligible compared to C_{p1}, the loop has a pole at a frequency ω_p of g_m / C_{p1}. To ensure a minimum phase margin of 45°, ω_p should be larger than ω_0. This leads to a minimum required transconductance g_m of the integrator OTA:

$$g_m > g_{mF} \frac{C_{p1} C_{x,max}}{C_{int}(C_{x,max} + C_{p2})} \quad , \tag{3-6}$$

where $C_{x,max}$ has been substituted for C_x to obtain the worst-case value across the sensor-capacitance range. By combining (3-6) and (3-4), a minimum g_m can be calculated for which stability is ensured over a given range of sensor capacitances and for given parasitic capacitances. Thus, the current consumption of the OTA can be minimized too.

3.4 Circuit Implementation

Figure 3.8 shows the complete transistor-level implementation of the interface. Using the approaches discussed in Section 3.2, a fairly compact implementation is obtained. The left part shows the two feedback OTAs, each of which consists of a simple differential pair biased at a tail current of 1 μA, and a current mirror that scales up the output current of the differential pair by a factor of 6. In line with the discussion in Section 3.3, this current-mirror ratio is a trade-off between the ability to handle parasitic capacitance and power consumption. This design is optimized to handle parasitic capacitances up to five times larger than the sensor capacitance. The integrator employs a telescopic OTA with an integration capacitor C_{int} of 4 pF. The transconductance of this OTA is optimized using Eq. (3-6). To

obtain the required transconductance at a minimum supply current, the input transistors of the OTA are sized to operate in weak inversion, resulting in a current consumption of 34μA. The control voltages V_{b1} and V_{b2} are designed to be 2.6V and 1.4V, respectively, which is in line with the output swing of the telescopic OTA.

The comparator consists of a simple differential pair with a current-mirror load, followed by a common-source stage. The errors due to its propagation delay are eliminated by the three-signal auto-calibration. On the other hand, the delay introduced by comparator should not be so large that it stops the oscillation. As a compromise, for the comparator we selected a supply current of only 9 μA.

The integration currents I_{int} of 1μA are generated by degenerated MOS current sources using large MOS transistors to achieve a low flicker-noise corner frequency. This is of particular importance, since errors due to the low-frequency noise of these current sources are not reduced by the chopping technique. The auto-calibration does reduce these errors, but only to the extent that they are correlated between the successive measurements of the offset, reference and sensor capacitances. The current source are sized such that their 1/*f* noise corner is low enough to ensure that this is the case for measurement times up to 100ms, which corresponds to sensor capacitance values up to 100pF.

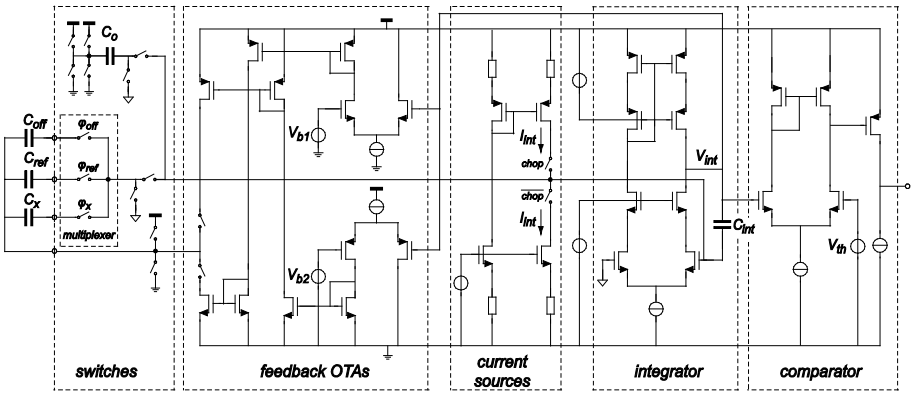
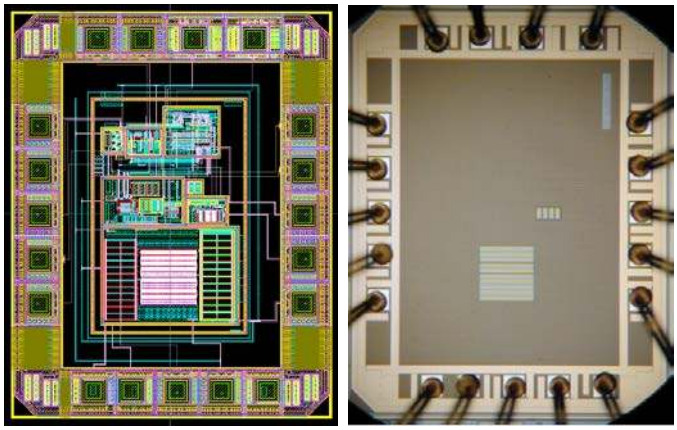


Figure 3.8: Complete transistor-level implementation of the interface.

The clock signals φ_1, φ_2, and the chop are derived from the output of the comparator using a simple on-chip digital state machine (not shown). For test purposes, the control voltages V_{b1} and V_{b2} and the threshold voltage V_{th} are generated off-chip in the current prototype, but they can be easily generated on-chip without significantly increasing the supply current or die size, using simple diode-connected MOS transistors biased at currents far below the supply current of the OTA.

3.5 Measurement Results

The proposed interface has been designed and fabricated in standard 0.35µm CMOS technology. The techniques applied in the interface do not rely on any particular features of this technology and are therefore expected to be equally applicable to designs in more modern CMOS technologies. Figure 3.9 shows a chip photograph. Since details of the layout are invisible due to the metal exterior, a layout plot is also shown in this figure. The active area (excluding pads) is 0.51 mm^2.



(a) *(b)*

Figure 3.9: (a) Layout plot and (b) photograph of the chip.

3.5.1 Measurements Results of the Changing Input Capacitor

The performance of the chip has been evaluated experimentally using discrete ceramic capacitors up to 50pF for C_x and C_{ref}. The offset

capacitance C_{off} needed to perform auto-calibration consists of the combined parasitic capacitances on the chip and the test PCB. The output signal of the interface (encoded as shown in Fig. 3.4) was digitized by a counter in a microcontroller, which also performed the digital post-processing required for auto-calibration. A 60MHz clock frequency was used for the counter, which is high enough to ensure that the quantization noise associated with the counting is much lower than the thermal noise of the interface.

To determine the resolution of the interface, we measured the standard deviation of the post-processed output M as a function of C_x. To demonstrate that the negative feedback loops of the interface can readily extend the input-capacitance range without increasing the integration capacitor C_{int}, the resolution was measured across three C_x ranges, corresponding to the ranges of 6.8pF, 27pF and 47pF. The results are shown in Fig. 3.10. Two trends can be observed in this figure: the measured resolution decreases with an increase in C_x, and with a decrease in C_{ref}. In spite of this, the measured resolution exceeds 15 bits for almost all the capacitance values measured.

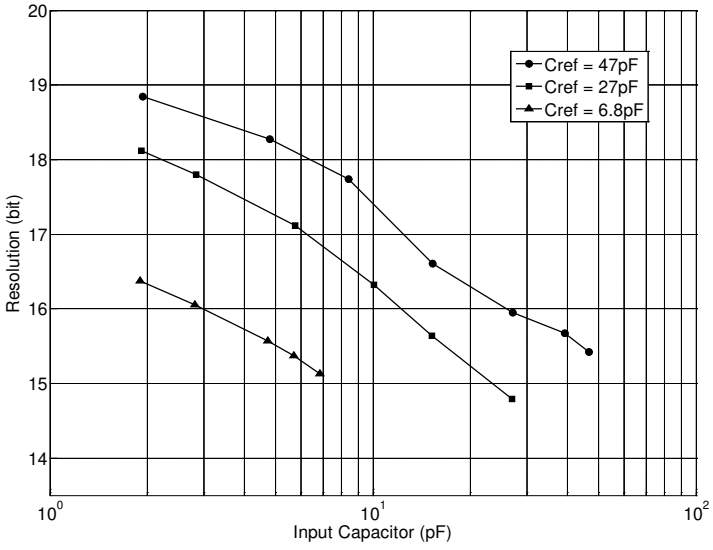


Figure 3.10: Measured resolution as a function of C_x for three values of C_{ref}, for C_p = 0 pF.

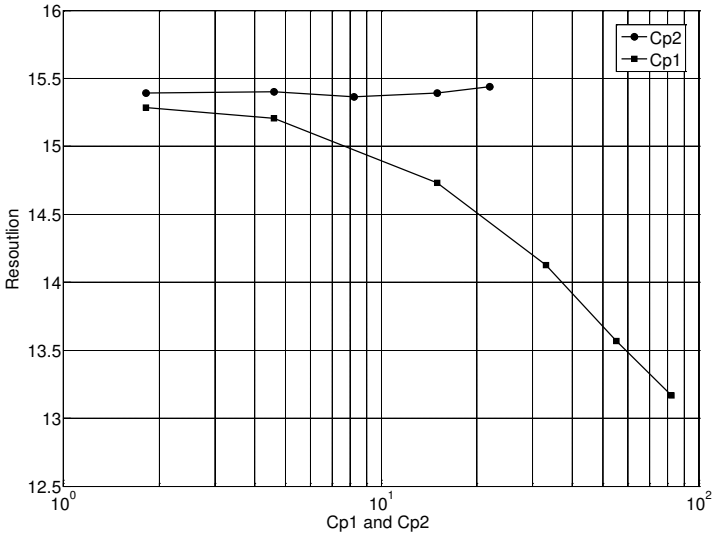


Figure 3.11: Measured resolution as a function of C_{p1} and C_{p2} for C_x = 5.6pF and C_{ref} = 6.8pF.

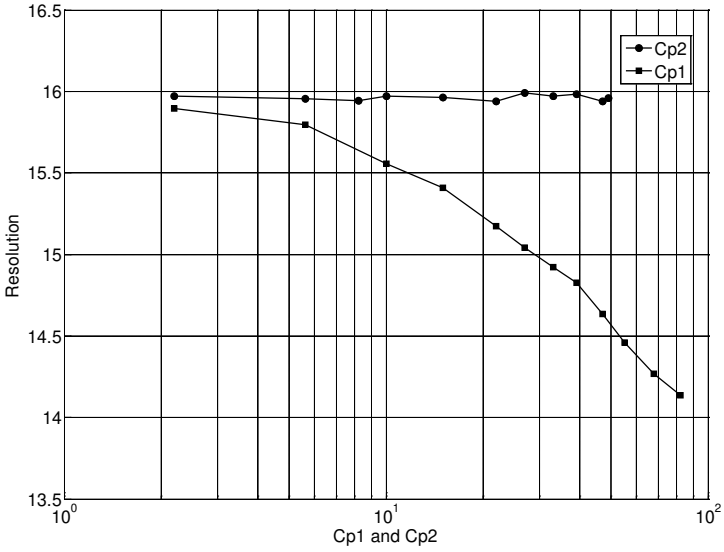


Figure 3.12: Measured resolution as a function of C_{p1} and C_{p2} for C_x = 12pF and C_{ref} = 27pF.

The quantitative analysis of the resolution of the interface is presented in following. The trends that can be observed in Fig. 3.10 can be explained by considering how time jitter on the three period times T_x, T_{ref} and T_{off} affects the auto-calibrated measurement result M given by Eq. (3-3). Assuming that the standard deviation of the jitter on these period times equals $\sigma(T_x)$, $\sigma(T_{ref})$ and $\sigma(T_{off})$, respectively, and assuming that T_{off} is much smaller than T_x and T_{ref}, the resulting standard deviation of M can be written as:

$$\sigma^2(M) = \left(\frac{\sigma(T_x)}{T_{ref}} \right)^2 + \left(\frac{\sigma(T_{ref})T_x}{T_{ref}^2} \right)^2 \quad . \tag{3-7}$$

This equation readily shows that for a given value of C_x (and hence a given value of T_x and $\sigma(T_x)$), $\sigma(M)$ can be reduced (and thus the resolution increased) by using a larger C_{ref} to obtain a larger T_{ref}. Conversely, for a given value of C_{ref}, the resolution drops for larger values of C_x (and hence larger values of T_x), because the effect of $\sigma(T_{ref})$ increases. Moreover, $\sigma(T_x)$ will also increase for larger values of C_x, because the noise gain of the integrator increases.

3.5.2 Measurements Results of Changing Parasitic Capacitor

Figures 3.11 and 3.12 show the effect of the parasitic capacitors C_{p1} and C_{p2} on the measured resolution for two combinations of C_x and C_{ref}. The resolution stays almost constant as C_{p2} increases until the point that C_{p2} becomes too large and draws too much current from the feedback loop, preventing the interface from working, as discussed in Section 3.3. The point at which this happens is in reasonable agreement with the design target of $5C_x$. Increasing C_{p1} has two effects on the system performance. Similar to an increase in C_x, it increases the noise gain of the integrator, resulting in a decreased resolution, as shown in Figs. 3.11 and 3.12. Moreover, it will increase the loading of the integrator and thus decrease the phase margin of the negative feedback loop, as discussed in Section 3.3. For sensor capacitances beyond the end points of the curves in Figs. 3.11 and 3.12, this lack of phase margin prevents the interface from producing a proper output signal.

3.5.3 Measurements Results of Linearity and PSRR

The non-linearity of the interface has been determined using the method presented in [7,18]. By measuring four combinations of three stable reference capacitors: C_1, C_2, $C_1 + C_3$ and $C_2 + C_3$, the non-linearity can be determined from the corresponding measurement results M_1, M_2, M_{1+3} and M_{2+3} as:

$$\lambda = \frac{M_{2+3} - M_{1+3}}{M_2 - M_1} - 1 \quad . \tag{3-8}$$

This expression is accurate even in the presence of parasitic capacitors, provided these capacitors are equal for the four measurements. Using combinations of the discrete capacitors 2.1pF, 4.2pF, 10pF and 22pF, a non-linearity less than 2×10^{-4} was obtained, corresponding to a linearity of better than 12 bits.

To evaluate the energy consumption of the interface, the measurement time and power consumption are of interest. Since the measurement time increases for larger values of C_x, the longest measurement time is obtained when C_x equals C_{ref}, assuming that $C_x \leq C_{ref}$. For a C_{ref} of 6.8pF, this maximum is 7.6ms. The chip consumes 64μA from a 3.3V supply, which then corresponds to an energy per measurement of 1.6μJ. The majority of the supply current (49μA) is static current consumed by the analog circuitry, while 15μA concerns dynamic current consumed by the digital circuitry.

Due to the auto-calibration technique applied in the interface, variations in its supply voltage V_{dd} should have little effect on the measured capacitance, provided the supply voltage remains stable during the three consecutive measurements of the auto-calibration sequence. This has been verified by sweeping the supply voltage from 2.6V to 3.7V for fixed values of C_x and C_{ref} of 6.8pF each. The measured capacitance value only changes by less than 23 ppm across this range, which corresponds to a supply sensitivity of less than 21 ppm/V.

3.6 Conclusion

An energy-efficient capacitive-sensor interface has been presented. The interface circuit is based on the use of a period modulator implemented with compact, energy-efficient building blocks. Auto-calibration is employed to achieve a well-defined transfer function in spite of the non-idealities of these building blocks. This enables the use of a simple telescopic OTA in the integrator and a slow, low-power comparator. The limited output swing of the OTA is accommodated using negative feedback loops. Measurement results show, in comparison with previous interfaces based on period modulation, not only comparable resolution and linearity, but also a significant improvement in energy efficiency.

3.7 References

[1] L. K. Baxter, *Capacitive Sensors: Design and Applications*. New York: IEEE Press, 1997.

[2] G. C. M. Meijer, *Smart Sensor Systems*. Chichester, UK: Wiley, 2008.

[3] F. van der Goes, "Low-cost smart sensor interfacing," Ph.D. dissertation, Delft University of Technology, Delft, the Netherlands, 1996.

[4] X. Li and G. C. M. Meijer, "An accurate interface for capacitive sensors," *IEEE Trans. Instrum. Meas.*, vol. 51, no. 5, pp. 935-939, Oct. 2002.

[5] A. Heidary, S. Heidary Shalmany and G. C. M. Meijer, "A flexible low-power high-resolution integrated interface for capacitive sensors," in *Proc. IEEE Int. Symp. on Industrial Electronics (ISIE)*, Bari, Italy, July 2010, pp. 3347-3350.

[6] G. C. M. Meijer and V. P. Iordanov, "SC front-end with wide dynamic range," *Electron. Letters*, vol. 37, no. 23, pp. 1377-1378, Nov. 2001.

[7] A. Heidary and G. C. M. Meijer, “Features and design constraints for an optimized SC front-end circuit for capacitive sensors with a wide dynamic range,” *IEEE J. Solid-State Circuits*, vol. 43, no. 7, pp. 1609-1616, July 2008.

[8] W. Bracke, R. Puers and C. Van Hoof, *Ultra Low Power Capacitive Sensor Interfaces*. Dordrecht, the Netherlands: Springer, 2007.

[9] D.-Y. Shin, H. Lee and S. Kim, “A delta-sigma interface circuit for capacitive sensors with an automatically calibrated zero point,” *IEEE Trans. Circuits and Systems II*, vol. 58, no. 2, pp. 90-94, Feb. 2011.

[10] S. A. Jawed, D. Cattin, M. Gottardi, N. Massari, A. Baschirotto, and A. Simoni, “A 828μW 1.8V 80dB dynamic range readout interface for a MEMS capacitive microphone,” in *Proc. ESSCIRC*, Edinburgh, UK, Sept. 2008, pp. 442-445.

[11] AD7156 datasheet, Analog Devices [Online]. http://www.analog.com.

[12] M. Paavola, M. Kämäräinen, E. Laulainen, M. Saukoski, L. Koskinen, M. Kosunen and K. A. I. Halonen, “A micropower ΔΣ-based interface ASIC for a capacitive 3-axis micro-accelerometer,” *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp. 3193-3210, Nov. 2009.

[13] H. Danneels, K. Coddens and G. Gielen, “A fully-digital, 0.3V, 270nW capacitive sensor interface without external references,” in *Proc. ESSCIRC*, Helsinki, Finland, Sept. 2011, pp. 287-290.

[14] Z. Tan, R. Daamen, A. Humbert, K. Souri, Y. Chae, Y. Ponomarev and M. A. P. Pertijs, “A 1.8V 11μW CMOS smart humidity sensor for RFID sensing applications,” in Proc. *A-SSCC*, Jeju, Korea, Nov. 2011, pp. 105-108.

[15] P. Bruschi, N. Nizza and M. Piotto, “A current-mode, dual slope, integrated capacitance-to-pulse duration converter,” *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 1884-1891, Sept. 2007.

[16] P. Bruschi, N. Nizza and M. Dei, “A low-power capacitance to pulse width converter for MEMS interfacing,” in *Proc. ESSCIRC*, Edinburgh, UK, Sept. 2008, pp. 446-449.

[17] Z. Tan, M. A. P. Pertijs and G. C. M. Meijer, “An energy-efficient 15-bit capacitive sensor interface,” in *Proc. ESSCIRC*, Helsinki, Finland, Sept. 2011, pp. 283-286.

[18] A. Heidary, “A low-cost universal integrated interface for capacitive sensors,” Ph.D. dissertation, Delft University of Technology, Delft, the Netherlands, 2011.

Chapter 4

Energy-Efficient Capacitive-Sensor Interfaces using Delta-Sigma Modulation

4.1 Introduction

This chapter discusses the system design and circuit implementation of energy-efficient capacitive-sensor interfaces using delta-sigma modulation. The interfaces presented in this chapter are dedicated for humidity sensing in RFID applications. For a better understanding of the motivation and specifications of the interface design, it is beneficial to start with the background of RFID applications. Afterwards, the sensing element will be discussed and the system-level design of the delta-sigma modulator for capacitive-sensor interface is addressed in detail. Two state-of-the-art prototypes will be presented which have been implemented in 0.16μm CMOS technology. Measurement results show that the first design achieves a 13-bit effective resolution for a measurement time of 10.2ms while consuming only 5.86μA from a 1.8V supply. The second design achieves a

12.5-bit effective resolution for a measurement time of 0.8ms while consuming only 8.6μA from a 1.2V supply.

4.2 System Background

4.2.1 RFID Application Introduction

Today, RFID tags are a rapidly growing billion-euro business, the bulk of which consists of product identification and tracking in retail and security applications. Equipping RFID tags with sensors, however, will open up a host of other applications. An example of a high-volume application is the monitoring of perishable food products, in which the use of RFID technology will enable wireless measurement of key parameters such as temperature, humidity, and CO_2 concentration at various stages in the supply chain [1,2,3]. The information thus obtained enables the shelf life to be more accurately predicted thus significantly reducing the waste caused by spoilage [2,3]. Such a solution, however, is only economically viable if the tags can be produced in volume at a very low cost. This calls for the use of CMOS-compatible sensors that can be co-integrated with the RFID circuitry, and the use of low-cost printed batteries, or even no batteries at all (passive RFID). The latter implies that the sensors should be able to operate at very low energy levels (<50nJ/measurement) [1,2].

Relative humidity (RH) is an important parameter used for monitoring perishable food products [1]. Among different humidity-sensing approaches, capacitive humidity sensing is the most attractive one for use in RFID tags, as the sensing element can be implemented in CMOS technology [4] and does not consume static power. A co-integrated energy-efficient capacitive-sensor interface is required to produce a digital output that is a well-defined function of relative humidity. Existing approaches, however, either use discrete components providing only a voltage output [1,2,4], or consume too much energy [4-6]. This chapter addresses these issues by presenting energy-efficient capacitive-sensor interfaces using delta-sigma modulation to realize a fully integrated CMOS humidity sensor that meets the stringent RFID requirements [7,8]. These interfaces have been designed for humidity sensing in RFID applications while consuming ultra-low energy. Before the

discussion on interface design, the properties of the capacitive humidity-sensing element will be described.

4.2.2 Capacitive Humidity-Sensing Elements

Capacitive humidity sensors are the most widely used class of humidity sensors. In such sensors, a change in relative humidity (RH) is detected by a humidity-induced change in the dielectric constant of a sensing layer, which in our case is a thin polyimide film. This approach provides high sensitivity, and a linear, stable response [4]. The advantages of capacitive humidity sensors also include their potentially high energy-efficiency, as in principle no static power is consumed, and their compatibility with standard CMOS fabrication technologies, as the humidity-sensing capacitor can be fabricated in the top metal layer on the silicon [9].

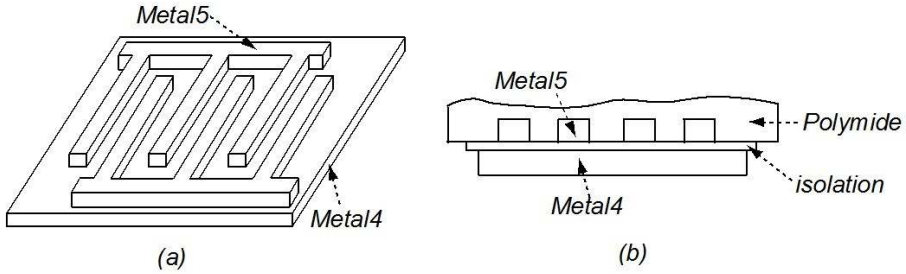


Figure 4.1: The sensing element of a CMOS-compatible fully integrated capacitive humidity sensor.

Figure 4.1 shows the sensing element of the CMOS-compatible fully integrated capacitive humidity sensor to be designed. As is shown, it consists of interdigitated electrodes in the top metal layer (metal 5) covering an area of 100μm ×100μm. The sensing capacitor is covered by a humidity-sensitive polyimide layer, as shown in Fig. 4.1 (b). Metal 4 is used to shield this structure from circuitry that can be integrated underneath the sensing capacitor. Figure 4.2 shows a prototype of the finger structure of a sensing element viewed from above. Figure 4.3 shows the cross section of the sensing element.

The polyimide (not shown in Fig. 4.2) has been selected based on its sensitivity to humidity, its linearity, and its compatibility with the tool-set and the materials already used in standard CMOS fabrication. The resulting sensing element has a sensitivity around 1 fF/%RH on a nominal capacitance around 0.8 pF. The sensitivity can be changed with the thickness of the polyimide layer. This is also the reason for the differences in the sensitivity of various samples of prototype sensors, as presented in Sections 4.6 and 4.7. Its cross sensitivity to CO_2 and O_2 is less than 2% and 1% of the humidity sensitivity, respectively. Figure 4.4 shows an electrical model of the capacitive sensing element. Besides the sensing capacitor C_x itself, it also includes a shunt resistor R_x and two parasitic capacitors C_{p1} and C_{p2}. The two parasitic capacitances are mainly due to the interconnect. When co-integrating the sensor with the associated circuitry, the parasitic capacitances C_{p1} and C_{p2} can be smaller than 0.3 pF. The shunt resistance (R_x) is larger than 1 GΩ.

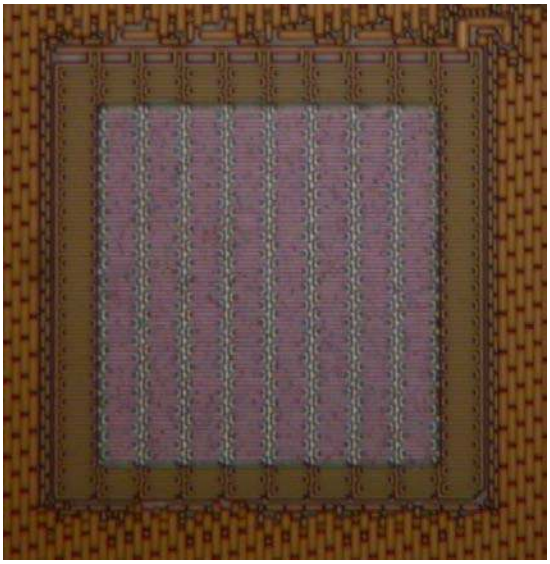


Figure 4.2: Finger structure of the sensing element prototype (top view) realized in CMOS technology.

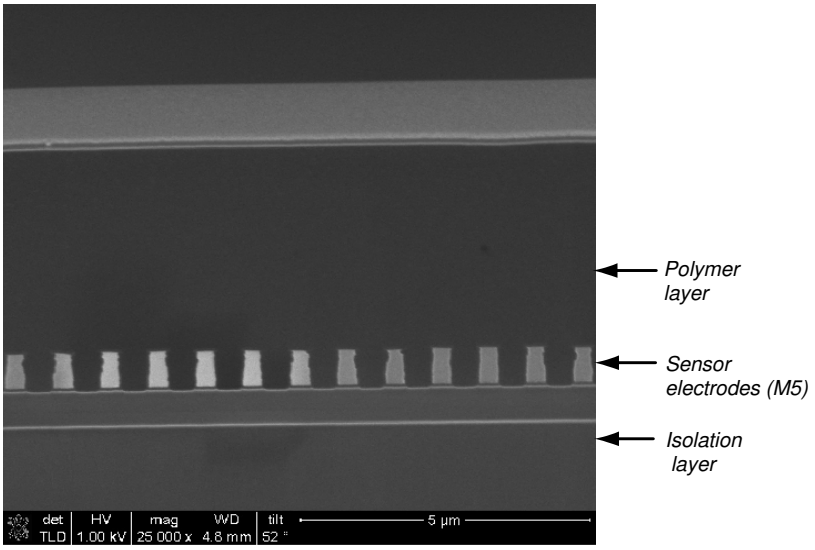


Figure 4.3: Cross section of the humidity-sensing element prototype.

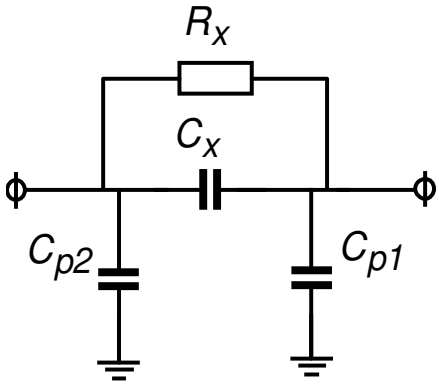


Figure 4.4: Electrical model of the capacitive sensing element.

4.3 Energy-Efficient Capacitive-Sensor Interface

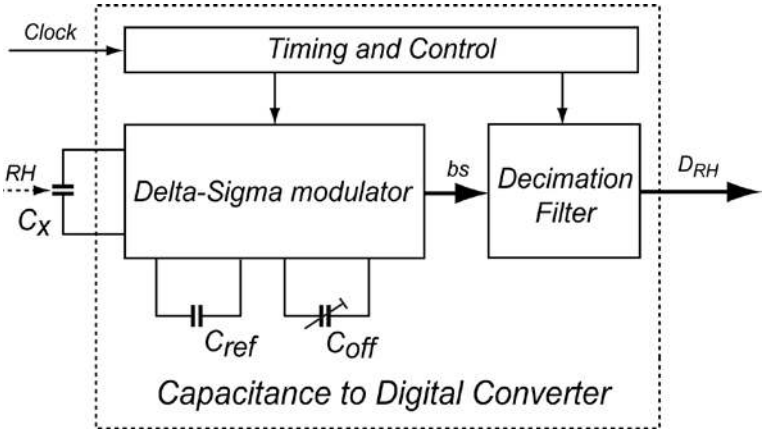


Figure 4.5: Block diagram of the smart humidity sensor.

Figure 4.5 shows a block diagram of the smart humidity-sensor presented in this chapter. C_x is the humidity-sensitive capacitor. The output of the smart humidity sensor, D_{RH}, is a digital representation of relative humidity. A *ratio-metric* measurement is performed: the ratio of C_x and an on-chip reference capacitor C_{ref} (0.4pF) is determined by a delta-sigma modulator. Since C_x has a baseline value of about 0.8pF, which can vary substantially from device to device, a programmable offset capacitor C_{off} is used to subtract this baseline capacitance from C_x. This offset capacitor can be digitally programmable from 0 pF to 1.5pF with a step size of 0.1pF. The delta-sigma modulator is used to design an energy-efficient capacitive-sensor interface. Its resolution and accuracy do not rely on component matching, which for Nyquist-rate converters is usually the limiting factor [10]. Traditional delta-sigma modulators were mainly used in telecommunications, audio and consumer electronics, and in applications where the input signal was assumed to be a "busy" signal. Thus the quantization noise is uniformly distributed throughout the sampling frequency band which refers to white noise. However, in sensor applications, for instance humidity sensing and pressure sensing, the input signal is band-limited or even near to DC. The delta-sigma modulators designed for low-frequency applications are the so-called incremental converters [11].

In this chapter, two prototypes of such incremental delta-sigma converters are presented. The first one, which is a second-order incremental converter-based capacitive-sensor interface, provides a resolution of around 13 bits. The second prototype is a third-order incremental converter-based capacitive-sensor interface with a resolution of 12.5 bits. Both converters use charge balancing to produce a bit-stream bs whose bit-density is proportional to the ratio of ($C_x - C_{off}$) and C_{ref}. A simple decimation filter is used to filter the quantization noise from bs and convert it into a digital value D_{RH}.

To illustrate the charge-balancing process applied in the capacitive-sensor interfaces, Fig. 4.6 shows a first-order delta-sigma converter. The bipolar operation is adopted in the design and after an initial reset of the integrator, a charge proportional to $C_x - C_{off}$ is integrated in every clock cycle of the conversion, in addition to a charge proportional to C_{ref} with a polarity that depends on the bit-stream output S_{bit}. The negative feedback in the modulator ensures that the former charge is balanced by the latter, resulting in a zero average charge flowing into the loop filter (the integrator) which yields the equation:

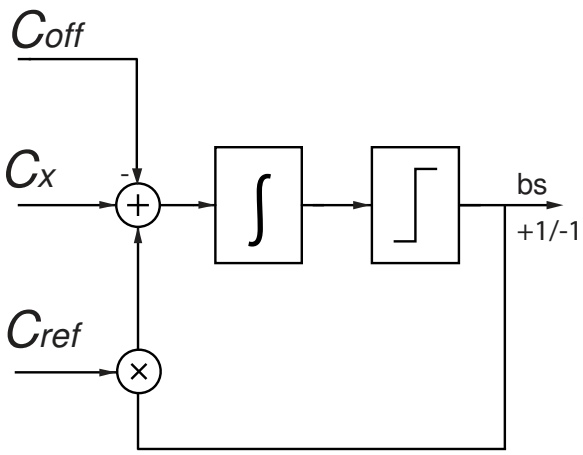


Figure 4.6: First-order delta-sigma modulator-based capacitive-sensor interface using charge balancing.

$$\left(C_x - C_{off}\right) - \mu \cdot C_{ref} + (1-\mu) \cdot C_{ref} = 0 \quad , \qquad (4\text{-}1)$$

where μ is the bit-density which is the ratio that the number "ONES" divide all the number of bits by. Solving μ gives:

$$\mu = \frac{C_x - C_{off}}{2C_{ref}} + \frac{1}{2} \quad , \tag{4-2}$$

which is the desired ratiometric function of C_x, and which equals 0.5 for $C_x = C_{off}$.

To obtain an energy-optimized capacitive-sensor interface, the oversampling ratio (OSR), i.e. the number of clock cycles required to produce a digital output, should be minimized. Based on the size of the sensor capacitance, a minimum oversampling ratio is required to bring the thermal noise (kT/C noise) to a level that is in agreement with the required resolution. A first-order delta-sigma modulator would require a much higher OSR to reduce the quantization noise to the same level. In sensing applications, higher-order modulators require much fewer conversion cycles to achieve a certain resolution than a first-order modulator. With a constant clock frequency, fewer conversion cycles means less energy consumption. Therefore, to lower energy consumption, higher-order modulators are preferred.

There are basically two approaches to implement a higher-order modulator: the use of (a) a single higher-order loop filter or (b) a multi-stage (MASH or cascading) low-order modulator. Theoretically, the usable input range of a first-order modulator is as large as the full-scale input S_{FS}, at which overloading of the integrator outputs is prevented. In a single-loop when the order of the loop filter increases, then the circuit complexity also increases, while the maximum input is limited to a fraction of the full-scale. This is because when the input approaches the full-scale, the modulator may become unstable. Typically, the usable input range for a second-order modulator is about 0.75 S_{FS}. For third-order delta-sigma converters this value shrinks to 0.67 S_{FS} [10,11]. These values are conservative and valid for most design cases. Moreover, the high-order single-loop modulators have a stability problem. This problem can be eased by using the structure of a cascade modulator, also called a multi-stage or MASH (for Multi-stAge noise-SHaping) modulator [10]. However, a big drawback of a MASH

structure is its sensitivity to component mismatches. In the MASH structure, the high resolution is achieved by accurate cancellation of the quantization noise from previous stages. This requires accurate matching between the analog transfer functions and the digital ones. Any mismatch between these two transfer functions will cause quantization noise "leakage", which will degrade the achievable resolution. In the designs presented in this thesis, for system simplicity and easy backhand digital processing (decimation filter), we apply single-loop higher-order incremental delta-sigma modulators.

It makes sense to increase the order of the modulator such that the minimum OSR required for quantization noise reduction is less than that required for the reduction of thermal noise. In doing so, it should be taken into account that the usable input range (relative to C_{ref}) shrinks when increasing the order of the modulator. While a first-order modulator can handle inputs over the entire full-scale range of $\pm C_{ref}$, the maximum input of higher-order single-loop modulators should be limited to prevent the integrators from overloading. As mentioned above, the usable input ranges for a second- and a third-order modulator are $\pm 0.75\ C_{ref}$, and $\pm 0.65\ C_{ref}$, respectively [10].

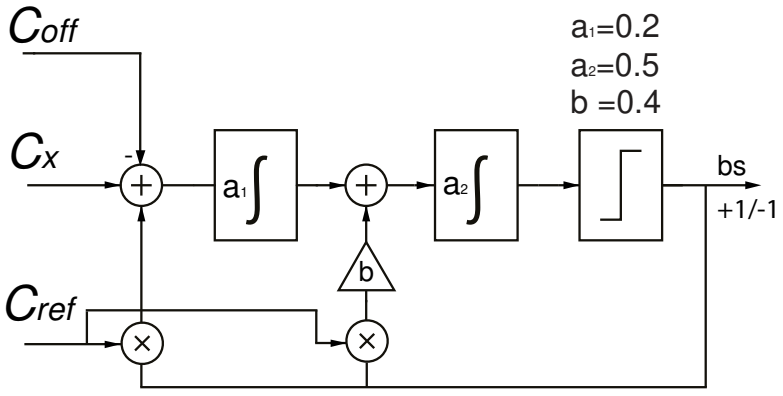


Figure 4.7: Topology of the capacitive-sensor interface based on a second-order delta-sigma modulator.

The first prototype is based on a second-order incremental converter (Fig. 4.7). Figure 4.8 shows that a second-order modulator needs 500 cycles to reduce the quantization noise to the 13-bit level.

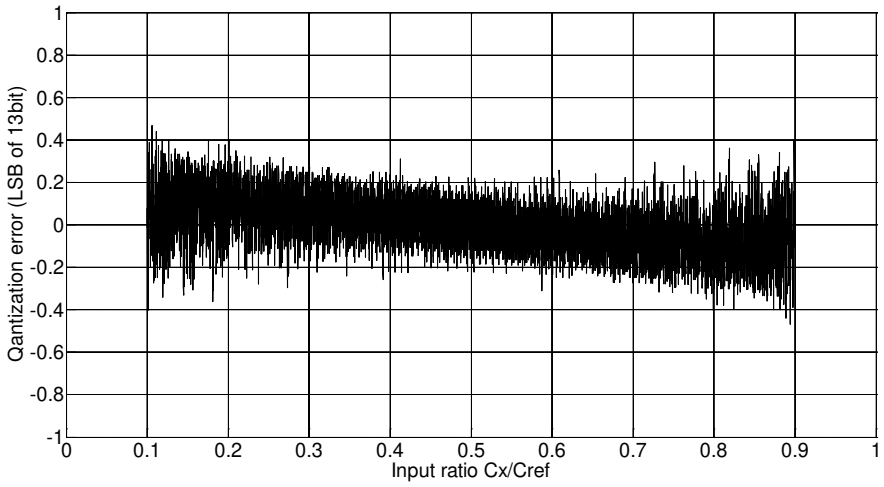


Figure 4.8 Quantization error of a simulated second-order incremental converter (conversion cycles $N = 500$).

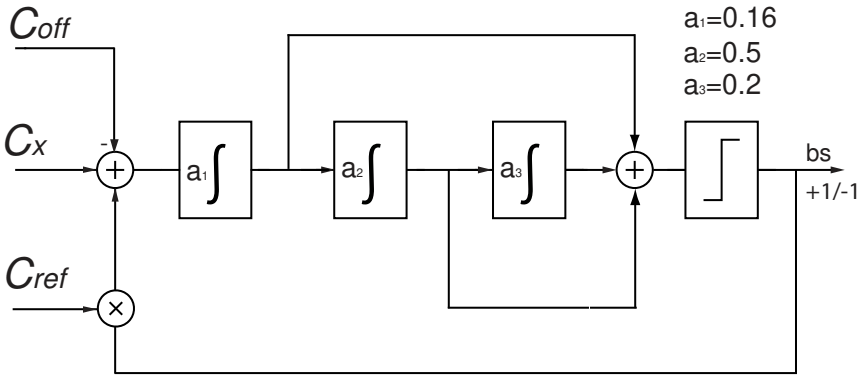


Figure 4.9: Topology of the capacitive-sensor interface based on a third-order delta-sigma modulator.

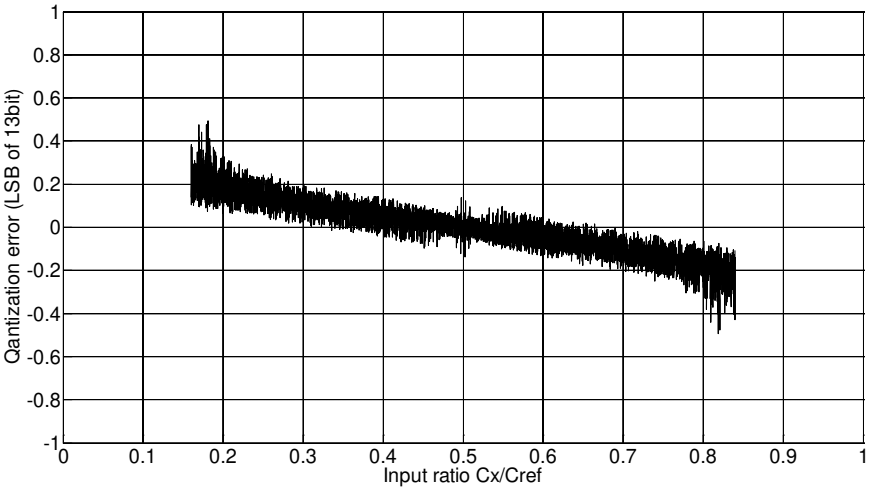


Figure 4.10 Quantization error of a simulated third-order incremental converter (conversion cycles $N = 103$).

Figure 4.9 shows a block diagram of the proposed readout structure of the second prototype of the humidity sensor. This design uses a third-order incremental converter. A feed-forward loop-filter is used, since it decreases the output swing of the integrators, which improves the linearity of the modulator [12]. Figure 4.10 shows that the third-order converter, only needs 100~120 cycles to achieve the target resolution [11]. It can be concluded that a third-order converter is the optimum choice: While using a second-order modulator would lead to a quantization-noise-limited design with an unnecessarily high number of cycles, the use of a fourth-order modulator would only increase complexity without enabling a further reduction in the number of cycles. Compared to conventional implementations of this topology [12], a direct feed-forward path from the input to the single-bit quantizer is omitted, as it would require duplicating the sensing capacitor and does not significantly help in reducing the swing of the integrators when a single-bit quantizer is used. The modulator coefficients chosen lead to a usable input range of $\pm 0.65\ C_{ref}$. In the next sections, details of the designs and their implementations will be presented together with the measurement results.

4.4 Energy-Efficient Capacitive Humidity Sensor I

4.4.1 Circuit Implementation

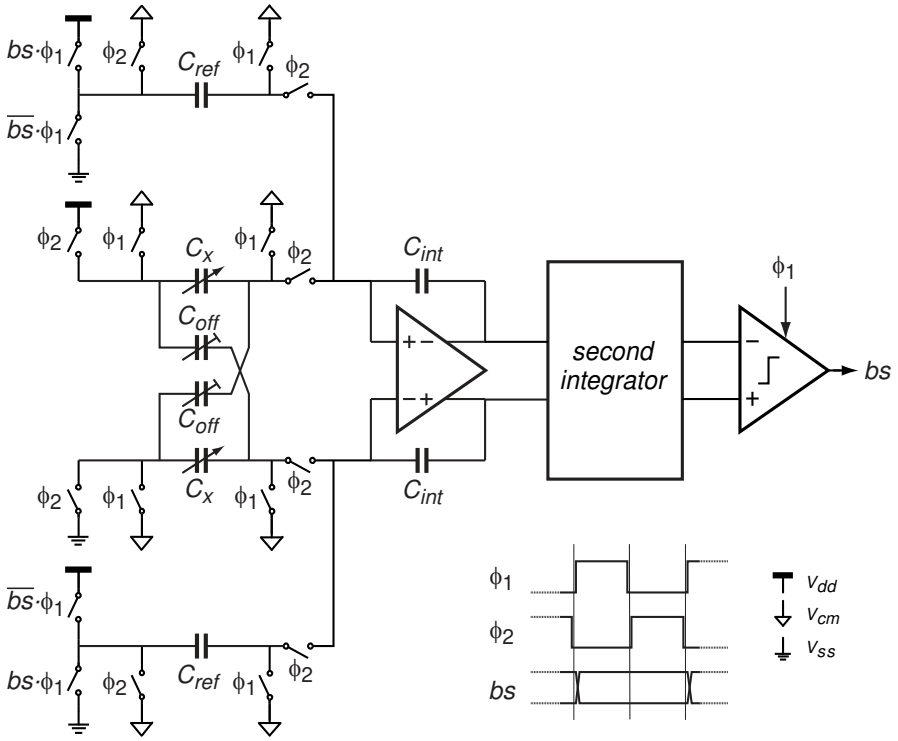


Figure 4.11: Complete circuit diagram of the front-end and delta-sigma modulator.

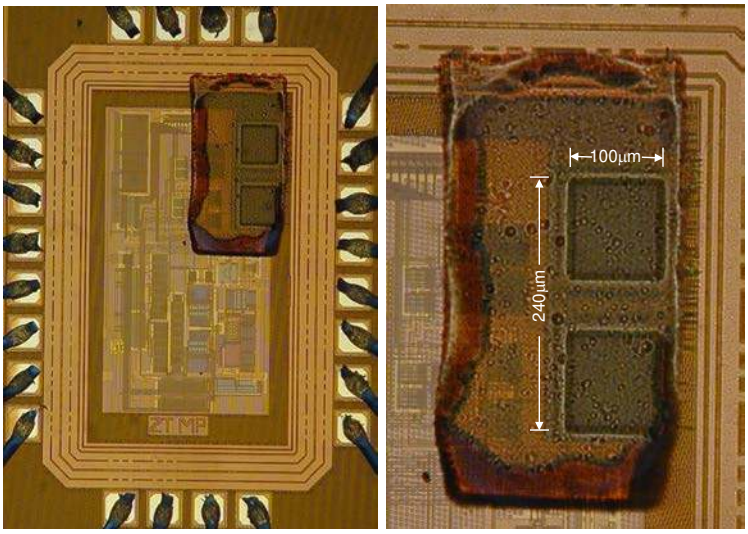
Figure 4.11 shows the circuit diagram of the first smart humidity sensor prototype. In this design, a fully differential circuit topology is used [10]. This topology reduces the sensitivity to noise coupling, which makes the circuit more suitable for co-integration with the other circuitry of an RFID sensor tag.

To provide a fully differential input signal, two sensing capacitors C_{x1} and C_{x2} are directly coupled to the first integrator. These capacitors are switched between V_{ref} and ground so that a differential charge proportional to the sensor capacitance is integrated. Programmable offset capacitors C_{off1} and

C_{off2} are cross-coupled between the sensor capacitors, resulting in the desired effective capacitance of $C_x - C_{off}$. The reference capacitors C_{ref1} and C_{ref2} are driven in the same way as C_x, but the polarity of their connection to the integrator depends on the bit-stream bs, resulting in the charge balancing described by Eq. (4-2). Both the offset capacitors and the reference capacitors are implemented using fringe capacitors in the first three metal layers.

To achieve sufficient signal swing and DC gain, the two integrators of the modulator are implemented using fully differential folded-cascode OTAs with switched-capacitor common-mode feedback. At a 1.8V supply and a bias current of 1.6 µA, the OTAs provide 85 dB of DC gain. The one-bit quantizer is implemented by a low-power dynamic comparator consuming 0.4µA. Including a bias circuit, the complete modulator consumes only 6 µA from a 1.8V power supply.

4.4.2 Measurement Results



(a) (b)

Figure 4.12: (a) Chip micrograph of the smart humidity sensor; (b) detail showing the humidity sensitive layer on top of the capacitors C_{x1} and C_{x2}.

The proposed smart humidity sensor was designed and fabricated in standard 0.16µm CMOS technology. Figure 4.12 shows a chip photo which also highlights the sensing element, showing the humidity-sensitive layer deposited on top of the two sensor capacitors. The area of the chip excluding pads is 0.25 mm^2.

The measurement was divided into two parts: the characterization of the interface circuit performance, and measurements with the humidity-sensing system. Figure 4.13 shows the measured spectrum of the bitstream, demonstrating the second-order noise shaping characteristic of the modulator. The measurement results show that for a 10.2 ms measurement time, the interface achieves a resolution of 13 bits.

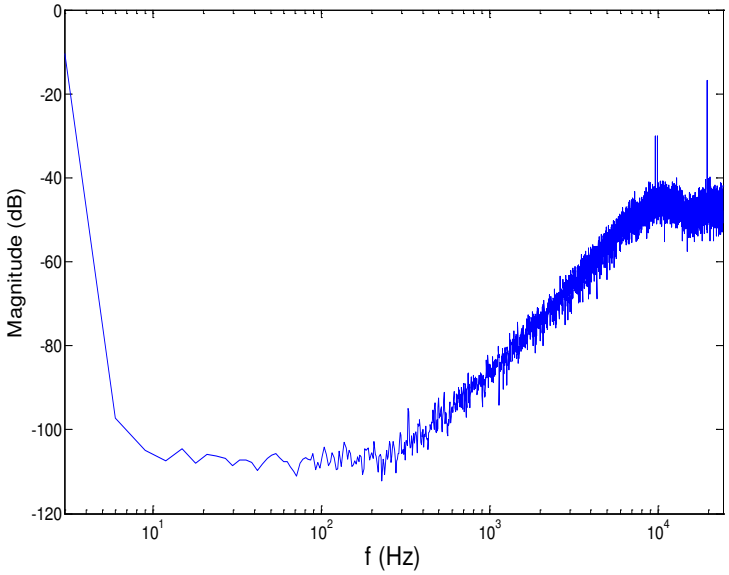


Figure 4.13: Measured spectrum of the bitstream (FFT of 2^{14} points).

To characterize the complete smart humidity sensor, several chips were placed in a climate chamber in which the relative humidity was swept from 20% to 90%. Figure 4.14 shows the measured digital output (the bit-density µ) of one of the chips for different settings of the programmable offset capacitor. Figure 4.15 shows the measured digital output of four chips as a

function of relative humidity at 25ºC and 45ºC. The four chips show similar performance and sensitivity. Due to process variations, the results show offset shifts from chip to chip, which will be calibrated out in the intended RFID sensing application. The cross-sensitivity to temperature will be corrected for by means of a co-integrated temperature sensor. The measured humidity-sensing resolution is 0.1% RH over the range of 20% RH to 90% RH.

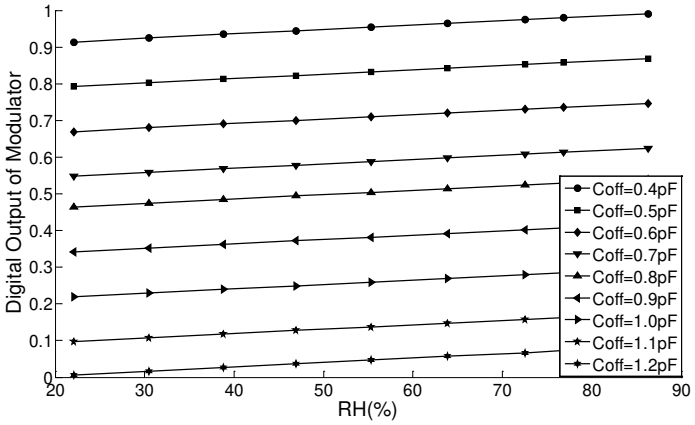


Figure 4.14: Measured digital output as a function of relative humidity for different settings of the offset capacitors.

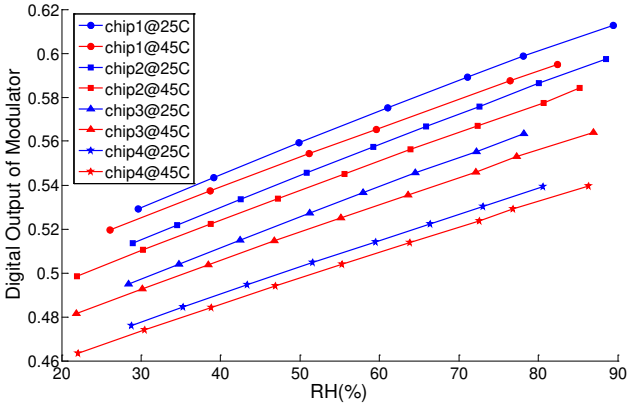


Figure 4.15: Measured digital output of four devices as a function of relative humidity for two operating temperatures.

4.5 Energy-Efficient Capacitve Humidity Sensor II

4.5.1 Circuit Implementation

Compared to the first prototype, in the second prototype, two main improvements have been implemented. As mentioned above, it employs a third-order modulator rather than a second-order modulator in order to achieve better balance between the thermal noise and quantization noise. Moreover, since the power consumption is dominated by that of the modulator's OTAs, this prototype has been implemented using an OTA topology that is more current-efficient than the folded-cascodes used in the first prototype.

The inverter-based SC circuit proposed in [13] outperforms designs based on conventional OTAs since both the PMOS and NMOS transistors of an inverter contribute to the transconductance while sharing the same supply current. As a result, the intrinsic current efficiency doubles compared to a telescopic OTA, and quadruples compared to a folded-cadcode OTA. However, a simple inverter cannot provide sufficient DC gain for our application, which requires at least 70dB in the first integrator. Moreover, an inverter is sensitive to process spread, supply and temperature variations.

To address these issues, we employ current-starved cascoded inverters, as shown in Fig. 4.16. The proposed structure essentially consists of a pair of inverters in which the PMOS and NMOS devices both contribute g_m, and to which cascode transistors have been added to increase the DC-gain beyond the required 70dB. A differential structure is used in which the two cascoded inverters share a tail current source to increase the PVT (Process, Voltage, Temperature) tolerance compared to an implementation in which the tail is tied to the positive supply, as in [13]. This comes at the expense of a small increase in the minimum supply voltage due to the headroom required by the tail-current source. The proposed structure can provide an output swing up to ±220mV. With the proper loop-filter coefficients, the output swing of the integrators in the delta-sigma modulator can easily be kept below this level.

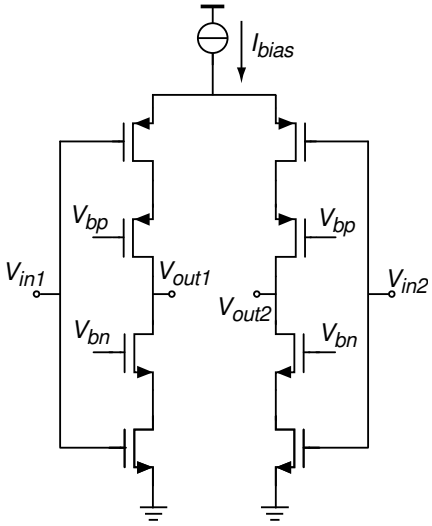


Figure 4.16: Proposed current-starved cascoded inverter.

An auto-zeroing technique is adopted to provide a level-shift between the input common-mode voltage and the gate-source voltage of the NMOS transistors [13]. Figure 4.17 illustrates the operation of the resulting inverter-based SC integrator (showing only half of the differential signal path for simplicity). During clock phase φ_1 (Fig. 4.17a), the inverter is switched to the unity-gain configuration and its input offset voltage, which appears at the inverter's input V_x, is stored on a capacitor C_C. At the same time, the input capacitor C_x is charged to a reference voltage V_{ref} with respect to the signal ground. During clock phase φ_2 (Fig. 4.17b), C_C is kept in series with the inverter's input, while the integration capacitor C_{int} is switched in the feedback path. Due to the negative feedback, V_X is roughly kept at the input offset voltage, and since C_C still holds this offset voltage, node V_G is kept at the signal ground. Thus, this node can be considered a virtual ground, and the charge in C_x will be transferred to C_{int} in a way similar to conventional SC circuits.

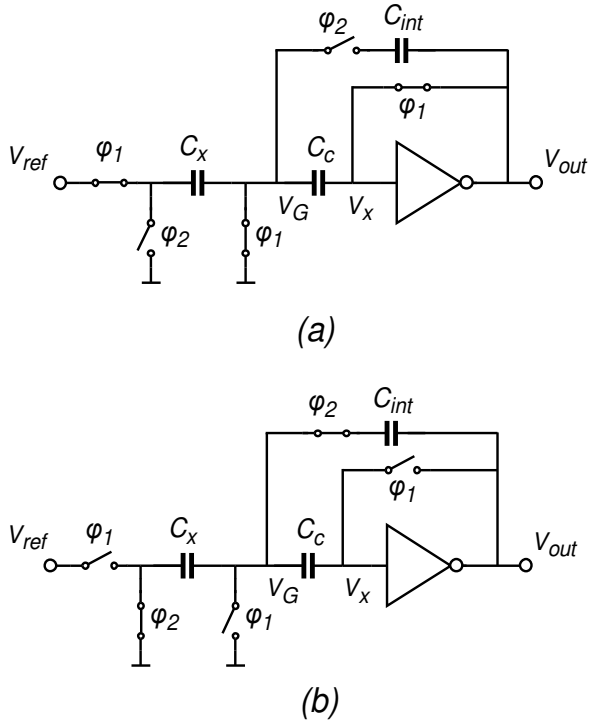


Figure 4.17: Operation of the inverter-based switched-capacitor integrator: (a) auto-zeroing phase φ_1; (b) integration phase φ_2.

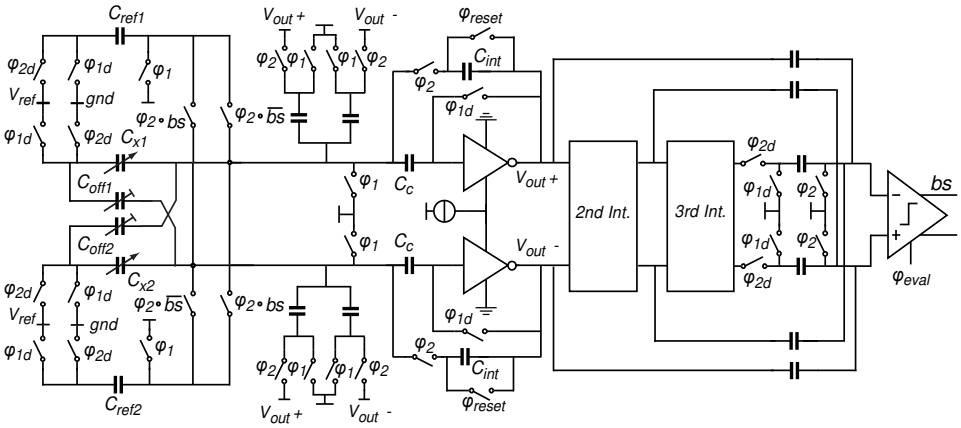


Figure 4.18: Complete circuit diagram of the front-end and delta-sigma modulator.

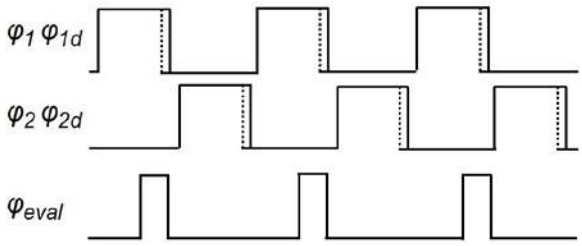


Figure 4.19: Timing diagram.

Figure 4.18 shows the circuit diagram of the proposed capacitive-sensor interface, while Fig. 4.19 shows a timing diagram of the associated clock signals. The interface is driven by a non-overlapping clock, and bottom-plate sampling is used to eliminate signal-dependent charge injection [8].

Details of the second and third integrator have been omitted for simplicity, but they employ the same inverter-based OTA as the first integrator, albeit with a scaled supply current. The current consumption of the first, second and third integrator is 2.2μA, 0.6μA and 0.3μA, respectively. The one-bit quantizer is implemented by a low-power dynamic comparator consisting of a pre-amplifier and a dynamic latch. This arrangement prevents kickback to the output of three integrators. Figure 4.20 shows the diagram of the circuit that generates V_{ref} .

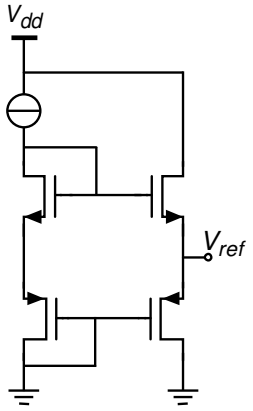


Figure 4.20: Circuit diagram of the reference-voltage generator.

Due to fabrication tolerances on the sensor capacitor, a two-point calibration is required to correct for offset and gain errors. The associated correction based on the calibration results is performed in the digital back-end. In principle, any offset and gain errors of the interface are included in this correction, so that the precise values of the offset and reference capacitors are not critical, as long as they are stable. Errors introduced to the interface that are sensitive to e.g. temperature or the supply voltage, in contrast, will lead to humidity-sensing errors and should therefore be reduced. The dominant source of such errors in this interface is differential charge-injection in the switches of the first integrator, which leads to an error in the charge-balancing process. These errors originate from mismatch between the switches in the two halves of the differential signal path, and are not stable, since the overdrive of these switches depends on temperature and on the supply voltage.

To reduce these errors, the entire system is also auto-zeroed by taking the difference between two conversions of 200 clock cycles each: one with the sensor capacitance connected and one without. In both cases, the charge-injection mismatch leads to an approximately equal error, which thus canceled in the difference. The consequence of this approach is a doubling of the conversion time—a disadvantage that can be mitigated in future designs by adopting a system-level chopping approach instead [14].

4.5.2 Measurement Results

The proposed smart humidity sensor has been designed and fabricated in 0.16μm CMOS technology. Figure 4.21 shows the layout plot along with a chip photograph. The active chip area (excluding pads) is 0.28 mm^2.

The measurements were divided into two parts: characterization of the interface and the overall humidity sensor. Figure 4.22 shows the modulator's output spectrum, demonstrating the third-order noise shaping. For a conversion time of 0.8ms, the interface achieves 12.5-bit resolution with respect to its stable input-capacitance range of ±0.26pF around C_{off}. This corresponds to a humidity-sensing resolution of 0.05% RH. By changing the setting of C_{off}, the interface can cover an input-capacitance range from 0pF

to 1.76pF, corresponding to a total dynamic range of 87.6dB. It consumes only 8.6μA from a 1.2V power supply (excluding the off-chip digital filter), which corresponds to 8.3nJ per measurement. The resolution for a different numbers of cycles N was also measured. Figure 4.23 shows the ENOB versus the measurement cycles. For $N < 200$, the interface is in the quantization-noise-limited region. For $N > 200$, the system is in the thermal-noise-limited region.

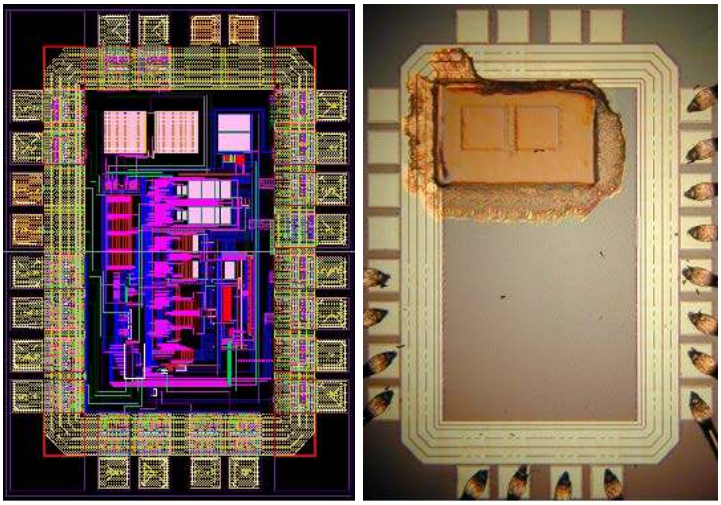


Figure 4.21: Layout plot and chip micrograph of the smart humidity sensor.

The power-supply dependence was also measured: for a ±10% supply-voltage variation, the output changes less than 2.6×10^{-4} with respect to the full scale, which is equivalent to 0.2% RH. When the supply voltage is swept from 1V to 2.5V, the current consumption of the analog part varies less than 8.5%, showing the effectiveness of the current-starved configuration of the inverter-based OTAs.

To characterize the complete smart humidity sensor, 14 chips were placed in a climate chamber in which the relative humidity was swept from 20% to 90% while the temperature was kept at 25ºC. Figure 4.24 shows the resulting digital codes measured of the 14 chips. The 14 chips show similar sensitivity. Due to process variations, the results show offset variations from

chip to chip, which will be calibrated out in the intended RFID application. Figure 4.25 shows the error as a function of relative humidity for the 14 chips after the two-point calibration at 25ºC. The sensor's cross-sensitivity to temperature will be corrected in the intended application by means of a co-integrated temperature sensor.

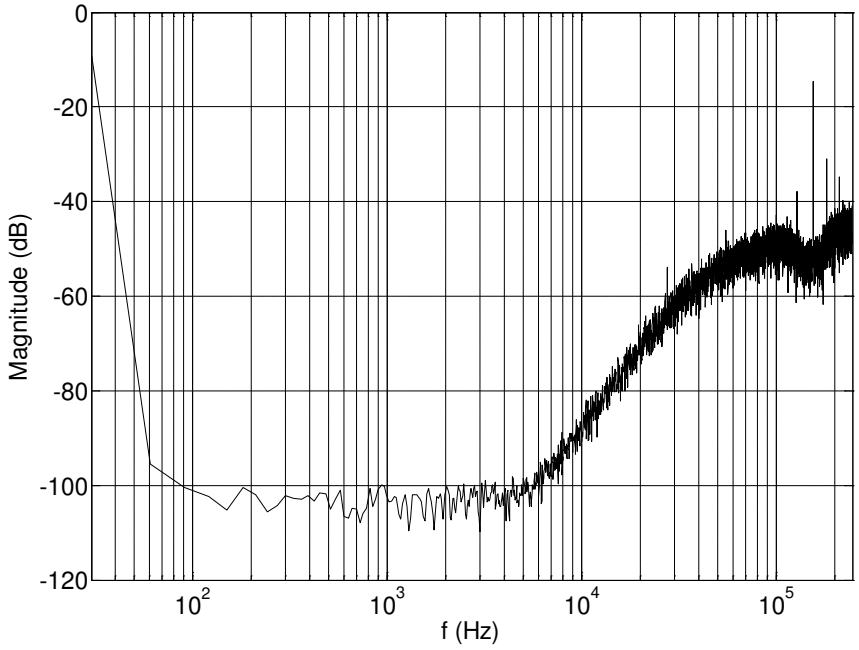


Figure 4.22: Measured spectrum of the bitstream (FFT of 2^{14} points).

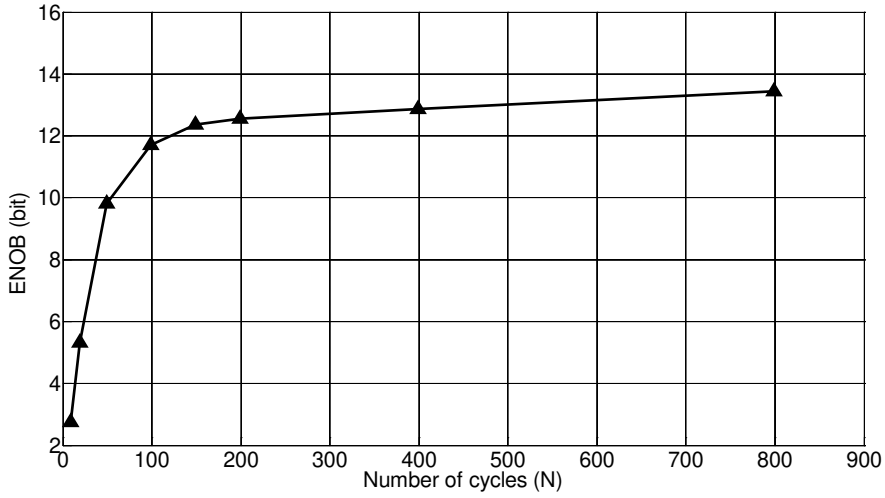


Figure 4.23: Measured cycles vs. ENOB.

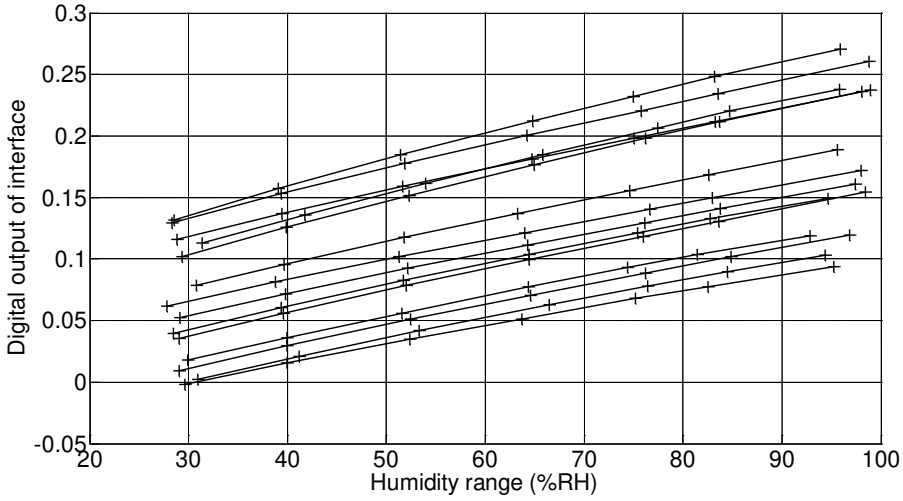


Figure 4.24: Digital output of the 14 chips as a function of relative humidity at 25ºC.

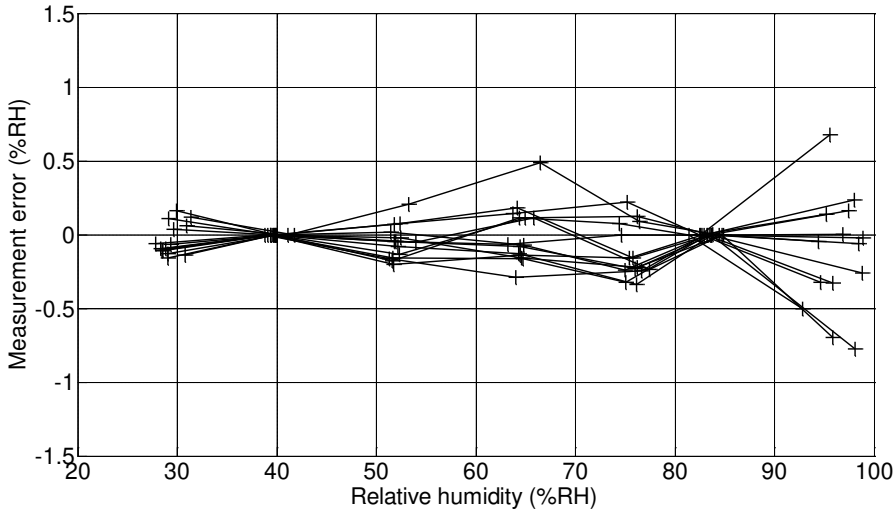


Figure 4.25: Humidity-sensing error at 25°C after a two-point calibration.

4.6 Conclusions

In this chapter, two capacitive-sensor interfaces based on delta-sigma modulation for RFID humidity sensing application have been presented. These interfaces are implemented with 0.16μm CMOS technology. They employ system and circuit techniques to improve energy efficiency. At the system level, the use of higher-order modulators helps to decrease the over-sampling ratio, which decreases the measurement time for a given resolution requirement. At the circuit level, we proposed current-starved-cascode inverters which can be biased more efficiently compared to traditional OTA structures. Measurement results show that the first design achieves a resolution of 13 bits within a measurement time of 10 ms, while drawing 6 μA from a 1.8V supply. The second design achieves a resolution of 12.5 bits within a measurement time of 0.8ms, while drawing only 8.6μA from a 1.2V supply. In combination with the sensor, a humidity-sensing resolution of 0.1 and 0.05% RH in the range from 20% to 90% RH are achieved, respectively.

4.7 References

[1] E. Abad, F. Palacio, M. Nuin, A. González de Zárate, A. Juarros, J.M. Gómez, S. Marco, "RFID smart tag for traceability and cold chain monitoring of foods: Demonstration in an intercontinental fresh fish logistic chain," *Journal of Food Engineering*, vol. 93, pp. 394-399, Aug. 2009.

[2] A. Oprea, N. Bârsan, U. Weimar, J. Courbat, D. Briand, N.F. de Rooij, "Temperature, humidity and gas sensors integrated on plastic foil for low power applications," Sensors and Actuators B, vol. 140, pp. 227-232, June 2009.

[3] D. Cartasegna, A. Cito, F. Conso, A. Donida, M. Grassi, L. Malvasi, G. Rescio, and P. Malcovati, "Smart RFID label for monitoring the preservation conditions of food," in *Circuits and Systems, IEEE International Symposium on*, Taipei, Taiwan, 2009, pp. 1161-1164.

[4] B. Okcan and T. Akin, "A low-power robust humidity sensor in a standard CMOS process," *IEEE Trans. Electron Devices*, vol. 54, no.11, pp. 3071-3078, 2007.

[5] Y. C. Jo, K. N. Kim and T. Y. Nam, "Low power capacitive humidity sensor readout IC with on-chip temperature sensor and full digital output for USN applications," in *Proc. IEEE Sensors Conference*, Christchurch, 2009, pp. 1354-1357.

[6] SHT21 datasheet, SENSIRION. http://www.sensirion.com.

[7] Z. Tan, R. Daamen, A. Humbert, K. Souri, Y. Chae, Y. V. Ponomarev and M. A. P. Pertijs, "A 1.8V 11μW CMOS smart humidity sensor for RFID sensing applications," in *Proc. A-SSCC*, Jeju, Korea, 2011, pp. 105-108.

[8] Z. Tan, Y. Chae, R. Daamen, A. Humbert, Y. V. Ponomarev and M. A. P. Pertijs, "A 1.2V 8.3nJ energy-efficient CMOS humidity sensor for RFID applications," in *Digest of Technical Paper of Symposium on VLSI Circuits*, Honolulu, HI, June 2012, pp. 24-25.

[9] P. Malcovati, A. Haberli, F. Mayer, O. Paul, F. Maloberti and H. Bakes, "Combined air humidity and flow CMOS microsensor with on-chip 15 bit sigma-delta A/D interface," in Digest of Technical Paper of Symposium on VLSI Circuits, Kyoto, Japan, June 1995, pp.45-46.

[10] R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters*. New York: Wiley, 2004.

[11] J. Markus, J. Silva and G. C. Temes, "Theory and applications of incremental delta-sigma converters," *IEEE Transactions on Circuits and Systems-Part I: Fundamental Theory and Applications*, vol. 51, no. 4, pp. 678-690, Apr. 2004.

[12] J. Silva, U. Moon, J. Steensgaard, and G. Temes, "Wideband low distortion delta-sigma ADC topology," Electronics Letters, vol. 37, no. 12, pp. 737-738, June 2001.

[13] Y. Chae and G. Han, "Low voltage, low power, inverter-based switched-capacitor delta-sigma modulator," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 2, pp. 458-472, Feb. 2009.

[14] M. A. P. Pertijs, K. A. A. Makinwa and J. H. Huijsing, "A CMOS temperature sensor with a 3σ inaccuracy of ±0.1°C from -55 ºC to 125 ºC," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 12, pp. 2805-2815, Dec. 2005.

Chapter 5

Conclusions

In this thesis, the design of energy-efficient capacitive-sensor interfaces has been presented. In Chapter 2, system and circuit techniques that can improve the energy efficiency of capacitive-sensor interfaces have been addressed. Equipped with these techniques, one design based on period modulation (Chapter 3) and two designs based on delta-sigma modulation (Chapter 4) have been implemented. This final chapter will first present a benchmark of all three prototypes. Then, the main findings and original contributions of this thesis will be summarized.

5.1 Benchmark

5.1.1 Capacitive-Sensor Interfaces

In Table II, the performance of the capacitive-sensor interfaces presented in this thesis are summarized and compared to the state-of-the-art capacitive-sensor interfaces published in the last decade [1]. The conversion principles are: successive approximation [2,3,4], period modulation [5,6], pulse-width modulation [7,8,9], and delta-sigma modulation [10,11,12,13,14,15,16]. The effective number of bits (ENOB) and figure-of-merit (FoM) reported in the table are defined by Eqs. (1-1) and (1-2).

Figure 5.1 plots the energy per measurement as a function of the ENOB for the designs listed in Table II [1]. For reference purposes, a line corresponding to a FoM of 1 pJ/step is also shown. This figure shows that the capacitive-sensor interfaces presented in this thesis are best-in-class in terms of energy efficiency compared to prior interfaces based on period-modulation and delta-sigma modulation. This confirms the effectiveness of the techniques presented in this thesis. Overall, the design presented in Section 4.5 achieves the second-best FoM in the survey. The design with the best FoM reported to date is a SAR CDC with a much lower resolution than the designs presented in this thesis.

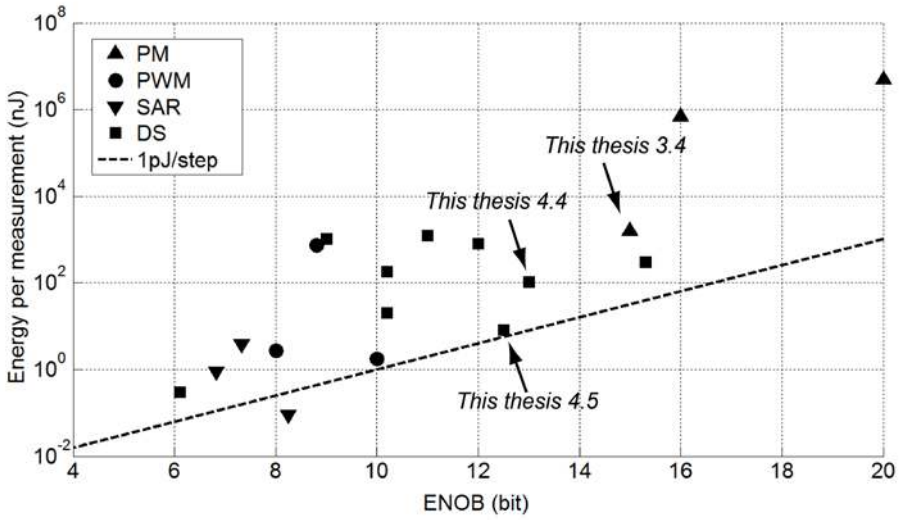


Figure 5.1. Survey of the energy consumption of capacitive sensor interfaces and benchmark of the interfaces proposed in this thesis.

TABLE II. PERFORMANCE SUMMARY OF THE CAPACITANCE-TO-DIGITAL CONVERTERS AND COMPARISON WITH THE STATE-OF-THE-ART.

	Type	Tech.	Supply voltage	Current cons.	Meas. time	Capacitance range	ENOB	FoM
[2]	SAR	0.8μm	2.8V	1.2μA	1.25ms	N.A.	7.3bit	23.5pJ/step
[3]	SAR	0.18μm	1.4V	169μA	3.8μs	3pF	6.8bit	7.9pJ/step
[4]	SAR	0.18μm	1.4V	6.3μA	10μs	N.A.	8.3bit	0.29pJ/step
[5]	PM	0.7μm	5V	1mA	1s	5.8pF	20bit	4.7nJ/step
[6]	PM	0.7μm	5V	1.4mA	100ms	4.7pF	16bit	10.7nJ/step
[7]	PWM	0.35μm	3V	5mA	50μs	0.8pF~1.2pF	8.8bit	1.7nJ/step
[8]	PWM	0.32μm	3V	28μA	33μs	0.5pF~0.76pF	8bit	10pJ/step
[9]	PWM	0.18μm	1V	60μA	30μs	N.A.	10bit	1.8pJ/step
[10]	ΔΣ	0.5μm	3V	3.3μA	100ms	2.1pF~2.9pF	9bit	2nJ/step
[11]	ΔΣ	0.25μm	1V	20μA	40ms	1.5pF~2.5pF	12bit	195pJ/step
[12]	ΔΣ	0.35μm	1.8V	460μA	0.025ms	N.A.	10bit	17pJ/step
[13]	ΔΣ	0.35μm	3.3V	436μA	0.128ms	-0.5pF~0.5pF	11bit	27.6pJ/step
[14]	ΔΣ	N.A	1.8V	70μA	10ms	0pF~4pF	11bit	610pJ/step
[15]	ΔΣ	0.35μm	3.3V	4.5mA	0.02ms	8.4pF~11.6pF	15bit	7.4pJ/step
[16]	ΔΣ	0.13μm	0.3V	0.9μA	1ms	6pF~6.3pF	6.1bit	3.9pJ/step
Section 3.4	**PM**	**0.35μm**	**3.3V**	**64μA**	**7.6ms**	**6.8pF**	**15bit**	**49pJ/step**
Section 4.4	**ΔΣ**	**0.16μm**	**1.8V**	**5.85μA**	**10.2ms**	**0.4pF~1.2pF**	**13bit**	**13pF/step**
Section 4.5	**ΔΣ**	**0.16μm**	**1.2V**	**8.6μA**	**0.8ms**	**0.5pF~1.0pF**	**12.5bit**	**1.4pJ/step**

5.1.2 Humidity Sensors

Table III compares the performance of the smart humidity sensor with the prior-art sensors [17,18,19]. The sensors presented in this thesis, admittedly,

integrate less functionality than some of the prior art (which offer e.g. temperature compensation). However, they show a significant improvement in energy efficiency.

TABLE III. SUMMARY OF THE PERFORMANCE OF THE HUMIDITY SENSORS IN COMPARISON WITH THE PRIOR-ART.

	Supply voltage	Power	Meas. time	Meas. range (RH)	Resolution	Area	Energy /meas.
[17][1]	5V	1.38mW	N.A.	20%~90%	N.A.	N.A.	N.A.
[18]	N.A.	150μW	1s	20%~80%	0.02%RH	N.A.	150μJ
[19][2]	3V	3.2μW	1s	0%~100%	0.7%RH	N.A.	3.2μJ
Section 4.4	**1.8V**	**10.5μW**	**10.2ms**	**20%~90%**	**0.1%RH**	**0.25mm^2**	**107nJ**
Section 4.5	**1.2V**	**10.3μW**	**0.8ms**	**20%~90%**	**0.05%RH**	**0.28mm^2**	**8.3nJ**

1 Only voltage output; no analog-to-digital converter included.

2 Commercial product which has temperature sensor on-board.

5.2 Main Findings

The most important main findings presented in this thesis are:

- The operating principle of capacitive-sensor interfaces shows a strong similarity to that of ADCs. However, their energy efficiency is at least an order of magnitude less (Chapters 1 and 2).

- The use of system techniques such as auto-calibration, baseline compensation, and circuits such as inverter-based OTAs can yield a significant improvement in the energy efficiency of capacitive-sensor interfaces (Chapter 2).

- In sensor systems, auto-calibration and negative feedback techniques are applied to reduce the systematic errors. In this thesis it is shown for period-modulated interfaces that these techniques can also significantly improve the energy efficiency of analog building blocks (Chapter 3).

- Incremental delta-sigma modulators are very useful in the design of energy-efficient capacitive-sensor interfaces. Especially the use of higher-order modulators can help to improve energy efficiency by providing a better balance between quantization noise and thermal noise (Chapter 4).

- It is possible to design a humidity sensor which only consumes 8.3nJ per measurement (Chapter 4).

5.3 Original Contributions

The most important original contributions presented in this thesis are:

Chapter 2

1. Summary of system-level techniques that can be used to improve the energy efficiency of capacitive-sensor interfaces, such as: charge balancing, baseline calibration, auto-calibration and system-level chopping.
2. Analysis of inverter-based switch-capacitor circuits to improve the energy efficiency of capacitive-sensor interfaces.

Chapter 3

1. Analysis of the stability of negative feedback loops used in period-modulation-based capacitive-sensor interfaces and analysis of the resulting trade-off between current consumption of the interface and its ability to handle parasitic capacitors.
2. Realization of a state-of-the-art energy-efficient capacitive-sensor interface based on period modulation.

Chapter 4

1. Realization of a capacitive-sensor interface based on current-starved cascoded inverters for RFID humidity sensing.

2. Realization of two state-of-the-art energy-efficient humidity sensors.

5.4 References

[1] M. A. P. Pertijs and Z. Tan, "Energy-efficient capacitive sensor interfaces," in *Analog Circuit Design*, A. Baschirotto, A. H. M. van Roermund and M. Steyaert, Eds. New York: Springer, 2012. pp. 129-147.

[2] B. Bechen, D. Weiler, T. v. d. Boom, and B. J. Hosticka, "A 10 bit very low-power CMOS SAR-ADC for capacitive micro-mechanical pressure measurement in implants," *Adv. Radio Sci.*, no. 4, 2006, pp. 243-246.

[3] K. Tanaka et al., "A 0.026mm^2 capacitance-to-digital converter for biotelemetry applications using a charge redistribution technique," in *Proc. IEEE Asian Solid-State Circuits Conference (A-SSCC)*, Nov. 2007, pp. 244-247.

[4] T. M. Vo et al., "A 10-bit, 290fJ/conv. steps, 0.13mm^2, zero-static power, self-timed capacitance to digital converter," in *Proc. SSDM*, Oct. 2009.

[5] A. Heidary and G. C. M. Meijer, "Features and design constraints for an optimized SC front-end circuit for capacitive sensors with a wide dynamic range," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 7, July 2008, pp. 1609-1616.

[6] A. Heidary, S. Heidary Shalmany and G. C. M. Meijer, "A flexible low-power high-resolution integrated interface for capacitive sensors," in *Proc. Int. Symp. on Industrial Electronics (ISIE)*, July 2010, pp. 3347-3350.

[7] P. Bruschi, N. Nizza and M. Piotto, "A current-mode, dual slope, integrated capacitance-to-pulse duration converter," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 9, Sept. 2007, pp. 1884-1891.

[8] P. Bruschi, N. Nizza and M. Dei, “A low-power capacitance to pulse width converter for MEMS interfacing,” in *Proc. European Solid-State Circuits Conference (ESSCIRC)*, Sept. 2008, pp. 446-449.

[9] J. H.-L. Lu et al., “A low-power, wide-dynamic-range semi-digital universal sensor readout circuit using pulsewidth modulation,” *IEEE Sensors Journal*, vol. 11, no. 5, pp. 1134-1144, May 2011.

[10] M. Paavola et al., “A micropower ΔΣ-based interface ASIC for a capacitive 3-axis micro-accelerometer,” *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp. 3193-3210, Nov. 2009.

[11] W. Bracke, R. Puers and C. Van Hoof, *Ultra Low Power Capacitive Sensor Interfaces*. Dordrecht, the Netherlands: Springer, 2007.

[12] S. A. Jawed et al., “A 828μW 1.8V 80dB dynamic range readout interface for a MEMS capacitive microphone,” in *Proc. European Solid-State Circuits Conference (ESSCIRC)*, Sept. 2008, pp. 442-445.

[13] D.-Y. Shin, H. Lee and and S. Kim, “A delta-sigma interface circuit for capacitive sensors with an automatically calibrated zero point,” *IEEE Trans. Circuits and Systems II*, vol. 58, no. 2, pp. 90-94, Feb. 2011.

[14] AD7156 datasheet, Analog Devices [Online]. http://www.analog.com.

[15] S. Xia, K. A. A. Makinwa and S. Nihtianov, “A capacitance-to-digital converter for displacement sensing with 17b resolution and 20μs conversion time,” in *International Solid-State Circuits Conference Dig. Tech. Papers*, 2012, pp. 197-198.

[16] H. Danneels, K. Coddens and G. Gielen, “A fully-digital, 0.3V, 270nW capacitive sensor interface without external references,” in *Proc. European Solid-State Circuits Conference (ESSCIRC)*, Sept. 2011, pp. 287-290.

[17] B. Okcan and T. Akin, “A low-power robust humidity sensor in a standard CMOS process,” *IEEE Trans. Electron Devices*, vol. 54, no.11, pp. 3071-3078, 2007.

[18] Y. C. Jo, K. N. Kim and T. Y. Nam, “Low power capacitive humidity sensor readout IC with on-chip temperature sensor and full digital output for USN applications,” in *Proc. IEEE Sensors Conference*, Christchurch, 2009, pp. 1354-1357.

[19] SHT21 datasheet, SENSIRION. http://www.sensirion.com.

Summary

This thesis describes the theory, design and realization of energy-efficient capacitive-sensor interfaces that are dedicated to low-power and energy-constrained applications, such as sensors employing RFID technology for wireless readout, and wireless sensors for environmental monitoring. The goal of this work is to explore methods at both the system level and the circuit level to reduce energy consumption without scarifying system performance. Three prototypes are presented to demonstrate the effectiveness of these techniques. The final prototypes, based on period-modulation and delta-sigma modulation, achieve best-in-class energy efficiency.

Chapter 1

Chapter 1 presents an introduction to this thesis and gives a motivation for the thesis topic. The basics of capacitive sensors and their interface circuits are described. Capacitive sensors are widely used both in industrial and consumer applications. They usually consist of a sensing element and an interface circuit that converts the sensing element's capacitance into the digital domain. The energy consumption of the interface circuit typically dominates the overall energy consumption of the capacitive sensor. Hence, for low-power, energy-constrained applications, an energy-efficient capacitive-sensor interface is an essential building block.

Chapter 2

Chapter 2 presents system-level techniques that can be applied to design energy-efficient capacitive-sensor interfaces. Auto-calibration can be used to reduce the effects of systematic errors and low-frequency noise. Although this technique comes at the cost of extra energy consumed by two extra conversions: an offset capacitance and a reference capacitance, in return it strongly relaxes the offset- and gain-accuracy requirements of the capacitive-sensor interface. In some cases this can be translated into a significant reduction in energy consumption. The baseline-compensation technique can cancel the effect of unchanged baseline capacitance in order to use the dynamic range of the interface more efficiently, which in some cases may also save energy. The system-level chopping technique can separate the sensor signal from undesired interfering signals by modulating the sensor signal to a higher frequency, so that it can be processed to eliminate the 1/*f* noise, offset and supply interference. This approach can be more energy-efficient than some other techniques such as auto-zeroing, which usually requires more measurement time.

Several circuit-design techniques for low-power capacitive-sensor interfaces are also presented in this chapter. Since many capacitive-sensor interfaces are implemented using switched-capacitor (SC) circuits, an operational transconductance amplifier (OTA) is used to transfer charge from the sensor capacitor to an integration capacitor for further processing. An analysis of the energy consumption of such a circuit is presented. An analysis of the settling behavior of a switch-capacitor integrator reveals the minimum current consumption of the OTA used in the integrator given the integrator's loading conditions, the required resolution and the clock period. Several OTA structures and their energy efficiency are reviewed, showing that structures with fewer current legs have better energy efficiency. Finally, SC circuits are presented which employ inverter-based OTAs. The inverter-based OTA outperforms conventional OTAs since both the PMOS and NMOS transistor of an inverter contribute transconductance while sharing the same supply current.

Chapter 3

An energy-efficient capacitive-sensor interface based on period modulation is presented in Chapter 3. This interface converts the sensor capacitance into a time period, which is then converted into a digital value using a counter. The interface circuit is implemented with compact, energy-efficient building blocks. Auto-calibration is employed to achieve a well-defined transfer function in spite of the non-idealities of these building blocks. This enables the use of a simple telescopic OTA in the integrator and a slow, low-power comparator. The limited output swing of the OTA is accommodated using negative feedback loops. It is shown that the energy consumption of the resulting interface is affected by the presence of parasitic capacitors in the sensor element and its wiring. The associated design trade-offs are presented. The interface circuit has been realized in 0.35μm CMOS technology. Measurement results show that for a measurement time of 7.6ms the resolution amounts to 15 bits. This yields a figure-or-merit of 49pJ/step which is a significant improvement in energy efficiency as compared with previous interfaces based on period modulation. The linearity amounts to 12 bits.

Chapter 4

In Chapter 4, two capacitive-sensor interfaces based on delta-sigma modulation are presented. These interfaces are tailored for a humidity-sensing application. They first convert the sensor capacitance into a bitstream which is then converted to a digital measurement result by a decimation filter. They employ both system and circuit techniques to improve energy efficiency compared with the prior art. At the system level, the use of a higher-order modulator helps to decrease the over-sampling ratio, so as to prevent the design from being quantization-noise limited and to reduce the energy consumption. At the circuit level, current-starved cascoded-inverters are used instead of traditional OTA structures to reduce the supply current. The two prototype interfaces have been implemented in 0.16μm CMOS technology. Measurement results show that the first design achieves a resolution of 13 bits within a measurement time of 10ms, while drawing 5.9μA from a 1.8V supply. The second design achieves a resolution

of 12.5 bits within a measurement time of 0.8ms, while drawing only 8.6μA from a 1.2V supply. In combination with the sensor, a humidity-sensing resolution of 0.1% and 0.05% RH (relative humidity) in the range from 20% to 90% RH are achieved, respectively.

Chapter 5

In this final chapter, the presented capacitive-sensor interfaces are compared to a survey of capacitive-sensor interface reported in the literature. These interfaces are based on successive approximation, period modulation, pulse-width modulation and delta-sigma modulation. This comparison confirms the effectiveness of the techniques presented in this thesis. Overall, the design presented in Section 4.5 achieves the second-best FoM in the survey. The design with the best FoM reported to date is a SAR CDC with a much lower resolution than the designs presented in this thesis. The humidity sensors proposed in this thesis are also compared with previous work. Although the sensors presented in this thesis, admittedly, integrate less functionality than some of the prior art (e.g. temperature compensation), they represent a significant improvement in energy efficiency.

Samenvatting

Dit proefschrift beschrijft de theorie, het ontwerp en de realisatie van energiezuinige interfaces voor capacitieve sensoren, die speciaal zijn ontworpen voor toepassingen waarbij het energiegebruik een belangrijke beperking vormt. Voorbeelden van dergelijke toepassingen zijn sensoren die van vermogen worden voorzien en worden uitgelezen met RFID systemen, en draadloze sensoren voor het monitoren van de omgeving.

Het doel van dit werk is om te verkennen welke ontwerptechnieken op systeem- en circuitniveau het energieverbruik kunnen beperken zonder dat de kwaliteit van het systeem hieronder lijdt. Dit onderzoek heeft geleid tot een drietal prototypen die de doelmatigheid van de gepresenteerde technieken laten zien. De laatste prototypen, die gebaseerd zijn op het gebruik van respectievelijk periodemodulatie en delta-sigmamodulatie, laten een energie-efficiëntie zien welke het beste is in hun klasse.

Hoofdstuk 1

Hoofdstuk 1 presenteert een introductie van het proefschrift en beschrijft de motivatie voor het onderzoeksproject. De basisprincipes van capacitieve sensoren en hun interfaces worden hierbij beschreven. Capacitieve sensoren worden veel gebruikt in zowel industriële als consumententoepassingen. Gewoonlijk bestaan ze uit een sensorelement en een interfaceschakeling die het signaal van het sensorelement omzet naar het digitale domein. Meestal zal het energiegebruik van de interfaceschakeling veel groter zijn dan dat

van het sensorelement. Daarom zal bij het ontwerpen van sensoren voor energiearme toepassingen de nadruk komen te liggen op de energie-efficiëntie van de interface.

Hoofdstuk 2

Hoofdstuk 2 presenteert technieken die op *systeemniveau* kunnen worden gebruikt voor het ontwerp van energie-efficiëntie interfaces voor capacitieve sensoren. ***Autocalibratie*** wordt gebruikt voor het verminderen van systematische fouten en laagfrequent ruis. Ofschoon voor het gebruik van deze techniek een beetje extra energie nodig is om twee extra signaalomzettingen van een offset en een referentiecapaciteit te kunnen doen, leidt dit gebruik tot sterk verminderde eisen die gesteld worden aan offset en versterking. In sommige gevallen levert dit een aanzienlijke reductie op van het totale energieverbruik. De techniek van ***basislijncompensatie*** compenseert het effect van het ongebruikte deel van het capaciteitsbereik, waardoor het dynamische bereik van de sensor beter benut kan worden, hetgeen soms energiebesparing oplevert. De techniek van ***chopping op systeemniveau*** kan het sensorsignaal scheiden van ongewenste storingen. Bij deze techniek wordt het laagfrequente sensorsignaal gemoduleerd naar hogere frequenties, waardoor het effect van storende laagfrequente signalen, zoals 1/f ruis, offset en voedingsspanningsvariaties, wordt onderdrukt. Deze techniek kan aanzienlijk meer energiebesparing opleveren dan sommige alternatieve technieken, zoals ***auto-zeroing***, omdat deze laatste techniek veel meer meettijd in beslag neeemt.

In dit hoofdstuk worden ook verschillende technieken voor het ontwerpen van energiezuinige interface*schakelingen* voor capacitieve sensoren besproken. Omdat veel van de interfaceschakelingen worden uitgevoerd als ***switched-capacitor*** (SC) schakeling, wordt een transconductantieversterker (OTA) gebruikt om de lading van de sensorcapaciteit voor verdere signaalverwerking over te dragen naar een integratiecapaciteit. Het energiegebruik van zo'n schakeling wordt besproken. Analyse van het "settling" gedrag van een SC integrator laat zien wat het minimale stroomverbruik is van de OTA voor een gegeven waarden van belasting, resolutie en klokperiode. Verschillende OTA structuren worden hierbij

beschouwd, hetgeen laat zien dat structuren met weinig vertakkingen een betere energie-efficiëntie opleveren. Tot slot worden SC schakelingen besproken die gebruik maken van *inverter-gebaseerde* OTAs. Deze OTAs kunnen volstaan met een veel lager stroomverbruik dan conventionele OTAs. Dit komt omdat zowel de PMOS als de NMOS transistoren bijdragen tot de transconductantie, terwijl ze gebruik maken van dezelfde voedingsstroom.

Hoofdstuk 3

Hoofdstuk 2 presenteert een energie-efficiënte interface voor capacitieve sensoren die gebaseerd is op het gebruik van periodemodulatie. Deze interface converteert de sensorcapaciteit naar een periodetijd, welke vervolgens met een teller wordt geconverteerd naar een digitale waarde. De interfaceschakeling is uitgevoerd met compacte energiezuinige bouwstenen. Autocalibratie wordt toegepast om een goed gedefinieerde overdrachtsfunctie te verkrijgen die immuun is voor niet-idealiteiten van de bouwstenen. Dit maakt het mogelijk om voor de integrator een eenvoudige OTA te gebruiken en een langzame laagvermogen comparator. De uitgangsspanning van de OTA wordt beperkt door een tegengekoppelde schakeling. Er wordt getoond dat het energieverbruik van deze interface beïnvloed wordt door de aanwezige parasitaire capaciteiten van het sensor element en zijn bedrading. De wisselwerking tussen de ontwerpparameters wordt besproken. De interface schakeling is vervaardigd in 0.35μm CMOS technologie. Meetresultaten laten zien dat bij een meettijd van 7.6 ms de resolutie 15 bit bedraagt. Dit levert een kwaliteitsgetal op van 49 pJ/stap, hetgeen erg goed is in vergelijking met de energie-efficiëntie van andere interfaces die zijn gebaseerd op het gebruik van periodemodulatie. De lineariteit van de interface bedraagt 12 bit.

Hoofdstuk 4

In hoofdstuk 4 worden twee interfaces die gebaseerd zijn op delta-sigma modulatie besproken. Deze interfaces zijn speciaal ontworpen voor gebruik in vochtigheidssensoren. Zij zetten eerst de waarde van de sensorcapaciteit om in een *bitstream*, welke vervolgens wordt geconverteerd naar een digitale waarde. Er wordt hierbij gebruik gemaakt van systeem- en

schakelingtechnieken die in vergelijking met vroegere versies energiebesparing opleveren. Op systeemniveau helpt het gebruik van hogere-orde modulatie om de *oversampling* verhouding te reduceren teneinde te voorkomen dat de interface resolutie beperkt wordt door kwantisatieruis en het energiegebruik te verminderen. Op schakelingniveau worden "*current-starved cascoded-inverters*" gebruikt in plaats van de traditionele OTAs, hetgeen een besparing van voedingsstroom oplevert. De twee prototypen zijn uitgevoerd in 0.16μm CMOS technologie. Metingen laten zien dat het eerste ontwerp een resolutie heeft van 13 bit bij een meettijd van 10 ms. Het stroomverbruik bedraagt 6 μA bij een voedingsspanning van 1.8V. Het tweede ontwerp heeft een resolutie van 12.5 bit bij een meettijd van 0.8 ms. Het stroomverbruik bedraagt 8.6 μA bij een voedingsspanning van 1.2 V. In combinatie met de sensor bedraagt de resolutie respectievelijk 0.1% en 0.05% RH (relative humidity) in het bereik van 20% to 90% RH.

Hoofdstuk 5

In dit laatste hoofdstuk worden de nieuwe interfaces voor capacitieve sensoren vergeleken met die welke in de literatuur worden beschreven. Deze interfaces zijn gebaseerd op een grote verscheidenheid aan modulatieprincipes, zoals successive approximation, periodemodulatie, pulsbreedte-modulatie en delta-sigma modulatie. De vergelijking bevestigt de doeltreffendheid van de technieken die in dit proefschrift worden voorgesteld. Van alle ontwerpen vertoont het ontwerp gepresenteerd in paragraaf 4.5 het op-een-na beste kwaliteitsgetal voor energieverbruik. Het ontwerp met het beste kwaliteitsgetal betreft een SAR CDC welke evenwel een veel lagere resolutie heeft dan de ontwerpen die in dit proefschrift worden voorgesteld. Ook de vochtigheidssensoren die in dit proefschrift zijn voorgesteld worden vergeleken met ontwerpen die bekend zijn uit de literatuur. Hoewel de sensoren die worden voorgesteld worden in dit proefschrift minder functionaliteit bezitten dan de andere sensoren (er ontbreekt bijvoorbeeld temperatuurcompensatie), vertonen zij duidelijk een grotere verbetering met betrekking tot energie-efficiëntie.

List of Publications

Book Chapters

G. C. M. Meijer, X. Li, B. Iliev, G. Pop, Z. Chang, S. Nihtianov, **Z. Tan** and M. A. P. Pertijs, "Dedicated impedance-sensor systems," in *Smart Sensor Systems*, G. C. M. Meijer and M. A. P. Pertijs, Eds. Chichester, UK: Wiley, 2013.

M. A. P. Pertijs and **Z. Tan**, "Energy-efficient capacitive sensor interfaces," in *Analog Circuit Design*, A. Baschirotto, A. H. M. van Roermund and M. Steyaert, Eds. New York: Springer, 2012.

Journal Papers

Z. Tan, Y. Chae, R. Daamen, A. Humbert, Y. V. Ponomarev and M. A. P. Pertijs, "A 1.2V 8.3nJ CMOS humidity sensor for RFID applications." Submitted to *IEEE Journal of Solid-State Circuits (JSSC)*.

Z. Tan, S. Heidary Shalmany, G. C. M. Meijer and M. A. P. Pertijs, "An energy-efficient 15-bit capacitive-sensor interface based on period modulation," *IEEE Journal of Solid-State Circuits (JSSC)*, pp. 1703-1711, July 2012.

X. Zhang, D. Yu, S. Sheng and **Z. Tan**, "Behavioral simulation method and an optimized design of sigma-delta ADC," *ACTA SCIENTIARUM NATURALIUM UNIVERSITATIS PEKINENSIS*, pp. 209-214, March 2009.

Conference Papers

A. Humbert, B. Tuerlings, R. J. O. M. Hoofman, **Z. Tan**, D. Gravesteijn, M. A. P. Pertijs, C. W. M Bastiaansen, and D. Soccol, "Low power CMOS integrated CO_2 sensor in the percentage range," in *The 17th International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS)*, Barcelona, Spain, June 2013.

Z. Tan, R. Daamen, A. Humbert, Y. V. Ponomarev, Y. Chae, G. C. M. Meijer and M. A. P. Pertijs, "Ultra-low energy CMOS humidity sensor for RFID applications," in *Proc. Sense of Contact 15*, Soesterberg, the Netherlands, Apr. 2013. (***Best Poster Award***)

C. Chen, **Z. Tan** and M. A. P. Pertijs, "A 1V 14b self-timed zero-crossing-based incremental ΔΣ ADC," in *Digest of International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, Feb. 2013. pp. 274-275.

Z. Tan, Y. Chae, R. Daamen, A. Humbert, Y. V. Ponomarev and M. A. P. Pertijs, "A 1.2V 8.3nJ energy-efficient CMOS humidity sensor for RFID applications," in *Digest of Symposium on VLSI Circuit (VLSIC)*, Honolulu, HI, June 2012, pp. 24-25.

M. A. P. Pertijs and **Z. Tan**, "Energy-efficient capacitive sensor interfaces," in *Proc. 21st Workshop on Advances in Analog Circuit Design (AACD)*, Valkenburg, the Netherlands, March 2012.

Z. Tan, R. Daamen, A. Humbert, K. Souri, Y. Chae, Y. V. Ponomarev and M. A. P. Pertijs, "A 1.8V 11μW CMOS smart humidity sensor for RFID sensing applications," in *Proc. IEEE Asian Solid-State Circuits Conference (A-SSCC)*, Jeju, Korea, Nov. 2011, pp. 105-108.

Z. Tan, M. A. P. Pertijs and G. C. M. Meijer, "An energy-efficient 15-bit capacitive sensor interface," in *Proc. European Solid-State Circuits Conference (ESSCIRC)*, Helsinki, Finland, Sept. 2011, pp. 283-286.

Z. Tan, M. A. P. Pertijs and G. C. M. Meijer, “Energy-efficient capacitive-sensor interface with high dynamic range,” in *Proc. Sense of Contact 12*, Zeist, the Netherlands, Apr. 2010.

Z. Tan and G. C. M. Meijer, “A low-power universal capacitive-sensor interface for autonomous sensor applications,” in *Proc. Sense of Contact 11*, Zeist, the Netherlands, Apr. 2009.

Acknowledgements

Now that I have arrived at this page, I know I am approaching the last part of my 1699 days of studying in the Netherlands. It was around 19:00 on October 16th 2008 that I landed at Schiphol Amsterdam airport. It was at that moment that I started the fantastic journey of studying in one of the world's lowest countries. Luckily, as a Ph.D. student I was never alone during this journey. I would like to take this opportunity to express my appreciation to everyone who helped and accompanied me in this journey. This thesis would not be finished without any one of you.

I first want to thank my promotor Prof. Gerard Meijer. Thank you for giving me the opportunity to come to the Netherlands and allowing me to work on such an exciting topic. The offer letter you sent to me on January 31st 2008 changed my life dramatically. I still remember at the beginning of my studies worshipping the red journal and anxiously asking you how and when I could get one. You surprisingly told me that Ph.D. studies are not about the red journal but about creating knowledge! As my promotor, you guided me through my entire Ph.D. studies. You taught me about life-work balance after seeing my "crazy" working style. I sincerely appreciate you for all the support, encouragement, patience and trust in me throughout these years.

I want to thank my co-promotor and supervisor Dr. Michiel Pertijs. As my supervisor, I benefited a lot from your enthusiasm, optimism and all the things I learned from you. Sometimes I was shocked by your ingenious thought process and ideas during our white board discussion. From that time, I started keeping a camera in my office to take pictures of the white board and capture the moment of our newly generated ideas. I still remember you

helping me “trim” my power point slides even one hour before my first international conference presentation at Helsinki. I was so fortunate to have had such a nice and “sharp-minded” supervisor along with me for my research.

I want to thank Prof. Kofi Makinwa for being so supportive and helpful over past years. You calmed me down many times when I encountered problems both in work and life, you also gave me really smart and valuable advice from which I benefited a lot. Your personal experience has already become a legend in my mind and it will continue to inspire me in the future. More importantly, meeting each other every weekend for our “tennis event” helped me keep my weight well under the 90kg threshold. I am so lucky to have had you as my teacher, mentor and tennis partner during the past several years.

I also want to thank Dr. Youngcheol Chae, who opened my mind to delta-sigma ADC design. I cannot remember how many times I brought these beginner level questions to you and you were always patient and answered them in a really clear way. You taught me how to use “inverter” design delta-sigma converters, which was really interesting to me. When my inverter-based design produced bit-stream for the first time, you were the only witness of that significant moment during my Ph.D. study. Thank you for all your help during your time at Delft. I am so happy to have had such a data-converter expert and good teacher so nearby when I started studying the delta-sigma ADC.

I want to express my thanks to Prof. Johan Huijsing. We got to know each other not from circuit discussion but from our Bible study sessions. You led me to reading some parts of Bible that I otherwise would never have discovered. You taught me “how to serve others”, which I think will take more time for me to understand fully. As one of the most renowned figures in the analog design business, I want to thank you for spending your time and sharing your valuable experience with me.

I would like to thank three Master’s students who did/are doing their Master’s student projects in our group: Fan, Chao and Lokesh. They gave me the opportunity to practice passing what I know to others and how to

address issues in more efficient way. Special thanks go to Chao: your hard work led to fulfilling my dream of making *ISSCC* finally appear in my publication list.

I want to thank my colleagues at NXP semiconductor: Roel Daamen, Aurélie Humbert and Youri V. Ponomarev for their cooperation and discussions in the Pasteur Project.

Thanks for my present and former roommates: Dr. Wang, Qi, Mahdi, Saleh, Caspar and Pelin. My thanks also go to Ali, Paddy, Joyce, Adri, Jawad, Willem and Karen for their administrative and financial support. I would like to thank Zu-yao, Piet, Jeroen, Jef and Lukasz for their help in technical problems. Special thanks must go to Zu-yao, who gave me so much help during my chip measurement. “Where is Zu-yao” is the first question comes to my mind if I run into issue with measurement equipment!

I also want to thank Sarah for her English corrections of this thesis.

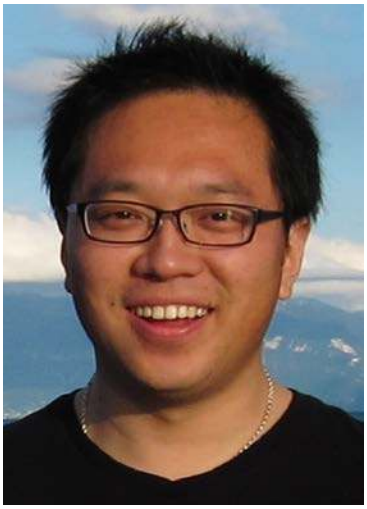
I want to thank all my lovely friends who made my life so enjoyable and warm: Ruimin (for all the transportation and accommodations in the past), Ning, Jianfeng, Sha&Zhongjie, Jianing, Zeyu, Yang, Huaiwen, Lei, Yue, Junfeng, Yongjia, Duan, Qinwen, Wanghua, Yuwei, Jinghuan, Yunan, Ming, Jia, Junchao, Qian (for checking these acknowledgements), Jiawen (for the cover design), and all those who I cannot name here.

Last but not the least, I would like to thank my parents for their love and encouragement. I really appreciate them for their understanding and being so supportive. From that spoiled boy who only knew how to play to the man who has written this complete thesis for his Ph.D. work, I must say: without you I am nothing and you are always the power behind my progress!

Zhichao Tan

Delft, May 2013

About the Author



Zhichao Tan was born in Shaanxi, China, in February 1982. He received his B.Eng. degree from Xi'an Jiaotong University, Xi'an, China, in 2004 and his M.Eng. degree from Peking University, Beijing, China, in 2008. He is currently working towards his Ph.D. degree at the Electronic Instrumentation Laboratory, Delft University of Technology, Delft, the Netherlands.

His Ph.D. topic is "Energy-Efficient Capacitive Sensor Interfaces". The results of his research have been applied in commercial sensor products in cooperation with NXP semiconductors. He is a two-time recipient of the IEEE Solid-State Circuits Society (SSCS) Student Travel Grant Award (STGA) from the Asian Solid-State Circuits Conference 2011 and Symposium on VLSI Circuit 2012. In addition to two book chapters, he has also authored and co-authored several technical journal and conference papers. His research interests include energy-efficient sensor interfaces and low power delta-sigma ADCs.

In his spare time, he likes playing violin (former member of Peking University student symphony orchestra) and tennis (NTRP level 3.0~3.5). He also enjoys swimming and jogging.