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Energy Efficient Swing signal generation circuits for clock distribution networks

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***Abstract*—**We propose Reduced Voltage Swing (RVS) signaling (by elevating the logic 0 voltage) as opposed to Low Voltage Swing (LVS) signaling (which reduces the logic 1 voltage). We propose an inverter which generates RVS signals, and an extension with programmable logic for adjusted logic 0 voltage. The proposed RVS scheme achieves reduced active power consumption, minimum performance degradation and minimum area overhead (without extra power supply network and a minimum number of extra transistors). Application of multi-threshold voltage design further alleviates compromises on noise margin and leakage. Experimental results based on SPICE simulation show that RVS clocking achieves an average of 37% active power consumption reduction, 8% performance degradation.

Keywords—VLSI, low power, reduced voltage swing, clock network.

I. INTRODUCTION

Continuous VLSI technology scaling has enabled integration of millions of transistors on a single chip working in over GHz clock frequencies. As a result, power consumption has increased steadily in recent technology nodes. It is increasingly critical to achieve low power consumption in modern VLSI designs due to the following reasons: (1) improving battery lifetime in mobile applications, (2) avoiding expensive cooling techniques for personal computers, and (3) enhancing energy efficiency for newly built data centers, web servers, supercomputing centers, etc.

Low-Voltage-Swing (LVS) is an effective active power consumption reduction technique since active power consumption is proportional to signal voltage swing. Interconnects are responsible for up to 50% of the active power consumption, while up to 90% of interconnect power consumption comes from only 10% of the interconnects, such as clock networks and global signal busses [1]. Developing LVS techniques for these powers hungry interconnects are critical to modern VLSI designs.

Existing LVS techniques achieve lower-voltage-swing signals either by a low power supply, or pulse signaling (terminating the signal before it rises to high voltage) [3][1] Reduced power consumption is achieved at the cost of (1) area overhead (especially for routing of the extra power supply network), (2) low supply voltage induced performance degradation, and (3) compromised signal reliability due to reduced noise margin and reduced signal width (for pulse signaling).

In this paper, we propose Reduced Voltage Swing (RVS) as opposed to the traditional Low Voltage Swing (LVS) scheme. We elevate the logic 0 voltage instead of lowering the logic 1 voltage. We propose an inverter design which generates RVS signals at the cost of an extra transistor, and an extension of the RVS inverter with programmable gates for adjustable logic 0 voltage. We achieve (1) minimum area overhead (by not requiring an extra power supply network), (2) minimum performance degradation (by keeping the supply voltage and the logic 1 voltage), and (3) robustness to process variations (the logic 0 voltage is adaptive to process variations). HSPICE simulation results show that we reduced active power consumption with very limited performance loss.

The rest of the paper is organized as follows. Existing low voltage swing signal and clocking is presented in Section II. Section III presents the reduce voltage swing principle and circuit followed by implementation and simulation results in section VI. Finally section V Concludes the paper.

II. EXISTING LOW-VOLTAGE-SWING SIGNALING AND CLOCKING SCHEMES

Existing low voltage swing circuits [2] process a number of deficiencies, such as: the need for extra supplies, performance impact, differential signaling and reliability degradation. They typically look at reducing the supply voltage on the targeted net, which impacts timing significantly. Most of the papers describing low or reduced voltage swing signals are targeting clock network or signal nodes with high capacitance to reduce power. Zhang et al. [2] surveyed the different options and circuits used to generate small or reduced signal swings. The paper lists the comparison of speed, power, and complexity of the different options. It also points out the deficiencies of each scheme. They also proposed their own scheme called pseudo differential Interconnect (PDIFF). However, all these LVS signaling schemes require an extra power supply which adds cost and complexity to the design.

A LVS clocking scheme which requires only a single power supply is proposed [3], wherein intermediate clock buffers are turned off once they reach the desired voltage levels. This makes the clock node essentially floating and is susceptible to noise. Subsequent regular clock buffers act as amplifiers which restore the clock signal to full swing. The short circuit power consumption of these amplifier clock buffers is reduced through the usage of small and high threshold voltage transistors.

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III. REDUCE VOLTAGE SWING PRINCIPLE AND CIRCUITS

Traditional LVS signaling schemes reduces signal voltage swing by lowering the logic 1 voltage. In contrast, we propose to reduce signal voltage swing by elevating the logic 0 voltages (Fig. 1).

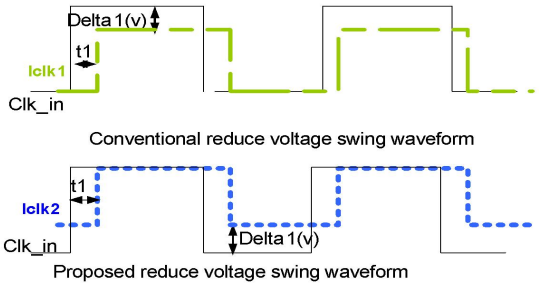

Figure 1: Traditional and new reduce voltage swing waveforms

Fig. 2 gives the inverter design which generates RVS signals. An extra NMOS transistor is inserted between the original NMOS transistor and the ground. It is gated by the output, such that the output discharge path to the ground is cut off when the output voltage is lower than the threshold voltage of the extra NMOS transistor. This leads to an elevated logic 0 voltage, reduced signal voltage swing, and degraded signal transition time (due to the extra serial NMOS transistor).

Let us compare these two schemes in terms of some of the key design metrics.

- Area. Traditional LVS signaling requires an extra power supply, routing of such an extra power supply network gives rise to considerable area overhead. RVS signaling does not require extra power supply, and has only one extra transistor for each inverter.
- Power consumption. Active power consumption is proportional to signal voltage swing. As a result, LVS and RVS signaling are equivalent in reducing signal voltage swing hence active power consumption.
- Performance. Low supply voltage and low logic 1 voltage in LVS signaling lead to performance degradation. While in RVS signaling, the constant supply voltage and logic 1 voltage do not degrade performance[2]
- Noise margin. The reduced signal voltage swing needs to cover the receiver flip-flop's meta-stability point (e.g., 0.5Vdd), and the minimum distance from the metastability point to input signal voltage swing boundary gives noise margin. For this, the noise margin for the proposed RV signaling scheme is given by the difference between the NMOS threshold voltage of the driver and the NMOS threshold voltage of the receiver.

An increased noise margin is achieve in multiple-threshold design, where the driver (inverter) is implemented in low threshold voltage (LVT) technology, while the receiver (flip-flop/latch) is implemented in high threshold voltage (HVT) technology. This enables a built in noise margin on the net lclk2 which is equal to the voltage difference between the HVT and LVT values. Also the receiver HVT transistor and its drain to source voltage being less than V_{dd} minimize the increased leakage due to elevated gate voltage. The receiver SSTC latch topology [5] is selected because the clock pin goes only into NFET transistor which eliminates the need of level translation to prevent short circuit current. Another advantage of this design is that the *lclk2* is always going to be actively driven. In case of coupling noise high on *lclk2* net the pull down stack will turn on and clear any charge on the net before it reaches the threshold for the receiver HVT nfet. This is true because the driver is LVT and the receiver is HVT device. The addition of series transistor to the final driver slows down the falling edge of the clock which only affect hold time and not the speed of the circuit *(clk− > q − delay)*. The M1 transistor that is controlled by *powermode* is meant as an override mode to the system. If *powermode* is set to 1 the RVS circuit will behave the same as the traditional one.

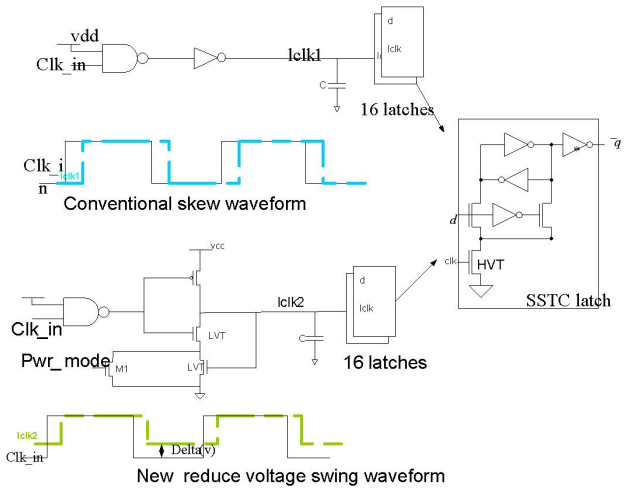

Figure 2: Traditional and new RVS illustration.

One limitation of the new circuit shown in Fig. 2 is that it only limits the swing of *lclk2* between V_{dd} and $V_{dd} - V_t$ where V_t is the value of the threshold voltage of the LVT transistor. We developed another circuit (Fig. 3) that gives programmability to the value to logic 0 based on control bits *Cnt[n : 0]:* The Programmable Reduced Voltage Swing (PRVS) circuit can vary the logic 0 value based on how many bits of *Cnt[n : 0]* bus are selected. The *Cnt[n : 0]* bits each corresponds to *W[n : 0]* transistor and it varies how fast the *fdb* node can be discharged to V_t through the dotted path 1. Both *Mp1* and *Mkp* are minimum size devices to pull up the *fdb* node and both have no impact on the circuit speed.

IV. EXPERIMENTS/SIMULATION

Comparing the proposed RVS signaling with the traditional LVS signaling and full voltage swing (FVS) signaling, we achieve HSPICE simulation results for a variety of design

parameters (supply voltage, load capacitance, input signal slew rate).

To compare our proposed RVS inverter and traditional full voltage swing (FVS) inverter, we achieve HSPICE simulation results for the two inverters with 2fF load capacitance under 0.9, 1.0, 1.1, 1.2, 1.3, 1.4, and 1.5V supply voltage. Table1 gives the average comparison results between FVS and RVS inverters.

Table 1 Comparison of full swing and RVS inverters.

	FVS	RVS
Power (uW)	0.279	0.107
Delay (ps)	0.449	0.394
Rise Slew Rate (ps)	0.074	0.168
Fall Slew Rate (ps)	0.074	0.131

To further verify this approach, we build a clock spine which drives an array of 6 * 32 = 192 flip-flops. HSPICE simulation shows that by replacing the clock buffers with the proposed RVS buffers as shown in figure 4, we achieve 37.2% power reduction, while the signal propagation delay from the spine input to a flip-flop is degraded by 8.6%, and clock signal slew rate is degraded by 30.0%. Table 2 gives the comparison results and figure 5 shows waveform of RVS and output results.

A complete measurements table is shown in table 3 where we show active power, leakage power, rise delay (delay is measured by 50%V_{dd}, fall delay, rise slew rate, and fall slew rate for different V_{dd}, C_{load}, and input slew rate for the 32nm technology.

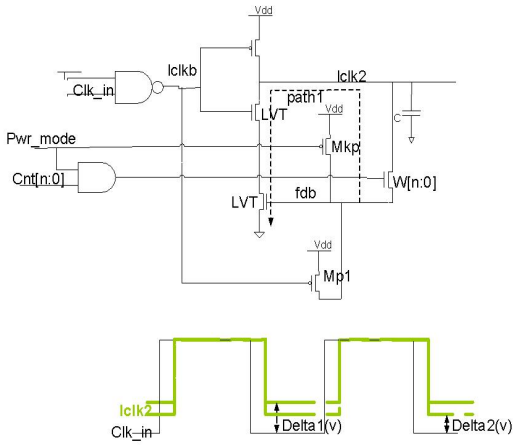

Figure 3: Programmable Reduced Voltage Swing Circuit and waveforms

Table 2 Comparison of FVS or RVS clock buffers.

	Delay *(ps)*	Slew rate*(ps)*	Power*(mW)*
FVS	185	4	3.709
RVS	201	5.2	2.7

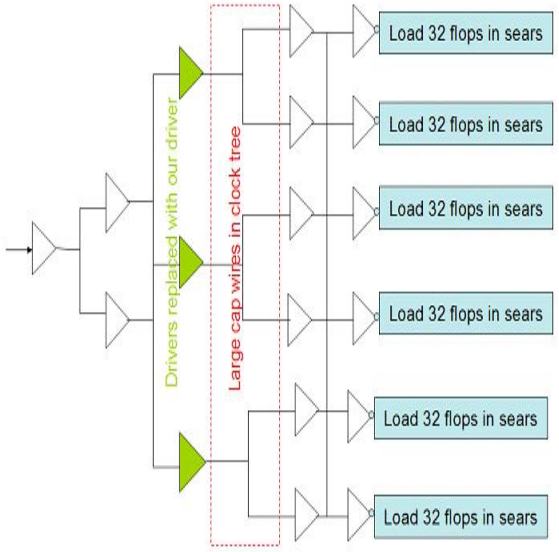

Figure 4 spine and load circuit

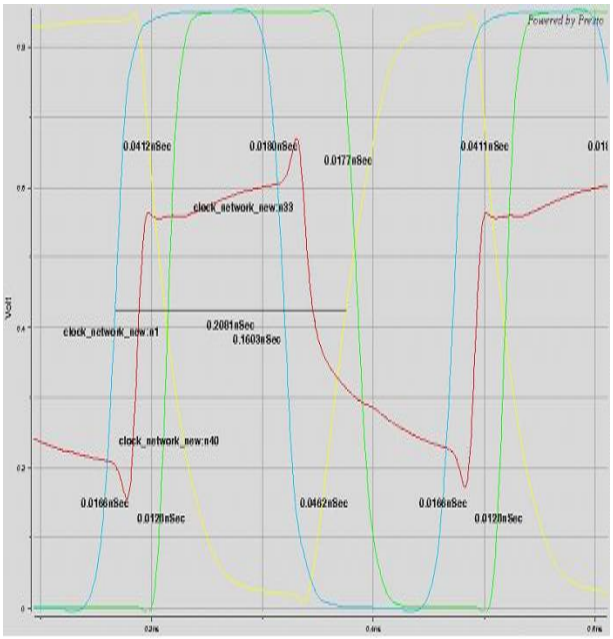

Figure 5 output and RVS simulation waveform results.

Table 3: simulation comparison with different setup

	clkin	Input	Power(w)		Delay(ps)		Slope(ps)			
cap(F)	pwidth	voltage	old	new	old	new	Fall old	Fall new	Rise old	Rise new
2.00E-15	2.0E-10	0.9	8.7E-06	3.9E-06	39.93	37.24	4.40	10.66	4.40	13.57
0	3.0E-10	0.9	1.2E-05	7.9E-06	52.15	42.62	6.55	13.45	6.55	19.41
2.00E-15	3.0E-10	0.9	5.7E-06	2.6E-06	39.99	38.37	4.40	10.66	4.40	13.57
0	4.0E-10	0.9	8.3E-06	5.3E-06	52.20	45.29	6.55	13.45	6.55	19.41
2.00E-15	4.0E-10	0.9	4.3E-06	1.9E-06	40.01	38.86	4.40	10.66	4.40	13.57
0	5.0E-10	0.9	5.9E-06	4.0E-06	52.22	46.37	6.55	13.45	6.55	19.42
2.00E-15	5.0E-10	0.9	3.5E-06	1.6E-06	40.02	39.17	4.40	10.66	4.40	13.59
0	6.0E-10	0.9	5.1E-06	3.2E-06	52.23	47.03	6.55	13.45	6.55	19.43
2.00E-15	6.0E-10	0.9	3.2E-06	1.3E-06	40.03	39.40	4.40	10.66	4.40	13.59
0	2.0E-10	1	4.3E-06	2.6E-06	52.24	47.51	6.55	13.45	6.55	19.43
2.00E-15	2.0E-10	1	1.2E-05	4.8E-06	33.93	31.31	3.98	9.87	3.98	10.57
0	3.0E-10	1	1.6E-05	9.8E-06	44.57	36.89	5.90	12.61	5.90	14.98
2.00E-15	3.0E-10	1	7.6E-06	3.2E-06	33.95	32.22	3.98	9.87	3.98	10.59
0	4.0E-10	1	1.1E-05	6.5E-06	44.59	39.01	5.90	12.61	5.90	14.96
2.00E-15	4.0E-10	1	5.7E-06	2.4E-06	33.96	32.63	3.98	9.87	3.98	10.58
0	5.0E-10	1	7.7E-06	4.9E-06	44.60	39.89	5.90	12.61	5.90	14.98
2.00E-15	5.0E-10	1	4.7E-06	1.9E-06	33.96	32.89	3.98	9.87	3.98	10.58
0	6.0E-10	1	6.7E-06	3.9E-06	44.60	40.44	5.90	12.61	5.90	14.97
2.00E-15	6.0E-10	1	4.2E-06	1.6E-06	33.96	33.07	3.98	9.87	3.98	10.58
0	2.0E-10	1.1	5.6E-06	3.3E-06	44.61	40.83	5.90	12.61	5.90	14.96
2.00E-15	2.0E-10	1.1	1.5E-05	5.8E-06	29.96	27.28	3.73	9.45	3.73	8.91
0	3.0E-10	1.1	2.1E-05	1.2E-05	39.49	32.98	5.49	12.25	5.49	12.43
2.00E-15	3.0E-10	1.1	1.0E-05	3.9E-06	29.97	28.07	3.73	9.45	3.73	8.88
0	4.0E-10	1.1	1.4E-05	7.9E-06	39.49	34.80	5.49	12.25	5.49	12.43
2.00E-15	4.0E-10	1.1	7.6E-06	2.9E-06	29.97	28.43	3.73	9.45	3.73	8.87
0	5.0E-10	1.1	1.0E-05	5.9E-06	39.49	35.56	5.49	12.25	5.49	12.43
2.00E-15	5.0E-10	1.1	6.2E-06	2.3E-06	29.97	28.65	3.73	9.45	3.73	8.88
0	6.0E-10	1.1	8.6E-06	4.8E-06	39.49	36.04	5.49	12.25	5.49	12.43
2.00E-15	6.0E-10	1.1	5.6E-06	1.9E-06	29.97	28.81	3.73	9.45	3.73	8.89
0	2.0E-10	1.2	7.2E-06	4.0E-06	39.49	36.38	5.49	12.25	5.49	12.42
2.00E-15	2.0E-10	1.2	2.0E-05	7.0E-06	27.33	24.43	3.57	9.18	3.57	7.90
0	3.0E-10	1.2	2.7E-05	1.4E-05	36.05	30.19	5.26	12.06	5.26	10.94
2.00E-15	3.0E-10	1.2	1.3E-05	4.6E-06	27.34	25.13	3.57	9.18	3.57	7.91
0	4.0E-10	1.2	1.8E-05	9.5E-06	36.05	31.81	5.26	12.06	5.26	10.91
2.00E-15	4.0E-10	1.2	9.9E-06	3.5E-06	27.34	25.46	3.57	9.18	3.57	7.91
0	5.0E-10	1.2	1.3E-05	7.1E-06	36.05	32.50	5.26	12.06	5.26	10.93
2.00E-15	5.0E-10	1.2	8.2E-06	2.8E-06	27.34	25.66	3.57	9.18	3.57	7.91
0	6.0E-10	1.2	1.1E-05	5.7E-06	36.05	32.93	5.26	12.06	5.26	10.94
2.00E-15	6.0E-10	1.2	7.4E-06	2.3E-06	27.34	25.79	3.57	9.18	3.57	7.90
0	2.0E-10	1.3	9.3E-06	4.7E-06	36.05	33.23	5.26	12.06	5.26	10.94
2.00E-15	2.0E-10	1.3	2.6E-05	8.2E-06	25.60	22.32	3.53	8.85	3.53	7.30
0	3.0E-10	1.3	3.4E-05	1.7E-05	33.69	28.06	5.11	11.92	5.11	10.00
2.00E-15	3.0E-10	1.3	1.7E-05	5.5E-06	25.60	22.95	3.53	8.85	3.53	7.28
0	4.0E-10	1.3	2.3E-05	1.1E-05	33.69	29.55	5.11	11.92	5.11	9.97
2.00E-15	4.0E-10	1.3	1.3E-05	4.1E-06	25.60	23.24	3.53	8.85	3.53	7.27
0	5.0E-10	1.3	1.6E-05	8.3E-06	33.69	30.18	5.11	11.92	5.11	10.00
2.00E-15	5.0E-10	1.3	1.1E-05	3.3E-06	25.60	23.42	3.53	8.85	3.53	7.26
0	6.0E-10	1.3	1.4E-05	6.7E-06	33.69	30.56	5.11	11.92	5.11	10.01
2.00E-15	6.0E-10	1.3	9.6E-06	2.7E-06	25.60	23.54	3.53	8.85	3.53	7.26
0	2.0E-10	1.4	1.2E-05	5.6E-06	33.69	30.83	5.11	11.92	5.11	10.01
2.00E-15	2.0E-10	1.4	3.4E-05	9.5E-06	24.48	20.70	3.49	8.46	3.49	6.91
0	3.0E-10	1.4	4.3E-05	1.9E-05	32.08	26.34	5.10	11.77	5.10	9.41
2.00E-15	3.0E-10	1.4	2.3E-05	6.3E-06	24.48	21.27	3.49	8.46	3.49	6.91
0	4.0E-10	1.4	2.9E-05	1.3E-05	32.08	27.70	5.10	11.77	5.10	9.40
2.00E-15	4.0E-10	1.4	1.7E-05	4.8E-06	24.48	21.52	3.49	8.46	3.49	6.92
0	5.0E-10	1.4	2.1E-05	9.7E-06	32.08	28.28	5.10	11.77	5.10	9.40
2.00E-15	5.0E-10	1.4	1.4E-05	3.8E-06	24.48	21.67	3.49	8.46	3.49	6.92
0	6.0E-10	1.4	1.8E-05	7.7E-06	32.08	28.63	5.10	11.77	5.10	9.40
2.00E-15	6.0E-10	1.4	1.3E-05	3.2E-06	24.48	21.77	3.49	8.46	3.49	6.92
0	2.0E-10	1.5	1.5E-05	6.4E-06	32.08	28.87	5.10	11.77	5.10	9.40
2.00E-15	2.0E-10	1.5	4.3E-05	1.1E-05	23.76	19.43	3.51	8.01	3.51	6.67
0	3.0E-10	1.5	5.4E-05	2.2E-05	30.98	24.89	5.07	11.61	5.07	9.05
2.00E-15	3.0E-10	1.5	2.9E-05	7.3E-06	23.76	19.92	3.51	8.01	3.51	6.67
0	4.0E-10	1.5	3.7E-05	1.5E-05	30.98	26.13	5.07	11.61	5.07	9.04
2.00E-15	4.0E-10	1.5	2.2E-05	5.5E-06	23.76	20.13	3.51	8.01	3.51	6.67
0	5.0E-10	1.5	2.6E-05	1.1E-05	30.98	26.66	5.07	11.61	5.07	9.03
2.00E-15	5.0E-10	1.5	1.8E-05	4.4E-06	23.76	20.26	3.51	8.01	3.51	6.67
0	6.0E-10	1.5	2.3E-05	8.9E-06	30.98	26.97	5.07	11.61	5.07	9.02
2.00E-15	6.0E-10	1.5	1.6E-05	3.6E-06	23.76	20.33	3.51	8.01	3.51	6.67

V. CONCLUSION

In this paper, we propose Reduced-Voltage-Swing (RVS) signaling as opposed to the traditional Low-Voltage-Swing (LVS) signaling for reduced active power consumption. We achieve minimum area overhead (without routing of an extra power supply network and a minimum number of extra transistors), equivalent active power reduction, and minimum performance degradation. HSPICE simulation results with respect to a variety of design parameters (supply voltage, load capacitance, input signal slew rate, etc.) verifies the effectiveness of these novel RVS circuits, which save an average of 37.2% dynamic power, with 8.6% clock insertion delay increase in a clock spine driving 192 flip-flops.

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[1] While a number of level converters have been developed which turn a low voltage swing signal into a full swing signal [3].

[2] While performance degradation exists due to degraded signal transition time in implementation.