Energy/Reliability Trade-Offs in Low-Voltage ReRAM-Based Non-Volatile Flip-Flop Design

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***Abstract*—The total power budget of Ultra-Low Power (ULP) VLSI Systems-on-Chip (SoCs) is often dominated by the leakage power of embedded memories as well as status registers. On the one hand, supply voltage scaling down to the near-threshold (near-V_T) or even to the subthreshold (sub-V_T) domain is a commonly used, efficient technique to reduce both leakage power and active energy dissipation. On the other hand, emerging CMOS-compatible device technologies such as Resistive Memories (ReRAMs) enable non-volatile, on-chip data storage and zero-leakage sleep periods. For the first time, we present and compare ReRAM-based Non-Volatile Flip-Flop (NVFF) topologies which are optimized for low-voltage operation (including near-V_T and sub-V_T operation). Three low-voltage NVFF circuit topologies are proposed and evaluated in terms of energy dissipation and reliability. Using topologies with two complementary programmed ReRAM devices, Monte Carlo simulations accounting for parametric variations confirm reliable data restore operation from the ReRAM devices at a sub-V_T voltage as low as 400 mV. A topology using a single ReRAM device exhibits lower write energy, but requires a near-V_T voltage for robust read. Energy characterization is performed at nominal, near-V_T, and sub-V_T supply voltages. The minimum energy point is reached for near-V_T read operation with a total read+write energy of 735 fJ.**

***Index Terms*—Flip-flops, low-power electronics, nonvolatile memory.**

I. Introduction

Ultra-low power (ULP) VLSI systems such as wireless sensor nodes [1] and biomedical implants [2], running for many days or even for several years on a single battery charge, have extremely low power budgets. Embedded memories as well as status and pipeline registers consume a dominant share of the total power and area of such systems [3], while for the digital signal processing core the share is often small. This power dominance of memories is further exacerbated for systems with only short active computational periods and long sleep periods requiring data and program state retention. In such cases, the leakage power of embedded memories and registers accounts for almost the totality of the VLSI system's power consumption.

Supply voltage scaling to the near-threshold (near-V_T) regime or even down to the subthreshold (sub-V_T) regime is an efficient technique to reduce leakage power consumption (as well as active energy dissipation), at the cost of a speed degradation and increased sensitivity to process parameter variations [4].

While near-V_T and sub-V_T operation enables extremely low leakage power, emerging device technologies allowing the integration of non-volatile memory devices on top of CMOS chips bear the potential of zero-leakage sleep states [5]. Among many technological options, Oxide Memories (OxRAMs) [6] are a promising candidate for next generation non-volatile memory applications. Compared to traditional Flash memories, OxRAMs have better scalability and faster programming time [6]. While a lot of research effort targets OxRAM-based stand-alone memories, this work focuses on the seamless integration of OxRAM devices into CMOS flip-flops for use as non-volatile, distributed storage elements. Previous works on non-volatile flip-flops were based on the "memristor" [5], [7], on bipolar OxRAM [8], and Magnetic Tunneling Junction (MTJ) devices [9]–[11]. All these works consider circuit operation at a high supply voltage, normally corresponding to the CMOS technology's nominal voltage.

In this work, we combine the advantages of an emerging non-volatile memory device technology (namely, OxRAM stacks) with the assets of low-voltage (near-V_T and sub-V_T) circuit operation by specifically optimizing the NVFF topologies for these operating regimes, thereby enabling future VLSI systems with ultra-low active energy dissipation in addition to non-volatile data storage with zero leakage. This article extends our previous work [12] by introducing two new NVFF topologies and by presenting a detailed comparative analysis of all topologies.

Our detailed, simulation-based analyses show that the state of the art of NVFF design is extended on the following fronts: 1) the NVFF topologies using two complementary programmed ReRAM devices reliably recover the saved data on wake-up with a sub-V_T supply voltage and a standard deviation of up to 5% of the nominal value of the ReRAM resistance; 2) in addition, all proposed NVFF circuits are able to reliably recover data

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with a High Resistance Value (HRV) to Low Resistance Value (LRV) ratio of less than two, even though a near-V_T voltage is required for the NVFF topology based on a single ReRAM device to do so; and 3) thanks to circuit optimizations allowing for aggressive voltage scaling (down to the sub-V_T domain for most circuits), the read energy has been drastically reduced to 5.4% of the total read+write energy, whereas for operation at nominal voltage, read and write would have similar energy costs.

The remainder of this paper is organized as follows. Section II introduces the manufactured ReRAM stacks and elaborates on their switching behavior. Next, Section III introduces three fundamentally different NVFF topologies based on one and two ReRAM devices and expatiates on their circuit-level optimizations for reliable low-voltage operation. Section IV presents detailed circuit simulation results of all NVFF topologies and compares their read robustness as well as their read and write energy at nominal, near-V_T, and sub-V_T supply voltages, and Section V concludes this paper.

II. Resistive Memory: Manufacturing Process and Switching Characteristics

Among many ReRAM candidates, OxRAMs base their working principle on the change in resistance of an oxide layer. Different physical mechanisms can be identified in the switching of ReRAMs [6]. In the following, we focus only on the Bipolar Resistive Switching (BRS) [13], related to the O_2 vacancy redistribution in transition metal oxide layers upon application of a voltage across the oxide. Oxide-based memories are promising for circuit applications thanks to their fast write time [14] and high endurance up to 10^{11} cycles [15].

We realized memory stack prototypes of $Al/TiO_2/Al$ from bulk-Si wafers passivated by a 100-nm thick Al_2O_3 layer. 70-nm thick Bottom Electrode (BE) lines were patterned by lift-off and e-beam evaporation. Then, a 50-nm thick TiO_2 layer was deposited by Atomic Layer Deposition (ALD) at 200°C. Finally, vertical Top Electrode (TE) lines were defined with a second lift-off step together with contact areas used for electrical characterization. Each fabricated device occupies an area of 1.5 μm^2. A Scanning Electron Microscopy (SEM) image of the fabricated devices is shown in Fig. 1. Note that a crossbar architecture was chosen only to ease the device demonstration and characterization. In the following circuit proposals, however, we consider single ReRAM devices embedded in CMOS NVFF topologies. As opposed to stand-alone memories, high integration density is not the primary objective of the present work. In fact, such OxRAM devices are eventually manufactured on top of standard, mature CMOS chips, with relaxed design rules.

In our ReRAM devices, the switching operations are enable after cycling the voltage across the device, as opposite to the traditional methodology, which involves larger voltages and current compliance to electrically form the devices. After 50 burn-in cycles, the resistive switching behavior stabilizes to the behavior shown in Fig. 1. Consistent BRS with a High Resistance State (HRS) and a Low Resistance State (LRS) is achieved. The SET and RESET threshold voltages range from -2 V to $+2$ V. Moreover, the switching operation is limited by a low current compliance of 10 μA, allowing the use of small (close to minimum size) programming transistors, which leads to a compact design. As reported in literature, there exist oxide stacks with higher compliance current, lower LRS, and a much higher HRS/LRS ratio, compared to our considered device. However, in this study, we chose a ReRAM device with low current compliance and high LRS on purpose, in order to minimize the size of the programming transistors and the write/read energies, while accepting a low HRS/LRS ratio. Note as well that this HRS/LRS ratio, smaller than two, can be considered a worst case ratio with respect to the impact of variability compared to other devices, but it does neither significantly decrease the endurance, nor increase the variability [16]. In the following, we show that under this worst case assumption, it is still possible to obtain robust NVFF operation even at low voltages with proper circuit design. Higher HRS/LRS ratios would tremendously facilitate the circuit design and would improve the read robustness at low voltages even further.

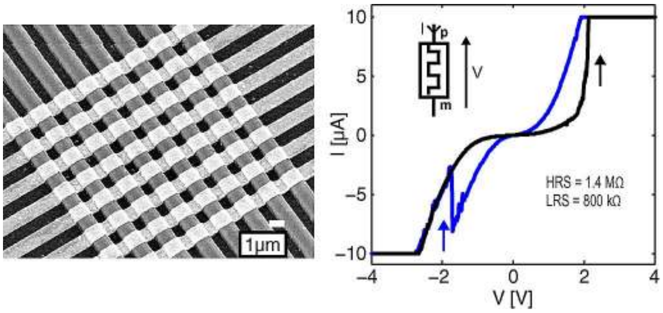

Fig. 1. 1.5 μm^2 $Al/TiO_2/Al$ ReRAM stack crossbar SEM image and single node switching characteristic under 10 μA current compliance. The crossbar structure is solely used for device characterization, while all NVFF topologies contain only one or two separate ReRAM stacks.

III. Non-Volatile Flip-Flop Topologies and Operation

This section explains the design and the operating principle of the various herein proposed ReRAM-based non-volatile flip-flop topologies. In all the designs, a conventional master/slave flip-flop based on tri-state inverters is modified to add the possibility of non-volatile data storage, through additional read and write sub-circuits to/from the ReRAM device(s), as shown in the block diagram in Fig. 2(a). The various NVFF topologies differ from each other mainly in their method of recalling the saved state from the ReRAM device(s) to the CMOS slave latch, and in the number and the position of the ReRAM devices inside the circuit. The writing process to the ReRAM device(s) is almost identical for all the circuits.

We first introduce a conventional master-slave flip-flop in CMOS technology with minor modifications to accommodate two complementary programmed ReRAM devices for non-volatility. Unfortunately, circuit simulations show that this baseline NVFF design works reliably only at high (close to nominal) supply voltages. Therefore, we then introduce three different NVFF topologies which are optimized for robust operation at low voltages (near-V_T and sub-V_T supply voltages). Two of these optimized NVFF topologies are similar to the baseline design in that they also use two complementary programmed ReRAM devices. However, circuit optimizations lead to robust operation at near-V_T and even at sub-V_T supply voltages. The third topology requires only a single ReRAM device and exhibits lower energy consumption than all previous topologies, which comes at the cost of reduced robustness.

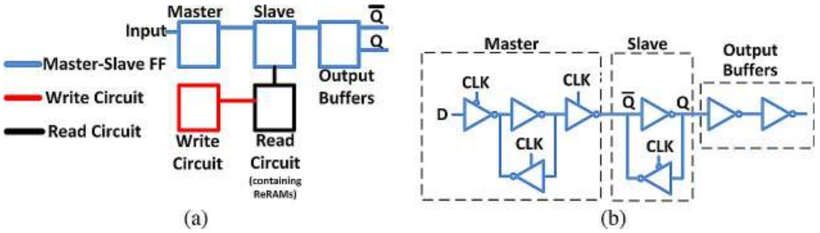

Fig. 2. (a) Conceptual block diagram of a non-volatile flip-flop; and (b) conventional master-slave flip-flop.

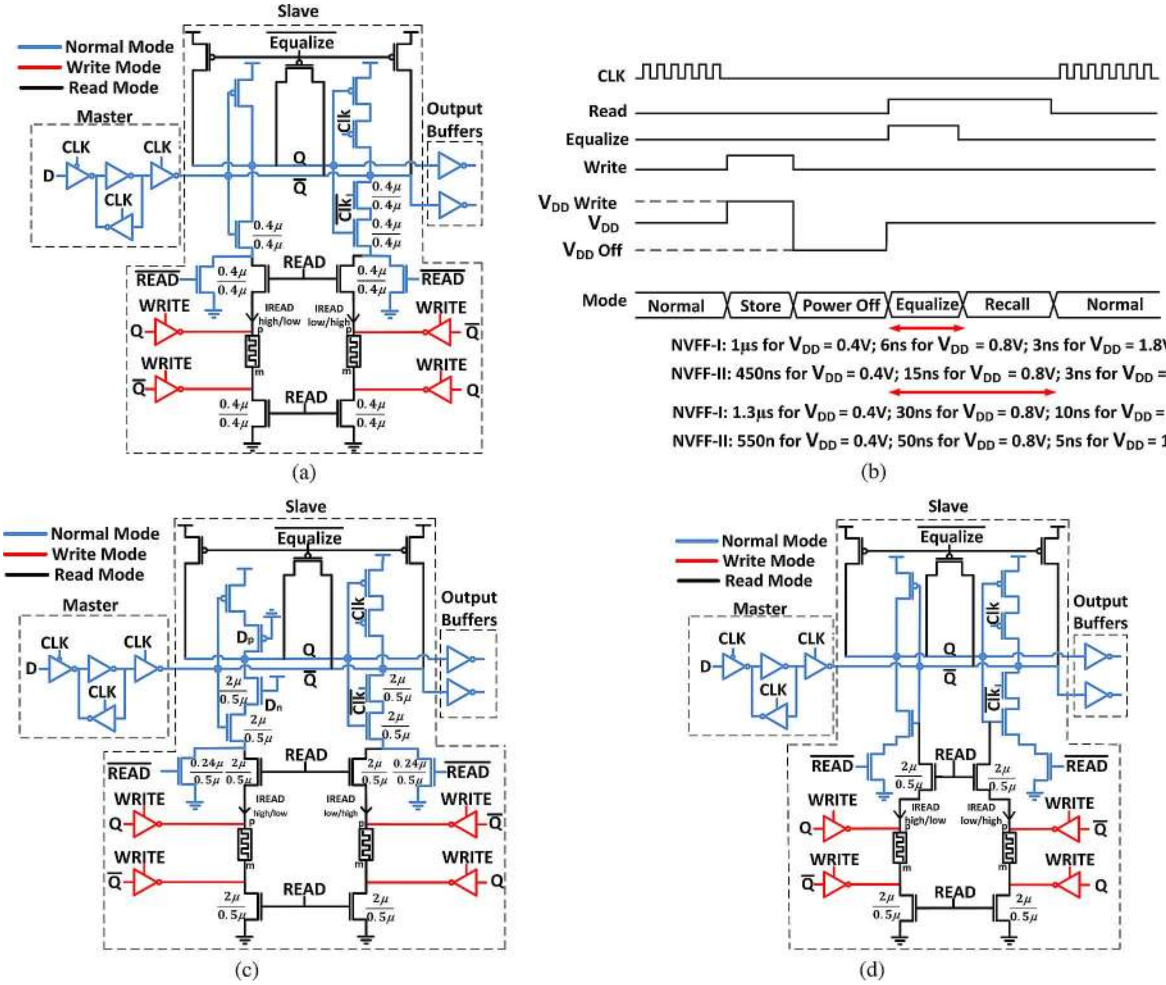
Normal Mode
Write Mode
Read Mode
Master
Slave
Equalize
CLK
D
Q
Q̄
Clk
Output Buffers
0.4µ/0.4µ
READ
WRITE
IREAD high/low
IREAD low/high
p
m
(a)
CLK
Read
Equalize
Write
V_DD Write
V_DD
V_DD Off
Mode
Normal
Store
Power Off
Equalize
Recall
Normal
NVFF-I: 1µs for V_DD = 0.4V; 6ns for V_DD = 0.8V; 3ns for V_DD = 1.8V
NVFF-II: 450ns for V_DD = 0.4V; 15ns for V_DD = 0.8V; 3ns for V_DD = 1.8V
NVFF-I: 1.3µs for V_DD = 0.4V; 30ns for V_DD = 0.8V; 10ns for V_DD = 1.8V
NVFF-II: 550n for V_DD = 0.4V; 50ns for V_DD = 0.8V; 5ns for V_DD = 1.8V
(b)
D_p
D_n
2µ/0.5µ
0.24µ/0.5µ
(c)
(d)

Fig. 3. (a) Baseline non-volatile flip-flop design (NVFF-0); (b) control signals sequence for ReRAM read and write operations for the complementary ReRAM-based NVFF circuits; (c) sub-V_{T} optimized NVFF structure, based on NVFF-0 topology (NVFF-I); and (d) sub-V_{T} optimized NVFF structure, inspired from [18] (NVFF-II).

A. Baseline Non-Volatile Flip-Flop (NVFF-0)

In order to enhance a conventional CMOS flip-flop structure, such as the one shown in Fig. 2(b), with non-volatile data storage, two ReRAM devices are inserted in the current sink of the cross-coupled inverter pair in the slave latch. The resulting baseline circuit, referred to as NVFF-0, is shown in Fig. 3(a). A similar circuit topology has been used in [17], which, however, used magnetic memory devices. In this baseline NVFF, the two ReRAM devices are always used in a complementary fashion, i.e., one device is programmed to the HRS, while the other one is programmed to the LRS. Dedicated non-volatile programming (or ReRAM write) circuits are highlighted in red color in Fig. 3(a), while dedicated restore on wake-up (or ReRAM read) circuits are shown in black color.

ReRAM Read Operation: During system wake-up (power-on), the slave latch would ideally be directly restored, based on the data stored in the ReRAM devices, during ramp-up or connection of the power supply. However, this is impossible due to a number of reasons: 1) the clock and the READ signal are not controlled yet; 2) there might be uncontrolled, residual charges on the internal nodes Q and $\overline{\mathrm{Q}}$; and 3) different power-gating approaches (mechanical, footer and/or header transistors, driving the supply to ground level) result in different wake-up scenarios. Therefore, the following wake-up sequence is proposed, as shown in Fig. 3(b): 1) turn on the power supply; 2) at the system level, silence the clock signal to low; 3) enable the READ and the EQUALIZE control signals; and 4) upon de-assertion of EQUALIZE, the slave latch is correctly restored based on the value of the ReRAM devices. Using this wake-up sequence, both internal storage nodes Q and $\overline{\mathrm{Q}}$ are first pre-charged and equalized using three dedicated PMOS transistors controlled by $\overline{\mathrm{EQUALIZE}}$. Following this pre-charge phase, the internal nodes Q and $\overline{\mathrm{Q}}$ are connected to ground through the ReRAM devices. The complementary resistance states of the two ReRAM devices modulate the discharge currents (the branch with HRS has a lower discharge current w.r.t. the branch with LRS), starting a race condition. As soon as one internal node is discharged to $V_{\mathrm{DD}} - V_{\mathrm{T,PMOS}}$, the PMOS transistor driven by that node turns *on* and starts to pull up the other internal node. This decides the race, before the feedback of the latch restores full logic levels.

ReRAM Write Operation: Prior to an active-to-sleep transition, the data stored in the slave latch needs to be written to the non-volatile ReRAM devices. To this end, as shown in Fig. 3(b), the clock is silenced and kept low for the entire duration of the ReRAM write operation, thereby forcing the slave latch to be non-transparent and isolated from the master. As shown in Fig. 3(a), during write, the ReRAM devices are completely disconnected from the slave latch and from the read circuits, so that the voltage drop across their terminals can be set by the write drivers (highlighted in red). The write drivers are controlled by the internal nodes Q and $\overline{\mathrm{Q}}$. In general, the write pulse width depends on the chosen ReRAM technology. Here, a write pulse width of 10 ns is used to successfully program the ReRAM devices. As previously illustrated in Fig. 1, a voltage of $+2$ V or -2 V is required for successful switching. To be able to use small programming transistors (with a non-negligible voltage drop across their channel) and limit the programming current, the write drivers are supplied with a voltage as high as 2.4 V. This voltage is only slightly above the nominal supply voltage range of the core transistors in the considered 0.18 μm CMOS technology and does neither seriously enhance the risk of oxide breakdown, nor compromise junction reliability, nor considerably accelerate aging.

While the ReRAM write operation requires a high voltage, the ReRAM read operation as well as the normal flip-flop operation can be performed at scaled voltages for better energy efficiency. Several architectural alternatives for the distribution of the high supply voltage are discussed in [12]. Here, we adopt the approach of dynamically rising the supply voltage of all NVFFs during a write operation, as shown in Fig. 3(b).

Normal Operation and Endurance: Note that during normal operation, the presented hybrid CMOS/ReRAM NVFF, and all other NVFF topologies introduced in the following, fully rely on CMOS transistors, which are known to exhibit high endurance. The part of the NVFF circuits containing ReRAM devices, whose endurance is not yet comparable with the one of CMOS transistors, do not switch very frequently (only during active-to-sleep state transitions), which guarantees high overall system endurance. Finally, note that the setup and hold times during normal operation of all herein proposed NVFF topologies are solely determined by the master latch and are not affected by the insertion of the ReRAM devices in the slave latch. The data call window of the presented NVFFs is therefore equal to the one of the conventional CMOS flip-flop shown in Fig. 2(b).

B. NVFF Topologies for Robust Sub-V_{T} and Near-V_{T} Operation (NVFF-I and NVFF-II)

For the baseline NVFF circuit (NVFF-0) shown in Fig. 3(a), a correct read operation depends on the modulation of the discharge currents (discharging nodes Q and $\overline{\mathrm{Q}}$) by the complementary ReRAM devices. However, the discharge currents might be altered due to the following reasons: 1) different pull-down networks in the two branches due to the use of either a simple or a tri-state inverter; and 2) mismatch between the transistor pairs (in the inverters and in the dedicated read transistors) and the ReRAMs, caused by local variations. Post-layout circuit simulations show that the read operation of the NVFF-0 circuit works reliably at nominal supply voltage, whereas the Pull-Down Network (PDN) mismatch other than the complementary resitance values leads to read failures at low voltages (see Section IV for detailed simulation results). Therefore, in order to enable the straightforward integration of ReRAM-based NVFFs into ultra-low power VLSI SoCs, i.e., operated in the near-V_{T} or sub-V_{T} domain, we introduce in the following two NVFF topologies which are optimized for operation at low voltages.

The two sub-V_{T} optimized NVFF-I and NVFF-II structures are shown in Fig. 3(d) and Fig. 3(c), respectively, with the dedicated programming (ReRAM write) circuits highlighted in red and the restore (ReRAM read) circuits in black. Both NVFF-I and NVFF-II use the same control signal sequence, shown in Fig. 3(b) during active-to-sleep and sleep-to-active transitions as the baseline circuit NVFF-0. Similarly to NVFF-0, the two ReRAM devices are used in a complementary way, i.e., one device is programmed to the HRS, while the other one is programmed to the LRS. The main difference between these two architectures is the connection of the read circuit to the slave latch of the CMOS flip-flop. Inspired by [18], the read circuit of NVFF-II is connected to the output nodes, Q and $\overline{\mathrm{Q}}$, while, in the NVFF-I topology, it is connected to the source of the NMOS transistors of the slave latch. Hence, during read operation, the PDN of NVFF-II consists of only the portion shown in black, whereas for NVFF-I, the PDN is composed of the circuit shown in black and the NMOS transistors shown in blue (which are part of the inverters forming the slave latch).

Since it is crucial to modulate the discharge current of the precharged nodes Q and $\overline{\mathrm{Q}}$ exclusively by the value of the ReRAM devices to ensure correct read at low voltages, any other type of mismatch in the PDN needs to be avoided. To this end, in case of NVFF-I, two always-*on* transistors (D_n and D_p) are inserted into the simple inverter (used in NVFF-0) to mimic the tri-state inverter in the other pull-down branch. The insertion of dummy transistors can be avoided in the NVFF-II topology, because the ReRAMs are connected to the output nodes rather than integrated in the PDN of the inverters. Moreover, all transistor pairs in the PDNs of both NVFF-I and NVFF-II are upsized to further improve matching (see Fig. 3(d) and Fig. 3(c) for the exact transistor dimensions).

C. NVFF Topology With Single ReRAM Device (NVFF-III)

All NVFF topologies considered so far require two ReRAM devices and a non-trivial wake-up sequence. Unfortunately, the total write energy increases with the number of ReRAM devices used in the NVFF topology. Therefore, this section proposes an

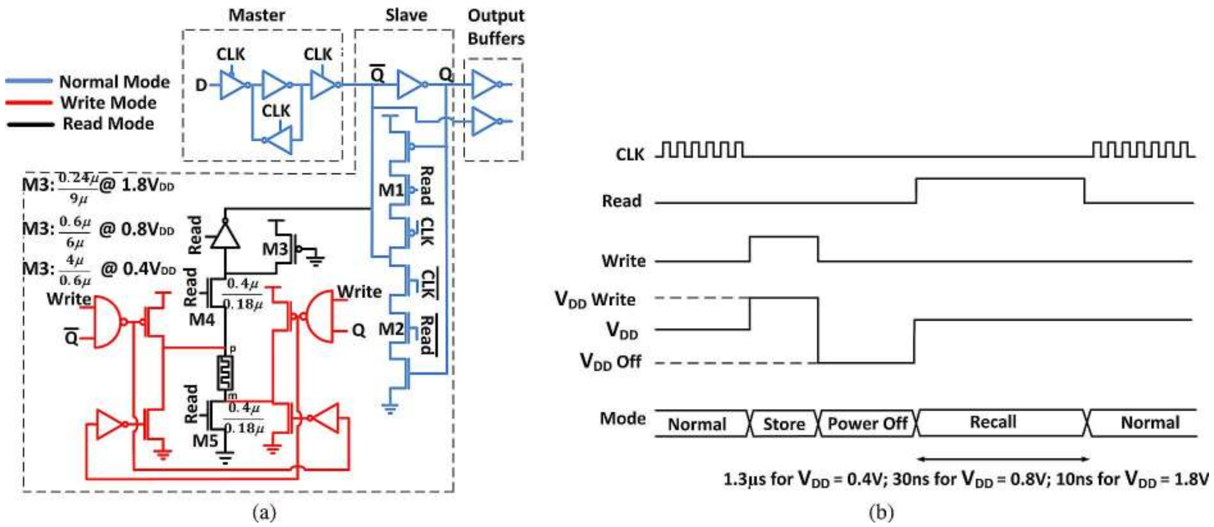

Fig. 4. (a) NVFF architecture with a single ReRAM device (NVFF-III); and (b) the corresponding control sequence for read and write operation.

NVFF topology which is based on a single ReRAM device, that leads to lower write energy, and allows for a simplified wake-up control signal sequence. Our NVFF topology is similar to [5] but uses our custom oxide stack (see Section II) instead of HP's "memristor" [7]. This single-ReRAM NVFF architecture, referred to as NVFF-III, is depicted in Fig. 4(a).

ReRAM Read Operation: When the VLSI system is in recall mode (after wake-up), the slave latch is disconnected from the master by keeping the clock signal low, as shown in Fig. 4(b). This is done to ensure that the recalled value is not overwritten by any disturbance from the master latch. Moreover, compared to the standard CMOS master/slave flip-flop shown in Fig. 2(b), two transistors (M1 and M2) are added to disable the feedback mechanism in the slave latch during the ReRAM read operation. Therefore, the inverting buffer controlled by the READ signal (also referred to as sense inverter) can easily impose a value to the slave latch during wake-up, according to the state of the ReRAM device. The READ signal is set high so that the ReRAM can be accessed through the transistors M4 and M5. The PMOS transistor M3 acts as a current source and provides a voltage drop across the ReRAM device. M3 needs to be sized carefully. In fact, its sizing depends on the power supply voltage, the voltage transfer curve of the sense inverter (especially the trip-point), and the HRS and LRS of the ReRAM device. The sizing of M3 ensures that two logically distinct input states for the sense inverter can be produced depending on the resistance of the ReRAM device. Once the READ signal goes high, the sense inverter is turned on and forces a logic state onto the internal node $\overline{\mathrm{Q}}$ of the slave latch. If the ReRAM is in LRS, a logic "1" is produced at node $\overline{\mathrm{Q}}$, and vice versa.

ReRAM Write Operation: Prior to an active-to-sleep transition, the ReRAM device is programmed to HRS or LRS during a write operation, depending on the logic state of Q and $\overline{\mathrm{Q}}$. Compared to all previously presented NVFF circuits (NVFF-0, NVFF-I, and NVFF-II), the write circuit is slightly modified in order to enable a slight reduction in the write supply. In fact, in Fig. 3(c) and (d), a tri-state inverter is used to connect the ReRAM devices to V_{DD} (and ground) during write. In this case, there is a stack of two transistor between the ReRAM devices and V_{DD} (internal tri-state inverter topology), and a write voltage of 2.4 V is required to account for the voltage drop across the transistor stack. In contrast, in Fig. 4(a), the write transistor is directly connected to the ReRAM device and is controlled by a NAND gate. Hence, there is only a single transistor between V_{DD} and the ReRAM device, and the write voltage can be reduced to 2.2 V. During normal mode of operation, the read (black) and write (red) circuits are disconnected from the rest of the main flip-flop.

IV. Energy and Reliability Analysis

In this section, the reliability of low-voltage (near-V_{T} and sub-V_{T}) operation as well as the energy dissipation of the various, previously introduced NVFFs are characterized. First, the post-layout simulation setup and the methodology to account for parametric variations in MOS transistors and ReRAM devices are described. Then, detailed, comparative simulation results for read robustness and energy dissipation, during read and write, of all NVFF topologies are presented.

A. Methodology and Simulation Setup

The ULP and especially the biomedical VLSI design community often prefers to use mature CMOS technology nodes for 1) high reliability, 2) low leakage currents, and 3) low cost. Therefore, this study adopts a mature $0.18\,\mu$m CMOS process. All simulations, run by CADENCE Spectre, assume a Typical-Typical (TT) process corner at $27\,^{\circ}$C. A dynamically adjustable power supply is presumed, switching between 2.4 V for write operations, and a lower value (V_{DD}) for read as well as normal operation (flip-flop sampling operation). V_{DD} assumes the technology's nominal value (1.8 V), a near-V_{T} value (0.8 V), and a sub-V_{T} value (0.4 V). Monte Carlo circuit simulations (1000 runs) account for local parametric variations of all MOS transistors, according to statistical distributions provided by the foundry. While advanced statistical models of the ReRAM devices are not available yet, we assume that the HRS and the LRS follow a Gaussian distribution. The measured, nominal value of HRS (1.4 MΩ) and LRS (800 kΩ) is taken as mean value, denoted by $\mu(\mathrm{HRS})$ and $\mu(\mathrm{LRS})$. The values 40 kΩ, 80 kΩ, and 160 kΩ corresponding to 5%, 10% and 20% of $\mu(\mathrm{LRS})$, respectively, are taken for the standard deviation, denoted by $\sigma(\mathrm{HRS})$ and $\sigma(\mathrm{LRS})$. Please note that these assumed HRS and LRS distributions correspond well

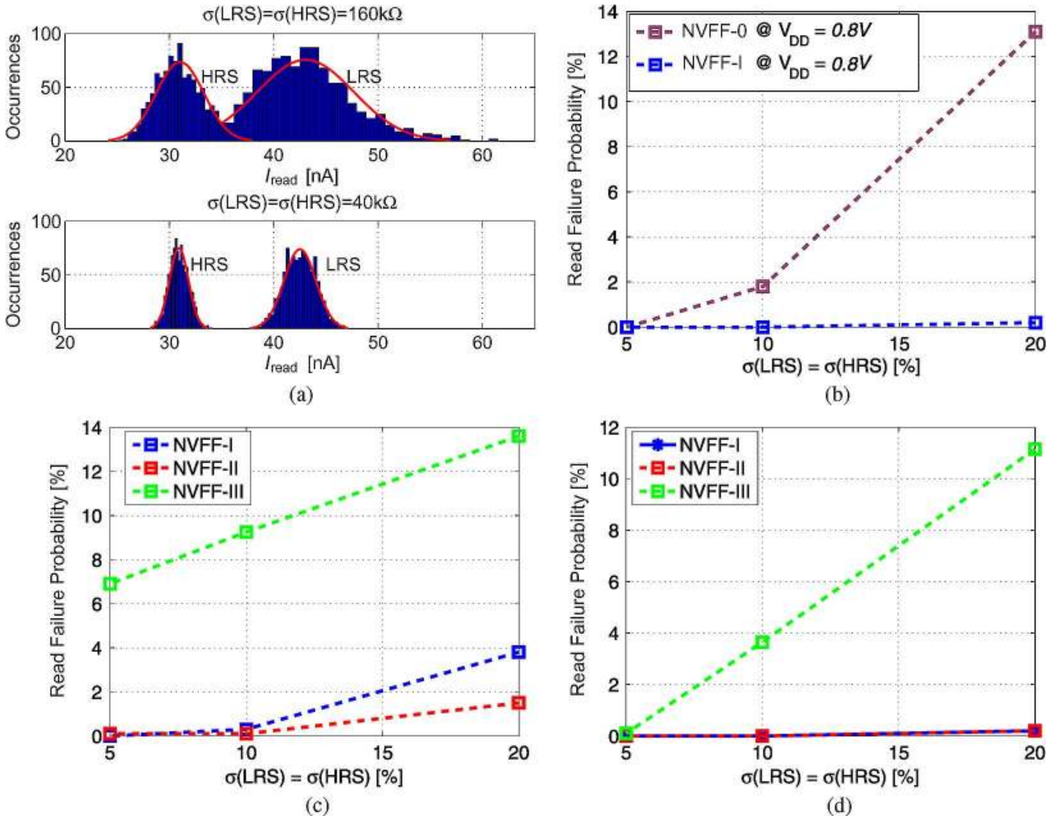

Fig. 5. (a): Distribution of the discharge current ($I_{\rm read}$) through the two branches of the slave latch of the sub-$V_{\rm T}$-optimized NVFF-I circuit, for 0.4 V, given for two different standard deviations of the ReRAM's resistance; (b)–(c): Read failure probabilities for a ReRAM resistance's standard deviation of 5%, 10%, and 20% of the nominal LRS value: (b) low-voltage optimization, NVFF-0 → NVFF-I, 0.8 V; (c) comparison NVFF-I–NVFF-III, 0.4 V; and (d) comparison NVFF-I–NVFF-III, 0.8 V.

with reports about comparable state-of-the-art oxide stacks available in the literature [19], showing LRS (σ/μ) ratios of 20% under the same electrical conditions. Also, for mature CMOS technologies, the (σ/μ) ratios of most parameters of MOSFETs, such as the threshold voltage or the saturation current, typically range from 1% to 10% [20], [21]. Therefore, for our ReRAM devices, we are indeed considering both the case of a realistic, future, mature ReRAM process ($\sigma/\mu = 5\%$), comparable to CMOS), and the case of a currently still less mature ReRAM process ($\sigma/\mu = 20\%$).

B. Robustness at Ultra-Low Voltages

Among normal flip-flop sampling, ReRAM write, and ReRAM read operations, the ReRAM read operation is the most critical one. Indeed, studies have shown that normal operation of CMOS flip-flops can be robust in the sub-$V_{\rm T}$ domain [22]. In addition, in the present case, the write operation uses an elevated supply voltage of 2.4 V and, therefore, leads to a reliable operation.

Effectiveness of Low-Voltage Optimizations (NVFF-0 → NVFF-I): The effectiveness of the proposed low-voltage optimization techniques is investigated by comparing the read reliability of NVFF-0 and NVFF-I. This analysis is carried out in the near-$V_{\rm T}$ domain (at 0.8 V) and in the sub-$V_{\rm T}$ domain (at 0.4 V), as well as for different values of $\sigma(\text{HRS}) = \sigma(\text{LRS})$.

An appropriate metric to assess the read robustness is the initial discharge current ($I_{\rm read}$) flowing through the two branches of the slave latch, right after the de-assertion of the EQUALIZE signal. Fig. 5(a) shows the distributions of $I_{\rm read}$ at 0.4 V for NVFF-I, with different standard deviations of HRS and LRS. For a well-controlled, repeatable ReRAM process with $\sigma(\text{HRS}) = \sigma(\text{LRS}) = 40\ \text{k}\Omega$, the discharge current flowing through the branch containing the ReRAM in the HRS is clearly lower than the current flowing through the other branch (non-overlapping $I_{\rm read}$ distributions). This results in zero read failures out of 1000 Monte Carlo runs, as shown in Fig. 5(c). However, for a less precisely controlled ReRAM process with higher standard deviation of the resistance ($\sigma(\text{HRS}) = \sigma(\text{LRS}) = 160\ \text{k}\Omega$), the distributions of $I_{\rm read}$ start to overlap, which results in a small read failure probability.

Fig. 5(b) shows the tremendous improvement in read robustness enabled by the low-voltage optimization techniques, i.e., by matching of the PDNs through the insertion of dummy transistors as well as transistor upsizing. More precisely, the figure shows the read failure probability (computed based on 1000 MC trials) versus the presumed values of $\sigma(\text{HRS})$ and $\sigma(\text{LRS})$, for a supply voltage of 0.8 V. Comparing NVFF-I with NVFF-0, the dummy transistors and the transistor upsizing decrease the read failure probability from 13% down to almost 0% for the presumed worst case ReRAM process ($\sigma(\text{HRS}) = \sigma(\text{LRS}) = 20\% \times \mu(\text{LRS})$).

Comparison of NVFF-I—NVFF-III, and Single-Ended vs. Differential: Fig. 5(c) and (d) illustrate the robustness of NVFF-I, NVFF-II, and NVFF-III for operation at near-$V_{\rm T}$ and sub-$V_{\rm T}$ voltages, respectively. The differential NVFF-I and

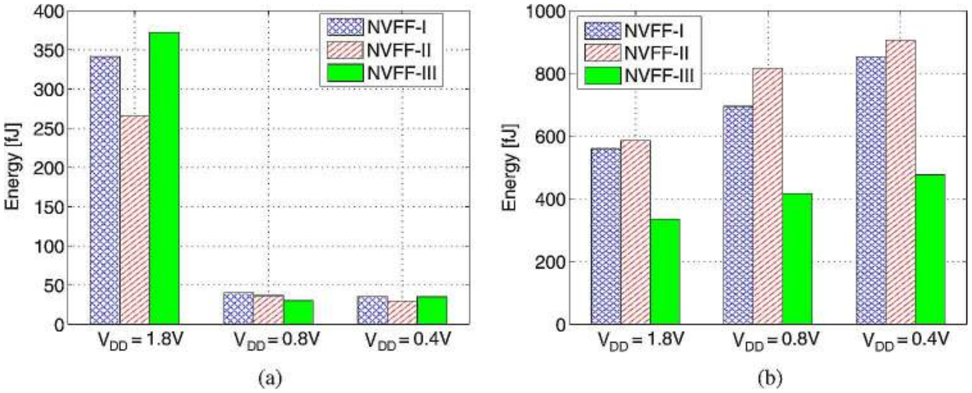

Fig. 6. (a) Read energy; and (b) write energy comparisons for different main supply voltages V_{DD}. Note that the voltage is always risen to 2.4 V for ReRAM write.

NVFF-II topologies exhibit a much lower read failure probability than the single-ended NVFF-III topology. In NVFF-III, accuracy is also needed for the current source (transistor M3), to create an appropriate drop across the ReRAM device. If the value of the generated current deviates from its nominal value, the sense inverter might switch erroneously, giving rise to read failures. Conversely, in NVFF-I and NVFF-II only relative accuracy is needed. This is why they are more robust than NVFF-III, both at near-V_{T} and sub-V_{T} supply voltages. For a near-V_{T} supply voltage, NVFF-I and NVFF-II exhibit no read failures for $\sigma(\mathrm{HRS}) = \sigma(\mathrm{LRS}) \leq 10\% \times \mu(\mathrm{LRS})$, whereas NVFF-III exhibits a read failure rate of almost 4% under the same conditions. Briefly, a differential structure using two complementary programmed ReRAM devices is more robust than a single-ended structure employing a single ReRAM device.

Finally, NVFF-II reads more reliably in the sub-V_{T} domain (at 0.4 V) than NVFF-I, since the former has fewer transistors and therefore less sources of mismatch in the PDN. In addition, NVFF-II has a slightly smaller area cost than NVFF-I since it uses two transistors less. In conclusion, the differential NVFF-II is selected as the best-practice circuit for robust operation at ultra-low voltages in the sub-V_{T} domain, whereas the smaller, single-ended NVFF-III circuit is a viable option only down to the near-V_{T} domain.

C. Energy Dissipation

Fig. 6(a) and (b) show the energy dissipation per single read and write operation, respectively, of the NVFFs at different supply voltages. The main power supply V_{DD} (used for read and normal operations) is swept from 1.8 V to 0.4 V. Prior to a write operation, the power supply is always risen to 2.4 V. For each V_{DD}, the read operation is performed at maximum speed, with the minimum required pulse widths for the $\mathrm{EQUALIZE}$ and READ signals, as given in Fig. 3(b) for NVFF-I and NVFF-II and in Fig. 4(b) for NVFF-III. We found that initially, voltage scaling from 1.8 V to 0.8 V considerably reduces the read energy; however, the active energy benefits of further voltage scaling are offset by longer pulse widths at 0.4 V (in the order of μs instead of tens of ns) and the associated integration of leakage currents.

Circuit NVFF-II can read faster than circuit NVFF-I thanks to the simpler PDN with a considerably reduced number of stacked transistors (only two instead of four). In fact, thanks to the lower resistance pull-down path, the minimum READ pulse width for NVFF-II is reduced by almost 2× compared to NVFF-I (see Fig. 4(b)), which leads to read energy savings in the sub-V_{T} regime where leakage plays a significant role. Note that the steady current flow during the entire duration of the READ pulse in the single-ended NVFF-III topology leads to a similar read energy compared to the differential topologies.

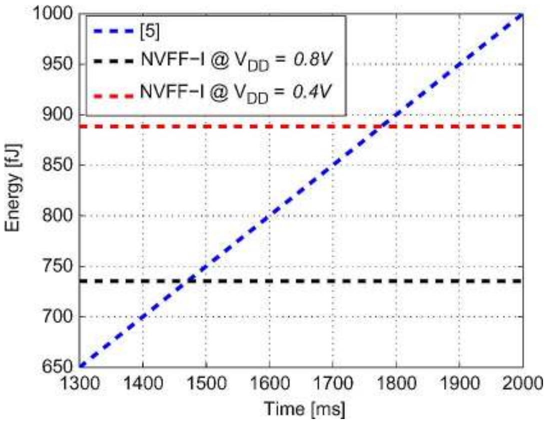

Fig. 7. Energy break-even sleep time of NVFF-I w.r.t. low-leakage CMOS latch [23].

Regarding the write energy, the supply needs to be risen by 0.6 V and 2 V for a write operation, for a main V_{DD} of 1.8 V and 0.4 V, respectively. As illustrated in Fig. 6(b), the lower the main V_{DD} is, the larger the transition to 2.4 V, and the larger the write energy. As a main insight from Fig. 6(b), we conclude that the single-ended NVFF-III topology exhibits around half the write energy compared to the differential topologies, irrespective of the main supply voltage. In other words, the write energy is approximately linear to the number of ReRAM devices in the NVFF topology.

Irrespective of the NVFF topology, the write energy is always higher than the read energy. In fact, the write energy mostly depends on the ReRAM stack and cannot be improved by voltage scaling. As opposed to this, the read energy can be significantly lowered by voltage scaling, and becomes small compared to the write energy for low-voltage operation. The total write+read energy is approximately the same for both NVFF-I and NVFF-II, whereas this total energy is reduced to around half of the NVFF-III topology.

Comparison With Volatile CMOS Storage Element: Since most ReRAM technologies are still immature, due to partially missing energy reports in the literature, and due to a multitude of different ReRAM technologies, we prefer to compare our approach with conventional, volatile, low-leakage CMOS storage elements. To this end, the total read+write energy of NVFF-I (or, equivalently, NVFF-II) is compared with the energy of a leakage-optimized latch in a mature CMOS technology [23]. The proposed NVFF topologies require a constant energy cost for sleep preparation and wake-up, i.e., the total read+write energy, wich is independent of the sleep time. In contrast, the energy cost resulting from leakage currents increases with the sleep time for the conventional CMOS latch.

Fig. 7 shows that the proposed NVFF-I (or NVFF-II) circuit is more energy efficient for sleep times longer than 1.47 s and 1.77 s for operation at 0.8 V and 0.4 V, respectively, compared to the low-leakage CMOS latch.

V. Discussions and Conclusions

In this paper, we have proposed several non-volatile flip-flop (NVFF) circuits based on ReRAM technology, and compared their energy efficiency and robustness for operation at ultra-low voltages. These circuits leverage the use of sub-V_T operation enabling energy-efficient VLSI systems with zero-leakage sleep states. The manufactured oxide stacks switch their resistive state with a 0.18 μm CMOS-compatible voltage of 2 V and under a low current compliance of 10 μA. For all proposed NVFF topologies, the write energy is mostly ReRAM technology dependent. Conversely, thanks to sub-V_T and near-V_T operation, the read energy is brought down to 5.4% of the total read+write energy (in case of differential NVFF circuits). Under voltage scaling, the read energy improvement saturates between near-V_T and sub-V_T due to the increase in the READ pulse width. For the differential NVFF circuits, Monte Carlo simulations demonstrate a robust read operation at 0.4 V, accounting for parametric variations in both ReRAM devices and MOS transistors. Robustness can be further increased by having a larger ratio between the high and low resistance values of the ReRAM device.

Differential NVFF circuits with two complementary programmed ReRAM devices are more robust than their single-ended NVFF counterpart using only one ReRAM device, especially for operation at low voltages. However, the single-ended topology is around 2× more energy efficient compared to the differential topologies. A differential NVFF circuit is required to ensure robust sub-V_T operation, while the more energy-efficient single-ended topology is a viable option only for operation at nominal or slightly scaled voltages. Among the considered differential circuits, it is clearly beneficial to connect the ReRAM read circuit to the internal nodes of the slave latch rather than to its current sink. In fact, the former architectural variant leads to smaller area (it avoids two transistors otherwise used for matching of PDNs), increased robustness at sub-V_T voltages (better matching due to less devices in PDN), higher ReRAM read speed (lower equivalent PDN resistance), and comparable total read+write energy.

In summary, the differential NVFF-II topology (with the ReRAM read circuit connected to the internal nodes of the slave latch) is selected as the best-practice circuit for robust operation at ultra-low voltages in the sub-V_T domain, whereas the more energy-efficient and smaller, single-ended NVFF-III circuit is a viable option only down to the near-V_T domain.

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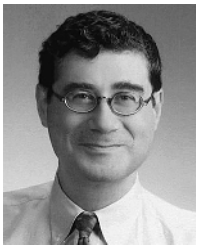

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