The Engineering of BSIM for the Nano-Technology Era and Beyond

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ABSTRACT

This paper presents the current status of the forth generation BSIM model and issues of modeling CMOS based devices with nanometer dimensions. Due to the divergence of device structures in sub-0.1μm gate length, it is more and more difficult to describe the device physics accurately and efficiently. In order to have a practical model with enough flexibility to accommodate a wide variety of technologies, vigorous engineering techniques have to be incorporated. At the same time, modern computer program techniques including numerical differentiation and parallel model evaluation are considered to shorten model development time. The tradeoffs between computation efficiency and development time will be discussed. Methodologies to design next generation extendible device models with advanced computer programming techniques are proposed.

Keywords: CMOS Device, Circuit Simulation, Device model, SPICE, BSIM

1 INTRODUCTION

Device models play very important roles in the advancement of CMOS technology and they appeared everywhere from fabrication technology development to IC design and manufacturing as shown in Fig. 1. Since the development of BSIM1 [1] one and a half decades ago, the BSIM family has entered its forth generation with the release of BSIM4 in the year 1999. In the course of BSIM effort, BSIM3 version 3 was acknowledged as the world's first and only industry-standard public-domain device model by the EIA Compact Model Council (CMC) [2]. BSIM4 offers many improvements over BSIM3 with a lot of new and important physical effects included. The model has been experimentally verified down to some sub-0.1μm dimensions. While BSIM4 has demonstrated the feasibility to model sub-0.1μm devices, the way to a "perfect" universal model is still very far away. On the other hand, the scaling trend as defined by the SIA roadmap continues in a very rapid pace with the introduction of new device structures. Therefore, providing a generic model that can keep up with the SIA roadmap and fit all different technologies is more challenging than ever and requires new innovations.

It should be noted that the most widely adopted modeling approach is based on the FORTRAN style programming framework developed a few decades ago, despite the tremendous changes in silicon technology and computer programming methodologies. Before further developing more advanced physical models, we intended to take a more high-level overview on the priorities and tradeoffs in various modeling requirements. We hope to come up with a better tactic and strategy for more long-term extendible and reusability development effort. The investigation will facilitate the planning development of the fifth generation of device model in the BSIM family.

2 REQUIREMENTS OF A GOOD MODEL

A model is a mathematical description of the device behaviors. Different interest groups used the model for different purposes and thus, push for different priorities in model developments. For example, a device engineer normally wants the model to be physical so that all the device physics are represented. On the other hand, circuit designers set higher priority for simplicity (for hand calculation) and efficiency in computation. Some of these requirements are summarized in Table 2.

In the BSIM development, emphasis has been placed on mainly 3 aspects: physical formulation, computational efficiency and ability to accommodate a larger variety of technologies. Physical formulation provides the predictive capability of the model that can be used beyond simple circuit simulations. The BSIM models have been frequently used to predict circuit performance at different technology generations, and a web-based technology performance prediction platform based on BSIM has been developed [3]. In addition, a physical based approach can be used for statistical simulation, which is getting more and more important due to the more significant device-to-device variation in nanometric devices.

To achieve high computational efficiency, smoothing functions are introduced since BSIM3v3 to ensure the smoothness and continuity of the currents and derivatives (conductances) for fast convergence in the SPICE engine. The formulation is an engineering solution that slightly compromised the accuracy in the small transition regions between 2 operation regions. This minor imperfection has been compensated by introducing fitting parameters to refine the curves in the transition regions.

Fitting of device data from different technologies across the industry with high accuracy is the most challenging task. However, it is one of the most essential features in an industrial standard model and represents the final test of the practicality of the model. BSIM3/4 achieves the task by introducing a lot of parameters to allow engineers to adjust the simulated *I-V* characteristics. The tradeoff is the continuous increase in the number of parameters with time as shown in Fig. 2. The trend is similar to the increase in circuit and device complexity with time as predicted by the Moore's law, to which model complexity has to follow. To deal with these large number of model parameters, efficient and powerful device extraction tools are essential.

3 CURRENT STATUS OF BSIM4 MODEL

The development of BSIM4 has attempted to maintain backward compatibility with the BSIM3v3, which is currently the industrial standard model. At the same time, a number of important advanced effects are introduced to cope with the rapidly shrinking MOSFETs. These include quantum mechanical charge thickness model, gate dielectric tunneling current model, holistic thermal noise model, substrate resistance model and others. In addition, a number of the improvements including the dynamic reference are included. The quantum mechanical (QM) model accounts for the finite inversion/accumulation layer thickness as shown in Fig. 3. With the QM model, the accuracy of the *C-V* is significantly improved as shown in Fig. 4. Experimental verification from the *I-V* model is underway, but similar benefit is expected.

The gate current model allows the simulation of devices with ultra-thin gate dielectric. In this model, 3 tunneling paths are included as shown in Fig. 5. The model works equally well for silicon dioxide and silicon nitride down to 1.2nm oxide thickness as shown in Fig. 6.

A new Holistic Thermal Noise Model is also introduced in BSIM4. In this model, the channel of a MOSFET is divided into small segments and each contributes a mini-noise source as shown in Fig. 7. The impact of each noise source is magnified through the tranconductances to the gate (G_m) and body (G_{mb}). These noise sources are combined to give the equivalent thermal noise as in Fig. 7. Excellent agreement between model prediction and experimental data is found as shown in Fig. 8.

To address the need for high-speed circuit, BSIM4 has improved its intrinsic channel resistance model (Fig. 9) together with the addition of electrode resistances (Fig. 10). With the new addition, MOSFET parameters are well modeled up to the cutoff frequency as shown in Fig. 11.

One major criticism of BSIM is the asymmetry between the source and drain due to the source reference structure. However, preserving the source reference is important for compatibility with the existing design methodology. To fix the asymmetry problem, a dynamic reference approach that smoothes out the absolute function $|V_D\text{-}V_S|$ is introduced. Using the dynamic reference, all derivatives become continuous at V_{DS}=0V as illustrated by $C_{GD,GS}$ in Fig. 12.

4 EXTENDING BSIM IN THE NANO-ERA

BSIM4 is a comprehensive model for existing technologies. However, it is anticipated that variations technologies used in the nanometric dimension will be more significant. The next generation modeling methodologies should be more proactive and should provide a simple methodology to adopt new features in the early development stage. An example is the gate-tunneling model to be used for different high-k dielectrics introduced. Instead of describing all the physical effects into a single equation, they should be broken up into modules as shown in Fig. 13. All internal nodes should be generated with a set of given parameters. As some features maybe mutually exclusive in real applications, users (or parameter extractors) can pick the important effects to be included in the model, or even add their own effects.

The tradeoff between model development time and simulation time is another issue worth considering. A good example is the need to recalculate all analytical derivatives even a minor change is introduced into the I-V equations. As a result, most of the valuable model development time will be spent on doing algebra and debugging. With the modern computer capability, numerical differentiation has almost become a standard math library function and should be used. A minor drawback is the slight increase in computation time. But the real bottleneck in speed is the use of traditional programming methodology in a modern computer era. The speed of computation can be increased by methods such as parallel evaluation that is particularly suit for numerical differentiation.

Another important issue that has always been overlooked is the job division between different simulation platforms in the CAD hierarchy. Modeling has been mostly done independently from other CAD tools. However, as device performance become more and more layout dependent, the job division between device model and layout extraction tools should be revisited.

5 CONCLUSION

BSIM4 is a comprehensive model than includes lots of advance features to cope with technology development for a number of years ahead. To extend the lifetime of BSIM family further down the timeline, a more revolutionary approach should be taken.

ACKNOWLEDGEMENT

BSIM research was conducted by past and present team members at UC Berkely with support by SR, EIA Compact Model Council, TI, Conexant, IBM, MICRO, DARPA and also Hong Kong RGC with a earmarked grant.

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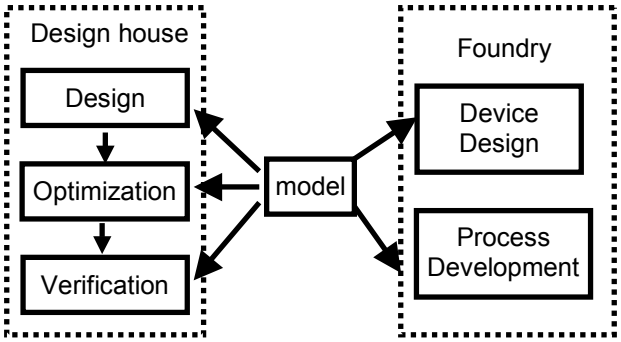


Fig. 1. MOSFET model acts as a bridge between designers and chip foundry

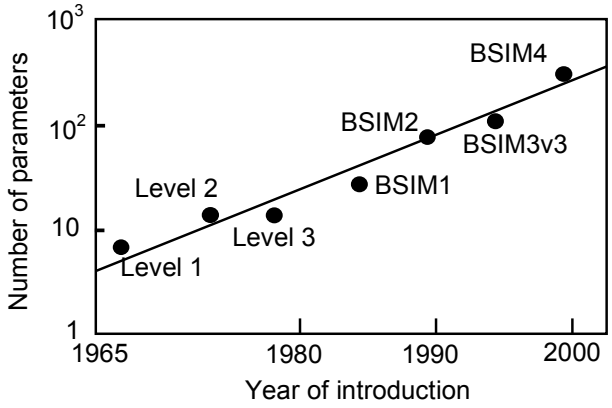


Fig. 2. The increase of MOSFET model parameters

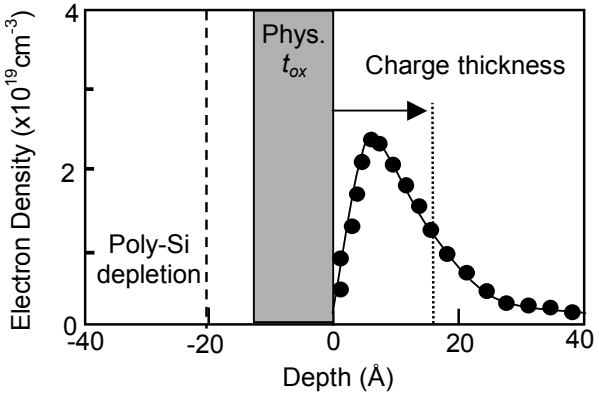


Fig. 3. Finite charge thickness in MOSFET

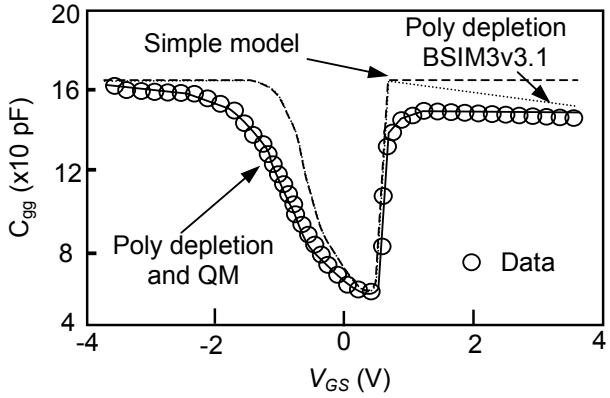


Fig. 4. C-V after including charge thickness model

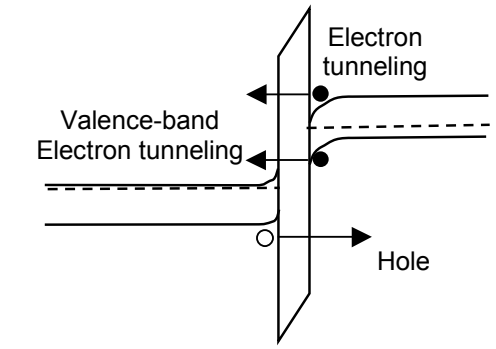


Fig. 5. Gate tunneling current components

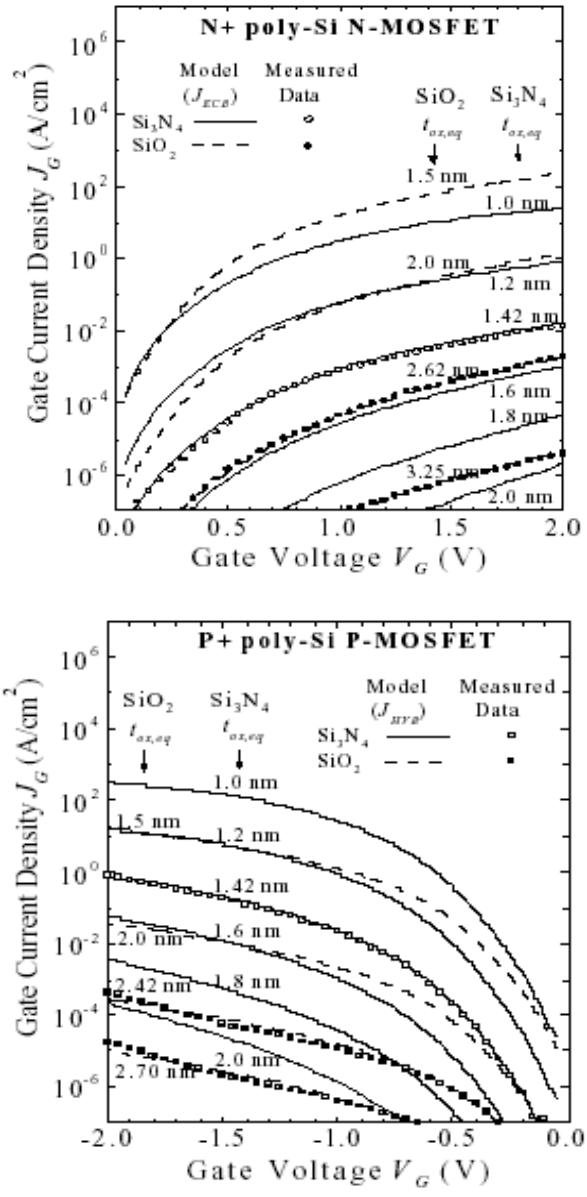


Fig. 6. Result of the gate tunneling current model

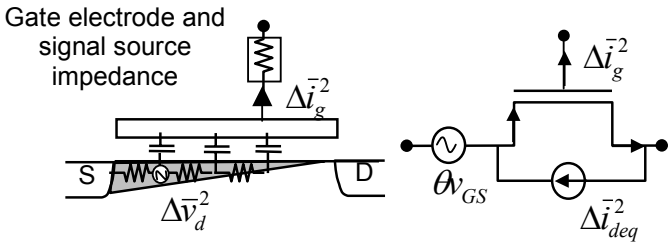


Fig. 7. The Holistic thermal noise model in BSIM4

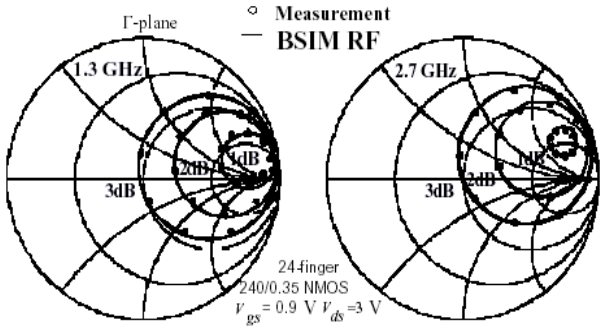
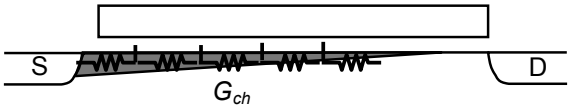


Fig. 8. Verification of Holistic Thermal Noise model



$$R_{ii} = \frac{R_{ch}}{\eta} = \frac{V_{DS}}{\eta I_{DS}} \text{ in triode region}$$
$$= \frac{V_{DSat}}{\eta I_{DS}} \text{ in saturation}$$
$$\eta \approx 14 \text{ as determined by 2-D simulation}$$

Fig. 9. Intrinsic channel resistance model in BSIM4

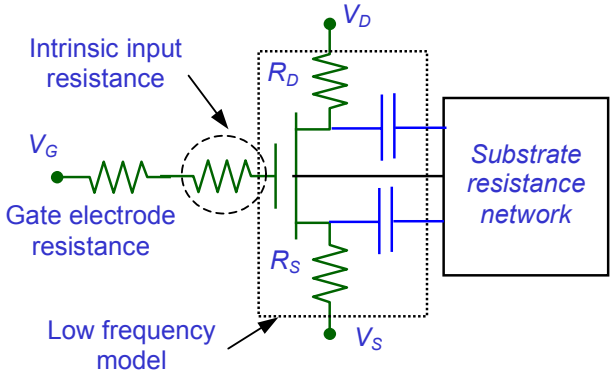


Fig. 10. External electrode resistance model in BSIM4

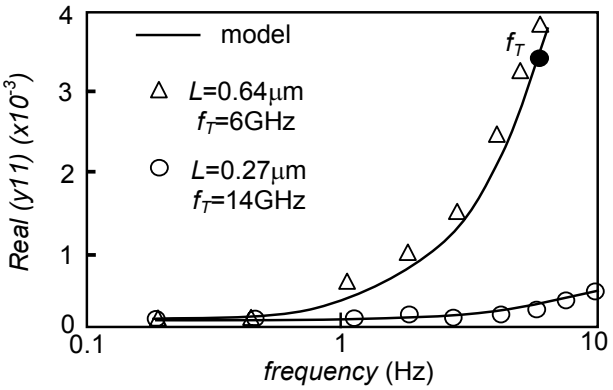


Fig. 11. Input resistance from the RF model

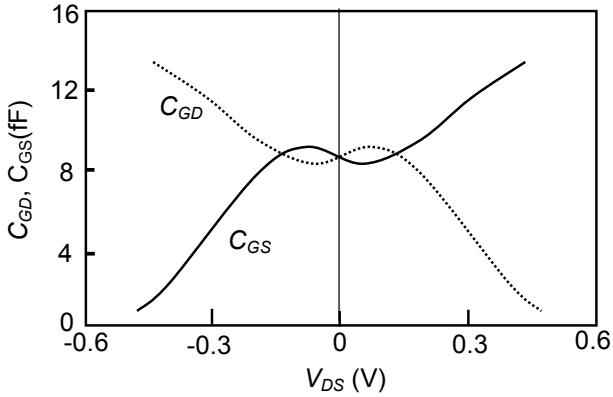


Fig. 12. Continuous C_{GD} and C_{GS} with dynamic reference

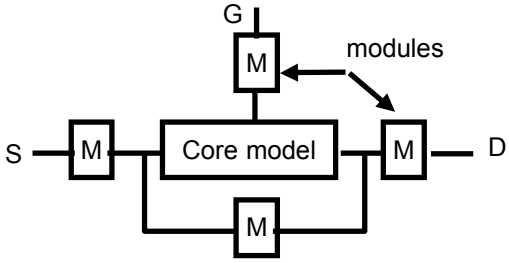


Fig. 13. Model structure with dynamic internal nodes

Features	Targeted group
Accurate physics	Device engineers
Computational efficiency	IC designers
Actual data fitting accuracy	IC designers, foundry
Fit different technology	CAD vendor, foundry
Simplicity	IC designers
Short development time	Model developers and CAD vendors
Backward compatibility	IC designers, CAD developers

Table 1: Model requirements expected from different interest groups