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Engineering nonlinearity into memristors for passive crossbar applications

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Although TaO_x memristors have demonstrated encouraging write/erase endurance and nanosecond switching speeds, the linear *current-voltage* (*I-V*) characteristic in the low resistance state limits their applications in large passive crossbar arrays. We demonstrate here that a TiO_{2-x}/TaO_x oxide heterostructure incorporated into a 50 nm× 50 nm memristor displays a very large nonlinearity such that $I(V/2) \approx I(V)/100$ for $V \approx 1$ volt, which is caused by current-controlled negative differential resistance in the device.

Resistive random access memory (RRAM or ReRAM, which is one physical embodiment of a memristor[1]) is viewed as a promising emerging technology to compete with charge-storage devices at feature sizes smaller than 25 nm.[2,3] Accordingly, a significant amount of research effort has been invested world-wide and dramatic progress has been made both in understanding the working mechanisms[4–24] and improving the switching properties[25–31] in the last decade. These memory cells are intended to be used in stacked crossbar arrays to satisfy the demand for increasing memory density,[32,33] and thus these ambitious architectures need to eschew select devices such as transistors or diodes to isolate a memory cell for reading and writing/erasing. A variety of device concepts and structures have been introduced recently to negate the need for select devices, including integrating metal-insulator-transition (MIT) materials,[34–36] building an intrinsic rectifier[37] into the memristors, and stacking two identical switches head-to-head to form a complementary device.[32,37] These schemes share a common goal, i.e., increasing the nonlinearity or asymmetry of the current voltage (*I-V*) characteristic of the device, especially in the low resistance state. Among the resistance switches reported to date, TaO_x-based devices have demonstrated encouraging electrical performance, including high endurance,[24,31] high switching speed,[38] low energy operation,[39,40] and forming-free.[40] However, these memristors normally exhibit a linear *I-V* relation in the low resistance state,[24,31] which limits their application in large crossbar arrays. Here, we show one scheme to engineer nonlinearity into the linear *I-V* of TaO_x-based devices: 50 nm× 50 nm $Pt/TaO_x/TiO_{2-x}/Pt$ oxide heterostructure devices display a large nonlinearity along with a sub 50 μA switching current. We then analyze the electrical properties of each interface in the device stack to track down the one responsible for the nonlinearity. The physical origin of the high nonlinearity is also briefly discussed.

Figure 1(a) is a schematic illustration of a crossbar array and Fig. 1(b) is an atomic force microscope (AFM) image of a 50 nm half-pitch crossbar array with electrodes fabricated by nanoimprint lithography. The Ta and Ti oxide thin films were sputter-deposited from Ta_2O_5 and Ti_4O_7 targets, respectively. The compositions of the oxide films in the devices were close to those of the oxide targets in the as-prepared state but changed from these nominal values after electrical operations.[15,40] Pinched hysteresis switching *I-V* loops typical of these nanodevices are shown in Figs. 1(c) and 1(d), where a positive voltage on the top electrode (TE) switches the devices ON (set, red loops) and a negative voltage on the TE switches the devices OFF (reset, blue loops). The bottom electrode (BE) was always grounded and the quasi-DC sweep voltages were applied on the TE in all the electrical measurements reported here. The insets to Figs. 1(c) and 1(d) are the semi-log plots of the same data as those in linear-linear plots. The device with a stack structure of Pt (BE)/TaO_x/Ta (TE) exhibits the *I-V* loop shown in Fig. 1(c), where the ON state has a linear *I-V* characteristic. In contrast, the device with a stack structure of Pt (BE)/TaO_x/TiO_{2-x}/Pt (TE) exhibits the *I-V* loop shown in Fig. 1(d), where the *I-V* curve of the ON state is highly nonlinear. A quantitative measure of nonlinearity can be defined as the ratio of the current level at V to that at $V/2$, i.e., $I_V/I_{V/2}$, where V is either the writing or reading voltage. This definition yields a ratio of 2 for the linear device shown in Fig. 1(c) and a ratio of about 100 for the nonlinear device shown in Fig. 1(d). A lower nonlinearity means a large current level at $V/2$ (Fig. 1(c)), while a higher nonlinearity means a small current level at $V/2$ (Fig. 1(d)).

The significance of $I_{V/2}$ is exemplified in the passive crossbar array illustrated in Fig. 1(a), where no extrinsic select device is used and the intrinsic nonlinearity of the memristor at each crosspoint is utilized to minimize the "sneak path" currents. A common electrical addressing scheme for either a reading or writing operation is to apply $V/2$ to one electrode and $-V/2$ to the other electrode of the required memristor, resulting in a total voltage drop of V across the selected device (red in Fig. 1(a)). Simultaneously, this leads to a voltage drop of $V/2$ on all the other memristors sharing a common row or column electrode (pink in Fig. 1(a)) with the selected device. These memristors are usually called half-selected devices (yellow in Figure 1(a)) in the crossbar array. Therefore, in addition to the current flow through the selected memristor, i.e., I_V, there are sneak path currents flowing through the half-selected memristors and some unselected memristors in the crossbar array. One such current path ($I_{V/2}$) is drawn in yellow in Fig. 1(a). The

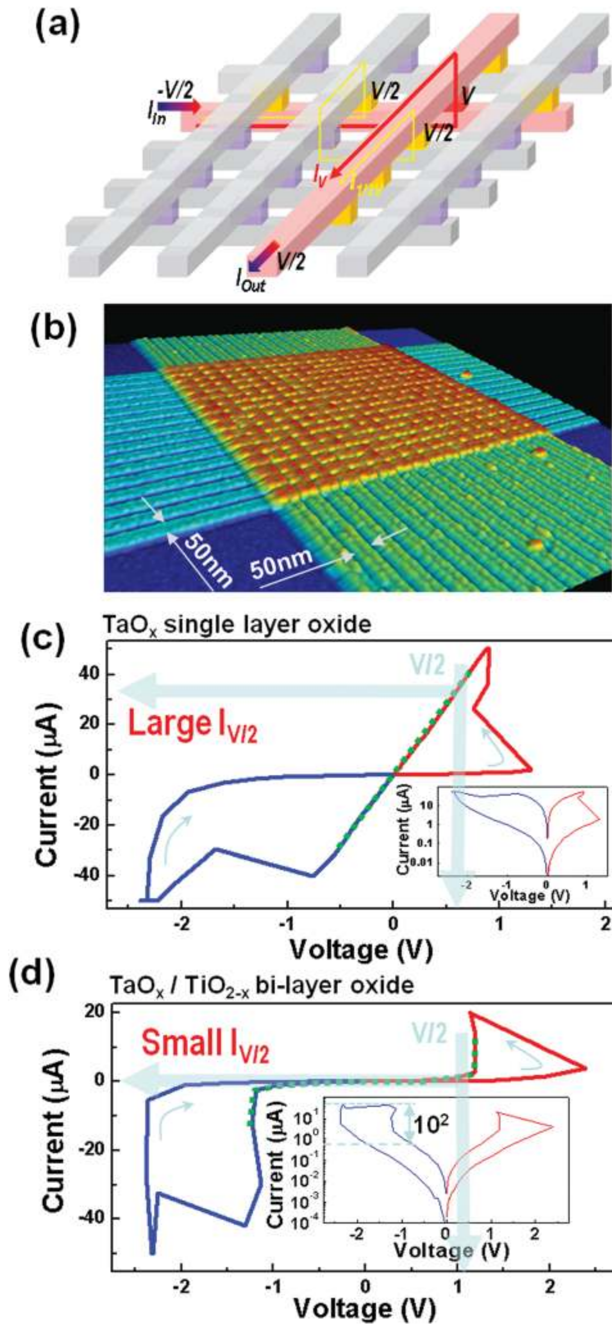

FIG. 1. (Color) Crossbar array and current voltage loops of nanodevices. (a) Schematic illustration showing the sneak path current through the half-selected memristors and (b) atomic force microscopy image of a crossbar array with 50 nm half-pitch fabricated by nanoimprint lithography. (c) Switching loop from a Pt/TaO_x/Ta 50 nm × 50 crosspoint device, showing linear *IV* curve in the ON state. (d) Switching loop from a Pt/TaO_x/TiO_{2-x}/Pt 50 nm × 50 nm crosspoint device, showing nonlinear *IV* curve in the ON state.

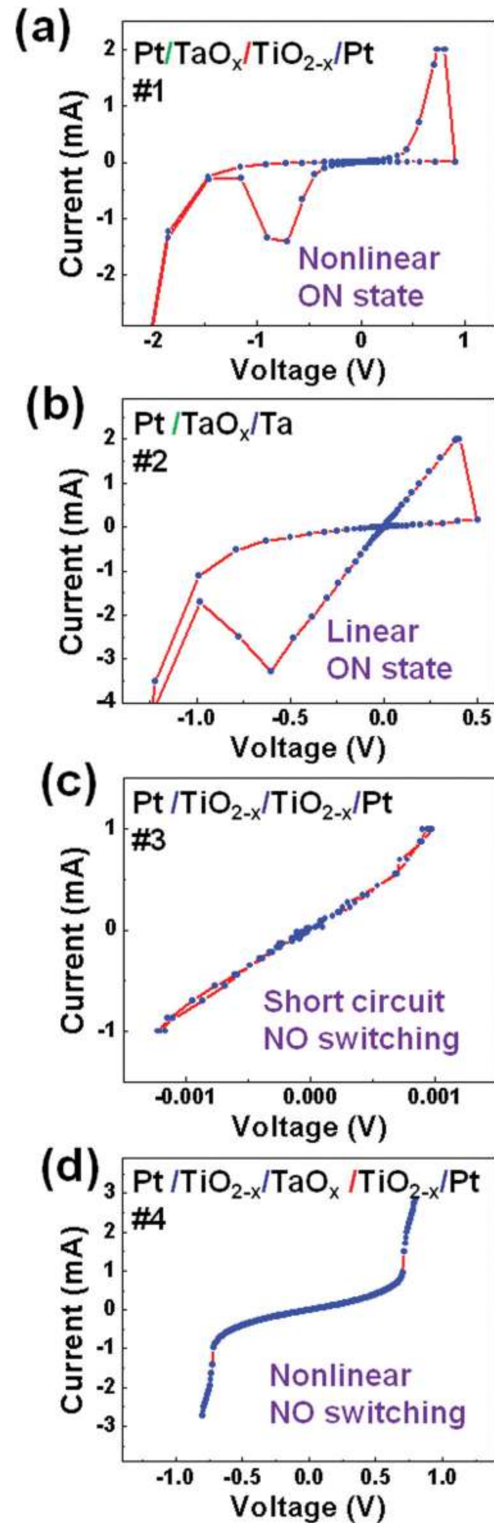

FIG. 2. (Color) Identification of the nonlinearity location by comparing a set of samples with different stack structures but sharing some identical layers. The TiO_{2-x}/TaO_x bi-layer oxide is responsible for the nonlinearity. All the TiO_{2-x} layers are 15 nm and TaO_x layers are 7 nm. Bottom Pt layers are 15 nm and the top Pt layers are 30 nm.

practical size of the crossbar array is thus limited by the sneak path currents, which can saturate the driving circuitry and generate unwanted Joule heating during writing/erasing operations. In addition, sneak paths limit the reading operation because of the large signal to background current level. The ON state is especially relevant because large sneak path currents run through those devices because of their relatively lower resistance. The relevance of nonlinearity can be seen from Figs. 1(c) and 1(d); the linear memristor exhibited $I_{V/2}$ of several tens of μA while that of the nonlinear nanodevice was less than 1 μA. An intrinsic nonlinearity of 100 in a memristor could enable a passive crossbar array with up to 1000 rows and columns, depending on the actual driving and sensing circuitry and the procedure used for writing and reading. Therefore, memristors with high nonlinearity are desirable for large crossbar arrays that in turn yield very high memory density.

We now examine which part of the device stack was responsible for the nonlinearity. We fabricated a set of four devices with different stack structures but sharing some identical layers. These crosspoint devices were fabricated with a shadow mask process at the micron scale to avoid exposing device interfaces to any chemical contamination during lithography and obtaining interfaces with minimum contamination for a clean comparison study. The stack structures of the four devices are: #1 Pt (BE)/TaO_x/TiO_{2-x}/Pt (TE), #2 Pt (BE)/TaO_x/Ta (TE), #3 Pt (BE)/TiO_{2-x}/TiO_{2-x}/Pt (TE), and #4 Pt (BE)/TiO_{2-x}/TaO_x/TiO_{2-x}/Pt (TE), where the TaO_x layers were 7 nm and sputter-deposited under the same experimental run for all four samples and the TiO_{2-x} layers were 15 nm and also sputter-deposited under the same experimental run for all four samples. The second TiO_{2-x} layers for samples #3 and #4 were deposited together. The Pt BE and the Pt TE for all the samples were 15 nm and 30 nm, respectively. A 50 nm sputter-deposited Ta film was used as the TE for sample #2, since it was found previously that Pt/TaO_x/Pt devices had a very poor yield, but those that switch behaved similarly to Pt/TaO_x/Ta devices. The typical *I-V* curves of $5\,\mu m \times 5\,\mu m$ devices from these four samples are presented in Fig. 2. The microdevice #1 with a stack of Pt/TaO_x/TiO_{2-x}/Pt shows a qualitatively similar nonlinear switching behavior as the nanodevice with the same stack structure but with a much higher current level. Interfaces have been shown to play a crucial role in various multilayered switching devices.[4,5,10] There were three different interfaces in the above nonlinear memristor: Pt/TaO_x, TiO_{2-x}/Pt, and TaO_x/TiO_{2-x}. Samples #2, #3, and #4 were used to identify the *I-V* characteristic of each of the three interfaces. Sample #2 with a stack of Pt/TaO_x/Ta showed a linear *I-V* characteristic in the ON state (Fig. 2(b)) as did its nanoscale counterpart shown in Fig. 1(c). Our previous studies have shown that the TaO_x/Ta interface is quite conductive and not switchable; the memristive switching occurs near the Pt/TaO_x interface.[24,40] Sample #3 with two layers of TiO_{2-x} but no TaO_x layer exhibited an effective short circuit, as shown in Fig. 2(c). This demonstrates that the TiO_{2-x} layer was very conductive and the Pt/TiO_{2-x} interface was ohmic, which agreed with the fact that the non-stoichiometric TiO_{2-x} layer grown here is metallic at room temperature. Sample #4 with the stack structure of Pt/TiO_{2-x}/TaO_x/TiO_{2-x}/Pt did not switch but did exhibit a nonlinear *I-V* curve. This further confirms that a TaO_x bulk layer itself does not generate the observed switching behavior and the Pt/TaO_x interface region is responsible for the memristive switching. From sample #3, it is already known that the Pt/TiO_{2-x} interface is ohmic and very conductive; thus the nonlinearity of sample #4 must arise from the TiO_{2-x}/TaO_x interfaces, which should also be responsible for the nonlinearity observed in sample #1. We can then conclude that in the Pt/TaO_x/TiO_{2-x}/Pt nonlinear device, Pt/TaO_x is the switching region, TaO_x/TiO_{2-x} is the nonlinear component, and TiO_{2-x}/Pt is an ohmic contact.

We briefly discuss the physical origin of the nonlinearity of a TaO_x/TiO_{2-x} bi-layer structure. The *I-V* curve in Fig. 2(d) displays an apparent current-controlled negative differential resistance (CC-NDR),[41] which has been verified by the fact that putting sample #4 and a 1 nF capacitor in series

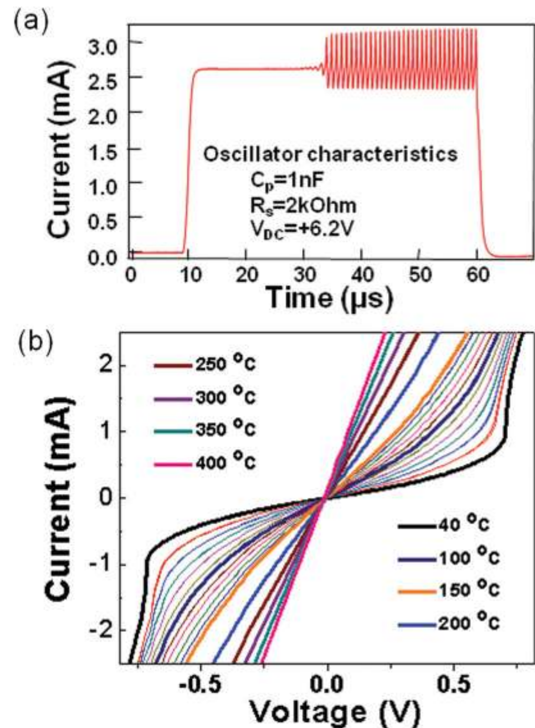

FIG. 3. (Color) The negative differential resistance property of the Pt/TiO_{2-x}/TaOx/TiO_{2-x}/Pt device. (a) The oscillation from a oscillator formed by the Pt/TiO_{2-x}/TaOx/TiO_{2-x}/Pt device and a capacitor of 1nF. The driving voltage is 6.2 V and the series resistor is 2 K ohm. (b) Temperature dependence of the Pt/TiO_{2-x}/TaOx/TiO_{2-x}/Pt sample. *IV* curves at different ambient temperatures in 1×10^{-6} Torr vacuum.

with a DC bias voltage produces a van der Pol relaxation oscillator, as shown in Fig. 3(a). The temperature dependence of the Pt/TiO_{2-x}/TaO_x/TiO_{2-x}/Pt *I-V* characteristic is shown in Fig. 3(b), where the *I-V* curves were measured at different ambient temperatures in a vacuum of 1×10^{-6} Torr. The *I-V* curves became linear once the ambient temperature exceeded 200 °C.

As a bi-layer oxide hetero-junction, there is a band offset between the two oxide layers, which was measured to be around 0.8 eV by photoemission (data not shown). Since TiO_{2-x} is metallic at RT, the intrinsic property of the interface should be a Schottky-like metal/semiconductor contact. An intrinsic electro-thermal NDR effect may be possible at such an interface, in a manner similar to the observed CC-NDR observed in a bulk insulating material.[42] On the other hand, the local temperature around the conducting channel can be significantly higher than the rest of the device because of Joule heating.[8,15,40] Thus, it is possible that the interface between the two oxide layers was chemically altered at the high temperature. As a result, a new oxide phase (binary or ternary) may have developed at this interface. Metal-insulator-transitions have been observed in some Ti suboxides with a transition temperature of around 200 °C (Refs. 43–45). This could be one of the possible causes of the nonlinearity observed, which are presently under investigation.

In summary, we have engineered a large nonlinearity into TaO_x-based memristors. Both micron-scale and nanodevices with a stack structure of Pt/TaO_x/TiO_{2-x}/Pt have shown significant nonlinearity, which can enable large crossbar arrays without an extrinsic select device at each

crosspoint. The switching occurs near the Pt/TaO_x interface and the TaO_x/TiO_{2-x} bi-layer is responsible for the nonlinearity, which has been identified as CC-NDR. This approach may work with other oxide switches as well, such as HfO_x based devices, which also have promising electrical performance but linear *I*-*V* in the ON state.[46]

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