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Enhanced bias stress stability of a-InGaZnO thin film transistors by inserting an ultra-thin interfacial InGaZnO:N layer

Xiaoming Huang, Chenfei Wu, Hai Lu,^{a)} Fangfang Ren, Dunjun Chen, Rong Zhang, and Youdou Zheng

Jiangsu Provincial Key Laboratory of Advanced Photonic and Electronic Materials and School of Electronic Science and Engineering, Nanjing University, Nanjing 210093, China

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Amorphous indium-gallium-zinc oxide (a-IGZO) thin film transistors (TFTs) having an ultra-thin nitrogenated a-IGZO (a-IGZO:N) layer sandwiched at the channel/gate dielectric interface are fabricated. It is found that the device shows enhanced bias stress stability with significantly reduced threshold voltage drift under positive gate bias stress. Based on x-ray photoelectron spectroscopy measurement, the concentration of oxygen vacancies within the a-IGZO:N layer is suppressed due to the formation of N-Ga bonds. Meanwhile, low frequency noise analysis indicates that the average trap density near the channel/dielectric interface continuously drops as the nitrogen content within the a-IGZO:N layer increases. The improved interface quality upon nitrogen doping agrees with the enhanced bias stress stability of the a-IGZO TFTs. © 2013 AIP Publishing LLC. [http://dx.doi.org/10.1063/1.4805354]

Transparent amorphous indium-gallium-zinc oxide (a-IGZO) thin film transistors (TFTs) are being intensively investigated as a replacement for silicon-based TFTs to be used in active matrix displays as they could simultaneously offer high channel electron mobility, high optical transparency, low off-state leakage, and low processing temperature.^{1,2} However, the instability problem of a-IGZO TFTs remains as an obstacle to overcome for practical applications. For example, large threshold voltage drift (ΔV_{th}) upon electrical stress is commonly observed in a-IGZO TFTs, which is mainly caused by the high density trap states existing at the channel/gate dielectric interface.^{3,4} As a result, improving interface quality is the key to enhance the bias stress stability of a-IGZO TFTs.

Recently, several studies have reported that TFTs with nitrogen-doped a-IGZO channel could show enhanced ambient stability, which is explained that nitrogen atoms would partially replace inactive oxygen atoms within the device channel and thus reduce the oxygen absorption/desorption effect.⁵ Meanwhile, there is also evidence that nitrogen doping could suppress the generation of oxygen vacancies within a-IGZO thin films.⁶ However, doping the entire device channel with nitrogen would remarkably change the electrical characteristics of the TFTs, and there is also report that heavy nitrogen doping could undesirably reduce the optical bandgap energy of a-IGZO thin films.⁷ In this work, to take the advantage of the favorable passivation effect of nitrogen doping and avoid large performance drift of the TFTs, we propose a method to enhance the bias stress stability of a-IGZO TFTs by inserting an ultra-thin nitrogenated a-IGZO (a-IGZO:N) layer at the channel/gate dielectric interface. It is found that the stability of the fabricated a-IGZO TFTs is significantly enhanced under positive gate-bias stress, which is attributed to the reduction of interface defects or dangling bonds by nitrogen doping.

The back-gate a-IGZO TFTs studied in this work are fabricated on heavily doped n-type silicon substrate. A 200 nm SiO₂ gate insulator is first deposited by plasma enhanced chemical vapor deposition (PECVD) on wafer front side. A 5 nm a-IGZO:N inter-layer is then deposited by dc sputtering at room temperature, which is followed by deposition of 45 nm a-IGZO active layer. During the sputtering deposition, the Ar and O₂ flow rates are fixed at 36 sccm and 6 sccm, respectively, while the N₂ flow rate is selected to set between 0 and 6 sccm. The composition of the ceramic target used is In_2O_3 :Ga₂O₃:ZnO = 1:1:1 in mole ratio. The device active region is defined by optical photolithography and wet chemical etching. The source/drain contact electrodes consisting of Ti/Au (30/70 nm) bi-layer are deposited by e-beam evaporation and are further patterned by lift-off technique, resulting in a device channel width/length (W/L) of 100/ $20 \,\mu\text{m}$. Next, a 100 nm SiO₂ passivation layer is deposited by PECVD and patterned by wet chemical etching to open the source/drain contact holes. Finally, after deposition of the Ti/Au back-gate contact metal, the a-IGZO TFTs are annealed in air at 250 °C for 1 h. The inset of Fig. 1 shows a schematic of the fabricated a-IGZO TFT.

Figure 1 shows the transfer curves of the a-IGZO TFTs with (or without) thin a-IGZO:N insertion layer grown at different N₂ flow rate. Very low off-state leakage on the order of mid-10⁻¹⁴ A are observed. The corresponding electrical parameters of the TFTs, including threshold voltage (V_{th}), sub-threshold swing (SS), on/off current ratio (I_{on/off}), and field effect mobility (μ_{FE}), are summarized in Table I. The values of μ_{FE} in saturation region (V_{DS} = 10 V) and V_{th} are determined by linearly fitting the plot of I_{DS}^{1/2} versus V_{GS} using the following equation:

$$I_{DS} = \left(\frac{\mu_{FE}WC_{\text{ox}}}{2L}\right) (V_{GS} - V_{th})^2, \tag{1}$$

where W is the channel width, L is the channel length, and C_{ox} is the capacitance per unit area of the gate dielectric. It is

^{a)}Electronic mail: hailu@nju.edu.cn



FIG. 1. The transfer characteristics of the a-IGZO TFTs with a-IGZO:N insertion layer grown at different N_2 flow rate. The inset shows the schematic of the device structure.

clear that as the N₂ flow rate increases from 0 to 6 sccm, both the μ_{FE} and SS of the TFTs show no apparent change, while the V_{th} rises from 3.5 V to 5.2 V. The small up-shift of V_{th} suggests that the carrier concentration of the a-IGZO:N layer is reduced upon nitrogen doping.

The electrical stability of the a-IGZO TFTs is tested by positive gate-bias stress (PBS), in which the TFT under test is stressed at a high gate voltage of 20 V for a total time up to 5000 s while keeping both its source and drain electrodes grounded. Figures 2(a) and 2(b) selectively show the evolution of transfer curves as a function of PBS time for the devices with a-IGZO:N insertion layer grown at N2 flow rate of 0 sccm (i.e., conventional nitrogen-free device) and 6 sccm, respectively. For both stressed devices, the parallel shift of their transfer curves after PBS indicates that there is little degradation of their SS and $\mu_{\rm FE}$, which agrees with past reports that moderate bias stress would not considerably generate additional trap states within a-IGZO TFTs.3 Therefore, the positive ΔV_{th} observed for both devices should be caused by field-induced electron trapping in the gate dielectric and/ or at the channel/dielectric interface.⁸ Meanwhile, it is found that the TFT with a-IGZO:N insertion layer shows apparently better bias stress stability, which exhibits much smaller ΔV_{th} than that of the nitrogen-free device after PBS. As further listed in Table I, when the N₂ flow rate during a-IGZO:N deposition increases from 0 to 6 sccm, the positive ΔV_{th} of the a-IGZO TFTs with a-IGZO:N insertion layer continuously drops from 2.2 V to 0.7 V after 5000 s PBS.

To investigate the detailed chemical effect of nitrogen doping, the bonding properties of a-IGZO:N films are analyzed by x-ray photoelectron spectroscopy (XPS). Figures 3(a) and 3(b)

TABLE I. Extracted electrical parameters of the a-IGZO TFTs with a-IGZO:N insertion layer.

N ₂ (sccm)	$V_{th}\left(V\right)$	$\mu_{\rm FE} ({\rm cm}^2/{\rm Vs})$	SS (V/dec)	I _{on/off}	$\Delta V_{th}\left(V\right)$
0	3.5	8.6	0.53	$>10^{9}$	2.2
2	4.5	8.5	0.53	$> 10^{9}$	1.1
4	5.0	8.4	0.55	$>10^{9}$	0.8
6	5.2	8.6	0.55	$>10^{9}$	0.7



FIG. 2. Evolution of the transfer curves as a function of PBS time for the a-IGZO(/a-IGZO:N) devices fabricated using N_2 flow rate of (a) 0 sccm N_2 and (b) 6 sccm.

show the N 1s and O 1s XPS spectra of the a-IGZO:N films grown at N₂ flow rate of 0 sccm and 6 sccm, respectively. For the nitrogen-free a-IGZO film, the signal of Ga Auger at 396.7 eV is observed in the studied energy range (Fig. 3(a)). When the film is doped with nitrogen, the combined signal peak is shifted to higher energy, which is caused by the formation of Ga-N bonds centered at 397.8 eV (inset of Fig. 3(a)).⁹ Meanwhile, as shown in Fig. 3(b), Gaussian fitting is used to de-convolute the combined O 1s peak. The resulting sub-peaks centered at binding energies of 530.1 eV, 530.9 eV, and 531.9 eV are attributed to O^{2-} ions surrounded by metal atoms (In, Ga, and Zn), oxygen vacancies (O_V), and OH⁻ impurities, respectively.^{10,11} Thus, the area ratio of the O_V peak to the whole O 1s peak represents the relative quantity of oxygen



FIG. 3. (a) N 1s and (b) O 1s XPS spectra of the a-IGZO:N films.

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vacancies, which reduces from 32% to 24% when the a-IGZO film is doped by nitrogen. This result means that oxygen vacancies within the a-IGZO:N film are suppressed by nitrogen doping, which is likely caused by the formation of N-Ga bonds. In addition, since oxygen vacancies are the main source of free electrons in a-IGZO, this result also agrees with the up-shift of $V_{\rm th}$ for nitrogen-doped devices observed in Fig. 1.

Finally, to further investigate the mechanism of the stability improvement, low-frequency noise (LFN) measurements are conducted on the a-IGZO (N) TFTs fabricated using different N₂ flow rate. A group of 1/f noise plots measured in the linear region of the TFTs ($V_{GS}-V_{th}=6V$ and $V_{DS} = 1 \text{ V}$) are selectively shown in Fig. 4(a). It is clear that the overall normalized drain current noise spectral density (S_{iD}/I_D^2) as a function of frequency decreases with increasing N₂ flow rate, indicating that the average trap density within the device active region is decreased.¹² To verify the origin of the LFN, S_{iD}/I_D^2 measured at f = 20 Hz and $V_{DS} = 1 V$ is plotted as a function of $V_{GS}-V_{th}$ (the inset of Fig. 4(a)). The slopes of the 4 curves corresponding to samples fabricated with different N_2 flow rate are all around -2. According to the established LFN theory, a slope of -2 here indicates that the main source of LFN can be attributed to carrier number fluctuation, which is caused by tunneling of free-charge carriers into the oxide traps at the channel/gate dielectric interface region.^{13,14} Moreover, it has been suggested that if carrier number fluctuation is the dominant LFN



FIG. 4. (a) LFN spectra of the a-IGZO TFTs with a-IGZO:N insertion layer grown at different N₂ flow rate. The inset shows the log-log plots of S_{iD}/I_D^2 against V_{GS}-V_{th}. (b) Calculated average trap density as a function of gate voltage overdrive.

source, the average interfacial trap density within the gate oxide can be extracted as 15

$$N_{\rm t} = \frac{S_{iD}C_{ox}^2 WLf (V_{GS} - V_{th})^2 \gamma}{q^2 k T l_D^2},$$
 (2)

where q is the elementary electron charge, kT is the thermal energy, C_{ox} is the gate dielectric capacitance per unit area, and γ is the attenuation coefficient of the electron wave function within the SiO₂ dielectric. Here γ can be further described by the following equation:¹⁶

$$\gamma = \frac{4\pi}{h} \sqrt{2m^*\phi},\tag{3}$$

where m^* (~0.26 m₀) is the electron effective mass in SiO₂ dielectric, ¹⁷ h is the Planck's constant, and ϕ (~4.27 eV) is the tunneling barrier height for SiO2/IGZO interface.18,19 Figure 4(b) shows the calculated average trap density N_t as a function of gate voltage overdrive for the a-IGZO TFTs with a-IGZO:N insertion layer grown at different N2 flow rate, in which the oxide traps are considered to be situated close to the channel/dielectric interface and approximately have uniform distribution in energy.^{15,16} It is found that N_t continuously drops from low- 10^{19} to mid- 10^{18} cm⁻³ eV⁻¹ as the N₂ flow rate during a-IGZO:N deposition increases from 0 to 6 sccm. The improved interface quality upon nitrogen doping should be related to the suppressed generation of oxygen vacancies at the device interfacial region. It has been reported that in oxide-based TFTs, like a-IGZO TFTs, a-SIZO TFTs, a-HIZO TFTs, the origin of Vth instability under negative bias illumination stress and positive gate-bias stress is O_V defects within the bulk channel and at the channel/ dielectric interface, which trap holes or electrons.^{14,20,21} For example, there is a report that the stability of a-SIZO TFTs under PBS is apparently improved as the O_V defects within the device channel decrease.²¹ Therefore, by comparing the LFN and the XPS results, the major interfacial trap states within the IGZO TFTs are likely Ov-related defects.

In addition, since the interface quality is improved by nitrogen doping, ideally the μ_{FE} of the a-IGZO TFTs should increase due to the reduced interface scattering.^{22,23} However, as shown in Table I, μ_{FE} shows very small change as a function of N₂ flow rate during the a-IGZO:N inter-layer growth. This observation can be explained by the simultaneously enhanced Coulomb scattering in device channel, which is composed of the a-IGZO:N inter-layer as well as part of the following a-IGZO layer.²⁴ It has been reported that in nitrogen doped ZnO thin films, the nitrogen atoms could substitute for oxygen as acceptors and then serve as fixed negative charges in the lattice.²⁵ Similar effect should happen in nitrogen doped a-IGZO thin films as well, leading to more Coulomb scattering events for channel electrons. As a result, under the influence of both positive and negative impacts, $\mu_{\rm FE}$ of the a-IGZO TFTs could show no apparent change in the studied nitrogen doping range.

In summary, the electrical stability of a-IGZO TFTs has been investigated by inserting an ultra-thin nitrogenated a-IGZO:N inter-layer at the channel/gate dielectric interface. The modified device shows enhanced bias stress stability

is article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to IP: 150 203 178 118 On: Wed, 11, Jun 2014, 05:57:39 with significantly reduced ΔV_{th} after PBS. Based on XPS and LFN analyses, this stability improvement can be attributed to the decrease of trap states near the channel/gate dielectric interface region. In addition, here it should be noted that the focus of this work is to improve the electrical stability of a-IGZO TFTs. Although the V_{th} of the studied TFTs shows small undesirable up-shift upon interfacial nitrogen doping, there are several available ways to lower (or adjust) the V_{th}, such as increasing the indium content of the device channel or reducing the gate oxide thickness.²⁶

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