Enhancement of Signal Integrity and Power Integrity with Embedded Capacitors in High-Speed Packages

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Abstract

Improvements in electrical performance of microelectronic systems can be achieved by the integration of passive elements such as capacitors, resistors and inductors. The advantage of embedded passives is their low parasitic values. In this paper, enhancement of signal-integrity and power-integrity is investigated when a high-k planar capacitor is used as a power-ground plane, with embedded high-k discrete capacitors that have low ESL and ESR values as decoupling capacitors for SSN suppression. In order to capture the effects of embedded capacitor performance, a test-structure involving many signal-lines referenced to a power-ground plane was simulated. Simulation results show that the high-k planar capacitor reduces coupling of noise currents through the power-ground planes and helps improve the eye-opening. Simulation results have been quantified for a case, where a fewer number of embedded discrete capacitors helps reduce SSN more significantly than surface-mounts. Transient co-simulation of the signal delivery network (SDN) and the power-delivery network (PDN) are performed using Y-parameters.

1. Introduction

Embedded passives are integral in building future electronic products that are superior in performance, cheaper and smaller sizes. Embedded passives are formed in a layer in the substrate and include resistors, inductors and capacitors that form the core of today's electronic systems. They eliminate soldering, which translates to lower cost and improved reliability by minimizing solder-joint failure.

The focus of this paper is on embedded capacitors and its role on improved electrical performance when used as Power/Ground planes and decoupling capacitors. The test-case considered is a structure composed of many microstrip lines referenced to a power-ground plane. Eye-diagrams and the switching noise magnitude are compared for high-k vs. low-k dielectrics used for the Vdd/Gnd planes, as well as embedded discrete capacitors vs. surface mounts used for minimizing switching noise. The metric that is used to evaluate signal-integrity is eye-diagrams and the metric used for power-integrity is the magnitude of the switching noise. Eye-diagrams capture effects such as cross-talk, jitter, signal-skew and provide a convenient visual representation. Transient simulation of the structure is performed using Y-parameters.

The transient-simulation methodology using Y-parameters is described in Section 2. Stamping of multi-layered structures is explained in Section 3. Simulations illustrating the advantages of high-k planar capacitors and embedded discrete capacitors are presented in Section 4, followed by conclusions in Section 5.

2. Y-Parameter Simulation Methodology

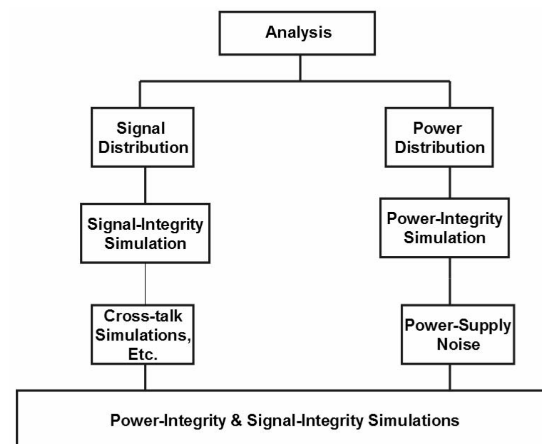

Figure 1: A segment of a PCB/Package design process.

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In the current design process of a PCB/Package, signal-integrity analysis and power-integrity analysis are performed separately as shown in Figure 1 [1]. The signal nets are simulated for cross-talk, delay, reflections, etc. assuming an ideal power-distribution network; the power-delivery network is analyzed separately. The two are integrated together, and an extensive CAD simulation is performed, to check if the design rules are met. In this section, a new methodology using Y-parameters to perform a co-simulation of power-delivery and signal delivery-network is presented. Savings in product development time can be achieved through this merger.

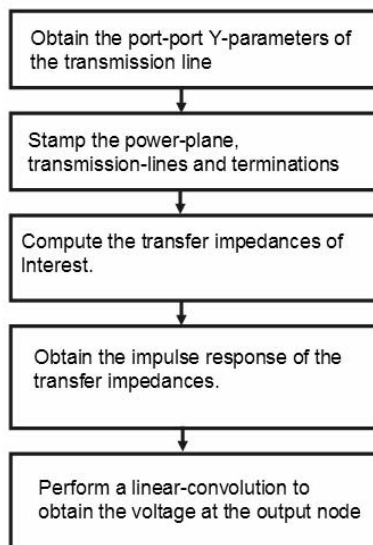

Figure 2: Flow-chart of the proposed simulation technique

The accuracy of the frequency-domain analysis has been verified in [2]. There are several choices for picking the parameter for frequency-analysis such as S-parameters and ABCD-parameters. The most memory and time efficient parameter for analysis with linear sources are the Y-parameters. References [2],[3] propose S-parameters for analysis using frequency-domain parameters. However, the disadvantage of this approach is the large memory consumption for bigger sized problems. S-parameter analysis requires a matrix of size N x N x f, where N is the number of ports of interest, and f is the number of frequency points. Today's packages contain thousands of interconnects and requires a more memory-efficient solution. The memory used may become prohibitively large for large-sized problems, or unnecessarily consume extra memory for smaller sized problems. However, using Y-parameters for the specific problem at hand requires a matrix of size N x f, where N is the number of ports of interest. This is a factor of N less than S-parameter analysis. The flow-chart of the proposed simulation methodology is outlined in Figure 2.

The first step is to obtain the Y-parameters of a transmission line. In this simulation, the transmission line parameters are obtained from ADS®. A transmission line that has been characterized by measurements can also be used. The second step is to stamp the power-plane, transmission lines and terminations. This step will be explained in detail in the next section. A circuit model for a power-plane can be obtained from [4]. The third step is to obtain the Z-transfer impedance parameters between nodes of interest. Typically, there is an output node and many nodes where current-sources are connected. The transfer impedances are calculated between the nodes where current-sources are connected to the output-node. A single output node will require calculating only one row of the inverse of the Y-matrix, from which all the transfer impedances of interest can be obtained. The next step is to compute the impulse response of the transfer-impedances using the inverse Fourier transform (IFFT). Finally, a linear-convolution is performed between the current sources and the impulse response of the transfer-impedance parameters to obtain the output voltage. In this paper, linear-current sources have been assumed.

3. Stamping of multi-layered Structures

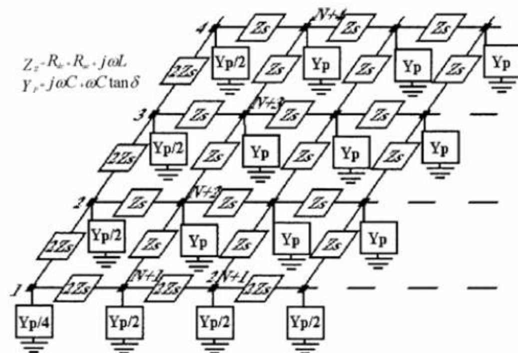

Figure 3: A planar circuit: A non-ideal power-plane model

Step 2 of the algorithm in Figure 2 requires stamping the impedances of the network. The stamp-rule is outlined in detail in [5]. In this technique, every node is assigned a unique number and the admittance value between the nodes is stamped to the Y-matrix. Y-parameters are convenient to represent planar circuits, e.g. a non-ideal power-plane (Figure 3), as well as multilayered circuits, e.g. transmission lines referenced

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to non-ideal power-planes (Figure 4). In addition, passive terminations can be easily incorporated.

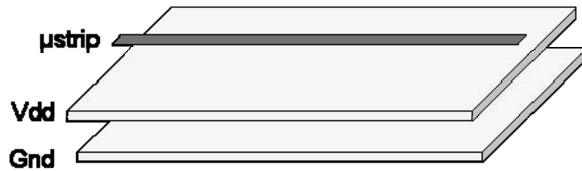

Figure 4: A Microstrip-line referenced to a non-ideal power-ground plane.

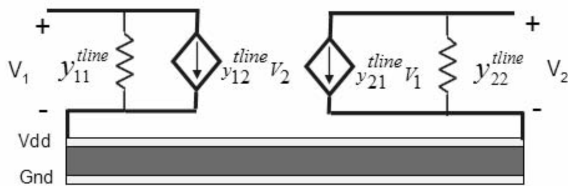

Figure 5: The microstrip-line is replaced with an equivalent two-port model, which can now be stamped in the Y-matrix.

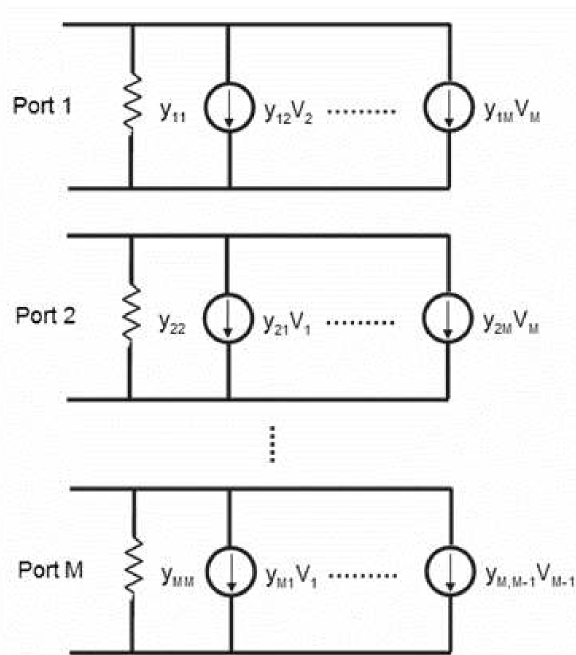

Figure 6: An equivalent model of a M-port network

The only modification is that when an M-port network is referenced to a non-ideal ground node, the M-port network is replaced with its equivalent model. For example, in Figure 4, the two-port transmission line network is replaced with the model shown in Figure 5. The stamp-rule can then be used to obtain the Y-matrix. The model for an arbitrary M-port network is shown in Figure 6. This model is used for modeling coupled transmission-lines.

4. Embedded Planar and Discrete Capacitors

Embedded passives are becoming increasingly important for next generation miniaturized systems through the gradual replacement of discrete passives. Improvements in electrical performance of microelectronic systems can be achieved by the integration of passive elements such as capacitors, resistors and inductors. This leads to an increase in the available real estate for active components that can improve the functionality of a system. The biggest challenges in integration of all passives are those posed by the capacitors. This is primarily because of the high capacitance that is associated with these structures. Decoupling in today's systems is primarily achieved by using surface mount (SMT) capacitors. These capacitors are ineffective at frequencies above 100MHz due to the large inductances associated with the capacitors [6]. Capacitors that are embedded inside a package overcome this limitation because of the low inductance microvias that connect these capacitors to the power and ground plane of the packages.

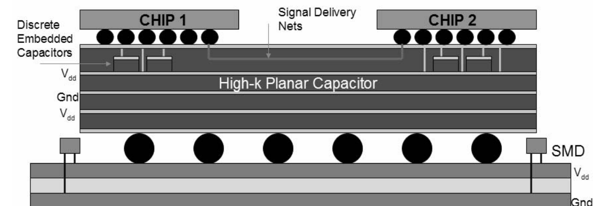

Figure 7: A typical package connected to a PCB

Two types of embedded capacitors are used in the simulations: (1) large planar capacitors, and (2) embedded discrete capacitors. The planar capacitors are used as Vdd/Gnd planes, as well as a reference for the microstrips. Figure 7 shows a typical package connected to a PCB. Two active chips are connected to a package. End to end simulation of signal-lines connected from driver to receiver that is referenced to a high-k planar capacitor is simulated. The embedded discrete capacitors are placed in the package, close to the chip. The proximity of capacitors to the chips minimizes parasitic inductance and provides charge to the switching circuits quicker. The SMDs, typically placed on the PCB, have larger parasitic inductances

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and resistances associated with them due to the longer current path to the chip.

In this section, simulations comparing the performance of high-k vs. low-k dielectrics for plane-pairs, as well as discrete embedded capacitors vs. surface mounts are presented. Results show that the high-k dielectric material for the plane-pair provides more decoupling and helps reduce the noise-voltage through the power-ground plane, thereby improving the eye-opening. Embedded capacitors have significantly lower ESL and ESR and better pin down the SSN voltage than surface-mounts.

The simulation setup is shown in Figure 8. For all the test-cases in this section, the thickness of the substrate between the power-ground plane is 14μm. The plane size is 15mm by 50mm. 100 50Ω-microstrips that are 15mm long are referenced to the power plane. Each microstrip is terminated with 99Ω resistors to the V_{dd} plane and the ground plane.

Results from signal-integrity simulations are shown in Section 4.1 and power-integrity simulations in Section 4.2.

4.1. Signal Integrity Simulations

Four cases are considered and summarized in Table 1. In the coupled-lines case, pairs of transmission lines are coupled, with no-coupling between pairs. The sources are regular bit-patterns. The frequency of the PRBS is 5GHz with a rise/fall time of 20ps.

The eye-diagrams for cases 1 and 2, at the far-end of the 50th line, are plotted in Figure 9 and Figure 10, respectively. $\varepsilon_r = 11$ case shows a larger eye-opening by 213mV. The eye-diagrams for cases 3 and 4, at the far-end of the 50th line, are plotted in Figure 11 and Figure 12, respectively. $\varepsilon_r = 11$ case shows a larger eye-opening by 152mV.

Table 1: Four simulation test-cases

Case #	ε_r of Vdd/Gnd Plane	Coupled/Uncoupled Lines
1	3.8	Uncoupled
2	11	Uncoupled
3	3.8	Coupled
4	11	Coupled

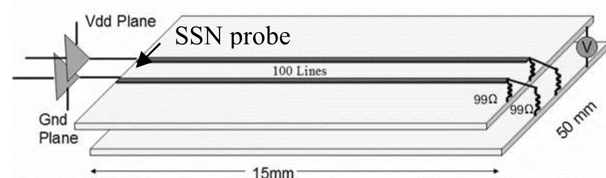

Figure 8: Simulation Setup

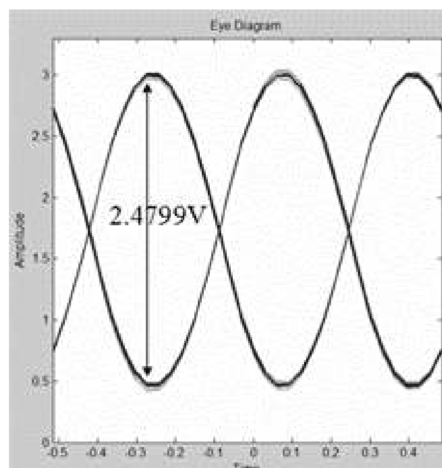

Figure 9: $\varepsilon_r = 3.8$, Uncoupled Lines (Case 1)

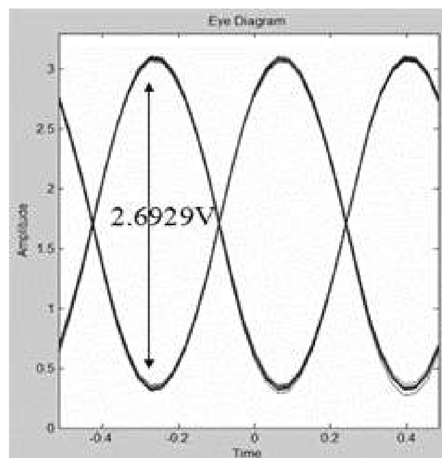

Figure 10: $\varepsilon_r = 11$, Uncoupled Lines, (Case 2)

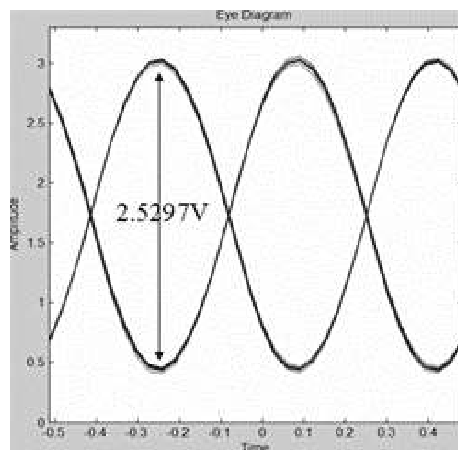

Figure 11: $\varepsilon_r = 3.8$, Coupled Lines, (Case 3)

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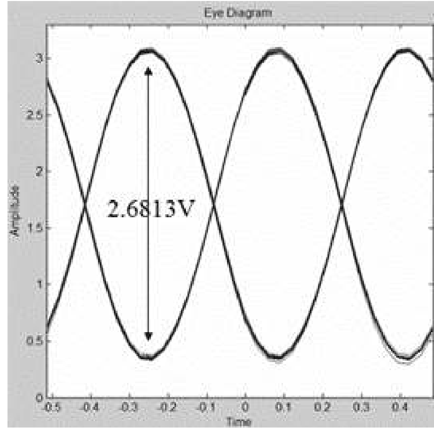

Figure 12: ε_r = 11, Coupled Lines, (Case 4)

4.2. Power-integrity Simulations

25 1nF embedded discrete capacitors of size 1mm by 1mm each, were added along the driver side in one case and 25 100nF SMT capacitors were added in another. SSN was monitored at the location marked by the arrow in Figure 8. The parasitics associated with the capacitors are given in Table 2. The drivers are switching at 1.25GHz with a rise/fall time of 200ps.

Table 2: Parasitics of the capacitors

C	ESL	ESR
1nF embedded	33.54pH	9mΩ
100nF SMT	205.5pH	100mΩ

The ESL and ESR are much smaller for the embedded discrete case due to smaller via and solder bump inductances. Figure 13 shows the switching noise due to 25 100nF SMTs, with a power-ground plane pair substrate ε_r = 3.8. The peak noise-voltage is approximately 150mV. Figure 14 shows the switching noise due to 100 100nF SMTs placed along the driver-side (Figure 8). The SSN has reduced to about 100mV. Figure 15 shows the SSN for the case with 25 1nF embedded capacitors, with a power-ground plane pair ε_r = 11. The peak noise voltage for this case is 50mV. As can be seen from the simulation results, high-k dielectrics and embedded discrete capacitors help substantially reduce the SSN.

5. Conclusions

A simulation methodology using the Nodal Admittance Matrix technique to model power-plane pairs, along with transmission lines was presented. Signal-integrity and power-integrity enhancements using high-k dielectrics were demonstrated. A fewer number of embedded discrete capacitors, along with high-k planar capacitors suppresses SSN better than SMTs.

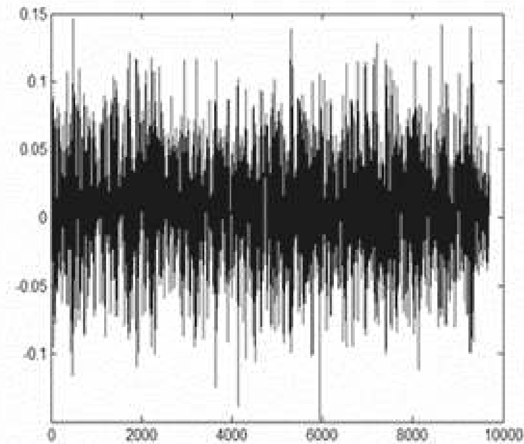
Figure 13: SSN: 25 SMTs 100nF, ε_r = 3.8

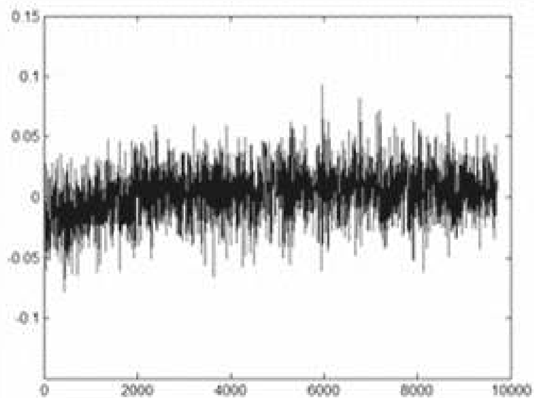
Figure 14: SSN: 100 SMTs 100nF, ε_r = 3.8

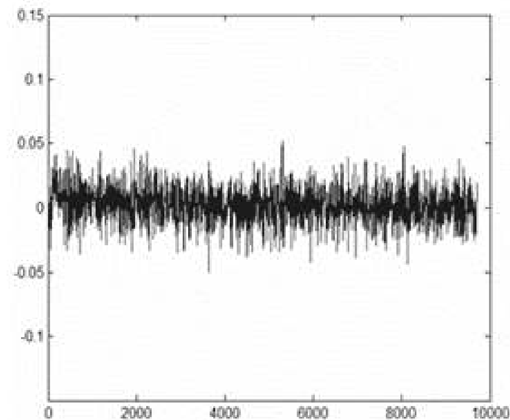
Figure 15: SSN: 25 Embedded discretes 1nF, ε_r = 11

6. References

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