Enhancing Delay Fault Coverage through Low Power Segmented Scan*

Zhuo Zhang[1], Sudhakar M. Reddy[1], Irith Pomeranz[2], Janusz Rajski[3], and Bashir M. Al-Hashimi[4]

1. ECE Dept., University of Iowa, Iowa City, IA 52242, {zhuzhang, reddy}@engineering.uiowa.edu
2. School of ECE, Purdue University, Wet Lafayette, IN 47907, pomeranz@ecn.purdue.edu
3. Mentor Graphics Corp., 8005 SW Boeckman Rd., Wilsonville, OR 97070, janusz_rajski@mentor.com
4. School of ECS, University of Southampton, United Kingdom, SO17 1BJ, bmah@ecs.soton.ac.uk

Abstract - **Reducing power dissipation during test has been an active area of academic and industrial research for the last few years and numerous low power DFT techniques and test generation procedures have been proposed. Segmented scan [17-20] has been shown to be an effective technique in addressing test power issues in industrial designs [18]. To achieve higher shipped product quality, tests for delay faults are becoming essential components of manufacturing test. This paper demonstrates, for the first time, that segmented scan facilitates increased delay fault without degrading the reduction of the switching activity obtained by segmented scan. The increased transition delay fault coverage is achieved through careful selection of the capture cycle application. Experimental results on larger ISCAS-89 benchmarks show that using three segments, on average, fault coverage using launch off capture can be increased by about 5.8% while simultaneously reducing the peak switching activity caused by capture cycles by over 24.8%.**

I. Introduction

With decreasing feature sizes of VLSI circuits, manufacturing tests based on the stuck-at fault model are becoming less effective in detecting defects which are typically resistive opens and shorts. To achieve low DPM (defective parts per million shipped parts), tests for delay faults are becoming essential components of manufacturing test. Excessive power may be dissipated during scan based tests due to increased switching activity in the circuit nodes caused by scan shifts as well as by capture cycles. Excessive current demand during test may cause supply voltage droops and increase circuit signal propagation delays. During at-speed test for transition delay faults, supply voltage droops

* Research supported in part by SRC Grant No. 2004-TJ-1243 (ZZ and SMR), in part by SRC Grant No. 2004-TJ-1244 (IP) and in part by EPSRC(UK) Grant GR/S05557 (BMH).

caused by switching activity during capture cycles have been observed to fail good chips due to increased circuit delays [1].

Testing for delay faults requires application of two pattern tests. In standard scan designs, delay faults are typically tested using skewed-load also called launch off shift [2] method or using broadside also called launch off capture method [3]. Both test methods may not achieve as high fault coverage for delay faults as, for example, for stuck-at faults. This is due to the fact that the second pattern of a two pattern test is correlated to the first pattern [2, 3]. To achieve maximum delay fault coverage, enhanced scan which allows application of arbitrary two-pattern tests has been proposed [4]. However the relatively high area overhead of enhanced scan precludes its use in many designs. The recent work in [5] achieves scan designs capable of applying arbitrary two pattern tests with area overhead less than that for enhanced scan. However the resulting area overhead may still be unacceptably high for many designs.

Several methods to reduce switching activity during scan based test have been proposed [5-20]. Methods proposed in [5-8] make modifications to scan chains to facilitate reduction of switching activity during scan shift. In [5] and [9] methods to select primary input values to reduce switching activity during scan shift as well as reduce leakage current have been proposed. Work in [10] proposes ordering tests to reduce switching activity during scan shift. Work in [11] proposes reducing the scan shift frequency to reduce dynamic power consumption during scan shift. The works in [12-14] propose modifying the test generation procedures such that the circuit operation during test capture cycles is restricted to functional or close to functional operation. This will render the switching activity caused by capture cycles to be close to that during normal circuit operation. However the fault coverage is typically reduced. The methods of [15] and [16] fill unspecified values in a test cube, in a specific manner, to reduce switching activity. This method as well as those in [12-14] reduces the number of unspecified values in tests that can be filled arbitrarily. Reduction in the number of unspecified values that can be filled arbitrarily impairs the achievable reduction in test data volume using test data compression methods. For example test data compression methods based on LFSR seeding [21] fill the unspecified values by linear combinations of the specified values.

As noted above most proposed methods that modify the scan chains and/or the circuit under test reduce switching activity caused by scan shifts but do not reduce switching activity caused by capture cycles. A method that facilitates reduction of switching activity caused by scan shift as well as by capture cycles is the segmented scan first proposed in [17] and investigated in [19,20] for testing stuck-at faults.

In this work we investigate test generation for delay faults in segmented scan designs. Earlier works on segmented scan chains considered stuck-at faults only [17-20]. In [19,20], it is shown that the same stuck-at fault coverage as that obtained for unsegmented scan designs can be obtained for segmented scan designs. We show, for the first time, that

using segmented scan design one can obtain higher delay fault coverage without reducing switching activity reduction during test.

For transition delay faults, even though segmentation of scan chains can be shown to improve fault coverage for both launch off shift and launch off capture methods, in this work, for the sake of brevity, we consider only launch off capture test method.

The remainder of the paper is organized as follows. In Section II we review test generation for delay faults and scan chain segmentation. In Section III we discuss methods to generate tests for delay faults in designs with segmented scan chains. In Section IV we present results on benchmark circuits and Section V concludes the paper.

II. Preliminaries

In this section we briefly review the launch off capture test method for delay faults and scan chain segmentation to reduce power dissipation during test. For the sake of simplicity of explanation we assume full scan designs with single clock and consider transition delay faults (TDF) only.

A. Scan-based delay tests

A test for a TDF requires the application of a two-pattern test (V1, V2). V1 is called the initialization pattern and V2 is called the launch pattern. The test application can be divided into three phases: (a) initialization phase (IP) during which V1 is scanned in, (b) launch phase (LP) during which V2 is generated through the combinational logic of the circuit under test by clocking the circuit once in functional mode, and (c) the test response capture phase (CP) during which the circuit is clocked once more in functional mode.

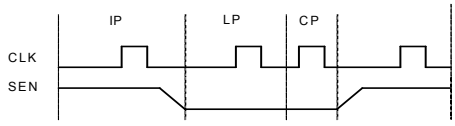

Figure 1: Launch off capture delay tests

Figure 1 illustrates launch off capture tests. The signals CLK and SEN are clock and scan enable, respectively. The three phases of test application are shown. After the initialization pattern V1 is scanned in, SEN is set to inactive state and two capture clock cycles (LP and CP in Figure 1) are applied. The launch cycle called the slow capture cycle [1] captures the launch pattern V2 generated at the outputs of the combinational logic of the circuit under test. The second capture cycle called the fast capture cycle [1] captures the circuit response to the test which is scanned out after setting SEN to active state.

During the application of launch off capture tests, circuit nodes switch states due to scan shifts as well as capture cycles. The switching activity caused by the launch cycle that generates V2 from V1 is an important concern in at-speed application of launch off capture delay tests [1]. This is because high node switching activity demands high supply current which may lead to supply voltage droop which tends to increase signal propagation delays of effected gates. Increased delay due to supply voltage droops may lead to capturing faulty responses during the second capture cycle. This causes good chips to fail tests leading to yield loss [1].

B. Segmented scan chain designs

Partitioning scan chains into two or more segments was first proposed in [17] as a way to reduce switching activity caused by scan shifting. During each scan shift, a large number of scan cells may switch states causing high switching activity in the scan cells as well as in the combinational logic of the circuit under test. To reduce this switching activity, a scan chain is partitioned into near equal length segments as shown in Figure 2. In Figure 2 (a) a single scan chain is shown. Figure 2 (b) illustrates the scan chain partitioned into three equal length scan segments. All segments are connected to the same scan input and to the same scan output through tri-state buffers. Each segment can be clocked independently. The SOi, i = 1,2,3, signals control scanning out responses from individual segments.

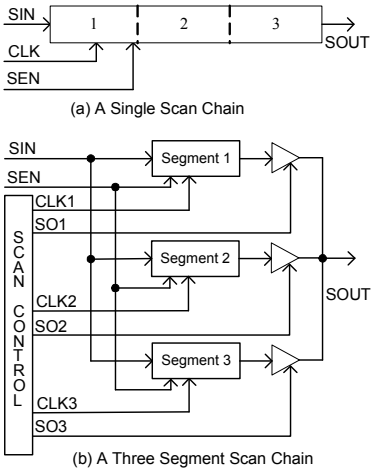

Figure 2: Segmented Scan Chains

In segmented scan designs, a test for stuck-at faults is applied in the following manner. The test is scanned in segment by segment and a capture cycle is applied after the complete test is scanned in. The capture cycle may be applied to all segments at the same time [17] or to one or more segments at a time [19, 20] followed by scanning out the test response again one segment at a time. In [20] it was shown that even if only one segment is allowed to capture test responses one can achieve the same stuck-at fault coverage as that for the unsegmented design. This is achieved by selectively capturing test responses in appropriate segments. Because only one segment is clocked at a time to

capture test responses, switching activity caused by the capture cycles is reduced compared to that in unsegmented scan designs in which all scan cells capture test response during one capture cycle.

In this work we consider TDFs. We experimentally demonstrate that the fault coverage for TDFs in segmented scan designs can be substantially higher than in unsegmented scan designs in contrast to obtainable stuck-at fault coverage which is identical in both the designs as shown in [19, 20]. The number of tests to achieve the higher TDF coverage is understandably higher.

As in the earlier works on segmented scan designs we assume that each segment can be clocked independent of other segments. It should be pointed out that designs with multiple scan chains can be considered as segmented scan designs when each scan chain (or a segment of a scan chain if the multiple scan design employs, in addition, segmentation of scan chains) can be independently clocked. The design flow to provide independent (gated) clocks for segments and scan chains in multiple scan chain designs is accommodated in industrial designs [18] by specifying the segments and the control logic for gated clocks at the top level of the design prior to synthesis. Thus tests for stuck-at faults and at-speed tests for delay faults can be applied to the resulting designs without additional post synthesis design effort.

III. Test generation for TDFs in scan designs with segmented scan chains

Consider generating a launch off capture two pattern test (V1,V2) for a TDF. In the unsegmented scan designs V2 is generated by shifting in V1 into the scan chain(s) and applying a functional clock cycle called the launch cycle. This is followed by applying a second functional clock cycle called the capture cycle. In segmented scan designs, in which each segment can be clocked independently, we have many options in applying the launch and capture cycles. Some of the possible test application methods are illustrated in Figure 3 for designs with two segments.

In Figure 3, SC stands for scan cycle, LC stands for launch cycle and CC stands for capture cycle. In all the tests shown in Figure 3, the initialization vector is scanned into Segment 1 (Segment 2) while Segment 2 (Segment 1) is not clocked. Tests in Figures 3 (a) through 3(d) apply launch clock cycles to only one segment. For example, tests illustrated in Figures 3(a) through 3(c) apply launch clock cycle to Segment 1 only while the tests corresponding to Figure 3(d) apply launch cycle to Segment 2 only. Tests of the type illustrated in Figures 3(e) and 3(f) apply launch clock cycles to two segments. As is the case with launch cycles, different numbers of segments can be clocked during capture cycles. For example in Figures 3(a), 3(b) and 3(e) only one segment is clocked during capture where as in tests illustrated in Figures 3(c), 3(d) and 3(f) two segments are clocked during capture cycle. Notice that the test application using Figure 3(f) is equivalent to the launch on capture test applied to unsegmented design since both

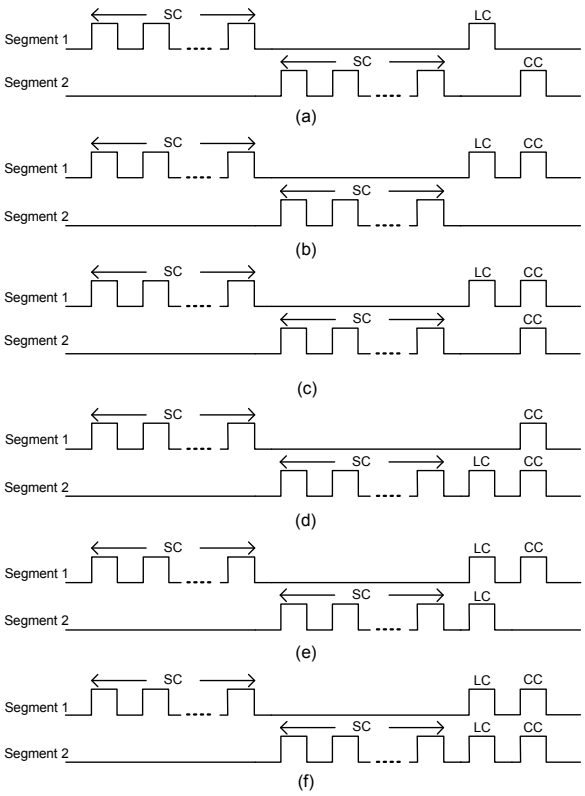

Figure 3: Some test application methods for designs with two segments

segments are clocked in both capture cycles. The maximum of the switching activity, called peak switching activity in this work, caused by the application of functional clocks for launch and capture depends on the number of segments clocked. The smaller the number of segments clocked, the smaller the peak switching activity is. As we discussed earlier, in at-speed testing for delay faults the switching activity caused by the launch cycle is of main concern since higher switching activity may cause supply voltage droops which may increase circuit propagation delays and affect the test responses captured during capture cycle. The switching activity caused by capture cycles is assumed to be not a concern. It can be readily proved that limiting the number of segments clocked during capture cycles may only affect the number of tests but does not affect the maximum delay fault coverage obtainable in segmented scan designs. The reason is that the second pattern V2 of a two pattern test (V1, V2) is derived from the scanned in initialization pattern. By allowing clocking of all possible subsets of segments in the launch cycle one can exhaust all possible ways of deriving V2 from the scanned in V1. Furthermore, since V1 is scanned in, it can be an arbitrary pattern. By simultaneously clocking all segments in the second capture cycle one would capture test responses on all observed scan cells. This can be seen by analyzing the following example. Consider the case of two segments with the clocking scheme shown in Figure 3(c). Let V1 be the initialization pattern. Consider two tests applied with clocking schemes in Figures 3(a) and 3(b) using the same initialization vector V1. Note that in both clocking schemes the launch cycle clocks the same segment – segment 1 – as the clocking scheme in Figure 3(c). Thus the same second

vector V2 is generated during the application of the tests. However the test response is captured in both segments simultaneously using clocking scheme in Figure 3(c) whereas the test response is captured in one of the two segments with two different tests using the two clocking schemes in Figures 3(a) and 3(b). For this reason, in the experimental results given in the next section, the tests used clocked all segments during the capture cycle. If the switching activity caused by capture cycles is a concern, then one can limit the number of segments clocked during capture cycles also.

Next we discuss why the TDF coverage in segmented scan designs may be higher than that for unsegmented scan designs. As noted above, there are several ways to apply the launch clock cycle. For example, one can clock one or two or even all segments simultaneously. Thus, more than one second pattern V2 can be generated from the same scanned in first pattern V1 by choosing different subsets of segments to clock during the launch cycle. This enlarges the set of two pattern tests that can be applied to the circuit under test using launch off capture. Of course, clocking only one segment during launch cycle leads to minimum peak switching activity.

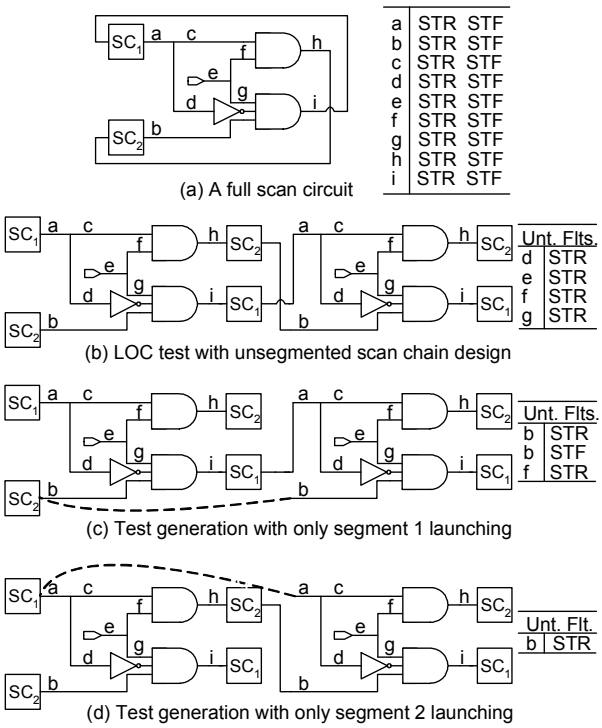

Figure 4: An example to illustrate why higher TDF coverage can be obtained in segmented scan design

Example: Consider the full scan circuit in Figure 4(a). In Figure 4(a) we also list the 18 collapsed TDFs in this circuit, where STR(STF) stands for slow to rise (slow to fall) TDF. Now consider generating tests using standard launch off capture (LOC) test method illustrated in Figure 4(b) where an ILA (iterative logic array) of two time frames is shown. Four TDFs that are given in the table of Figure 4(b) are undetectable in the standard unsegmented scan design, resulting in the TDF coverage of 14/18*100% = 77.78%. Suppose the two scan cells are divided into two segments, SC_1 assigned to segment 1 and SC_2 assigned to segment 2. Figures 4(c) and 4(d) show the test generation

with only one segment launching. The dotted lines from scan cells represent the fact that their contents are not changed after the launch cycle. If tests are generated with launch clock applied to segment 1 only, as shown in Figure 4(c), only three TDFs shown in the table of Figure 4(c) are undetectable. If we continue test generation this time applying launch clock to only segment 2, only one TDF shown in the table in Figure 4(d) remains undetected. Thus, the TDF coverage of the tests that apply launch clock to only one segment is 17/18*100% = 94.44%.

The experimental results presented in the next section also show that TDF tests that clock only one segment during launch cycle achieve higher fault coverage for all but one of the larger ISCAS-89 circuits while reducing the peak switching activity. This is in contrast to the coverage of stuck-at faults for which the fault coverage in segmented and unsegmented scan designs is identical [19, 20]. Additionally, the experimental results presented in the next section show that initially using tests that clock single segments in the launch cycle and continuing with tests that progressively clock more segments in the launch cycle allows achieving additional fault coverage with reduced peak and average switching activity during the launch cycle compared to the unsegmented scan design.

In this work we use *Weighted Switching Activity* (WSA) defined below as a measure of switching activity. WSA was also used to represent instantaneous power in earlier works [6]. The *weighted switching activity* (WSA) of a node is the number of state changes at the node multiplied by (1+node fan-out). The WSA of the entire circuit is obtained by summing the WSA of all the nodes in the circuit.

IV. Experimental results

In this section we report results of three experiments performed. As discussed in Section III for segmented scan designs one can use several different methods of launch cycles. For example one can launch transitions by clocking only one segment or by clocking two segments and so on. As illustrated in Section III through an example, this flexibility leads to the possibility of achieving higher TDF coverage in segmented scan designs compared to unsegmented scan designs. The first experiment we conducted is to investigate the maximum improvement in TDF fault coverage achieved in ISCAS-89 benchmark circuits using segmented scan designs. Results of this experiment are given in Section IV.A. In this experiment we allowed all possible ways to apply launch cycles.

The hardware to facilitate all possible methods of launch cycles may not be acceptable in some designs. For this reason, in the second experiment we restricted the number of different launch cycles to two. Results of this experiment are reported in Section IV.B.

The main reason for using segmented scan is to reduce switching activity during scan based test. However, as discussed above segmented scan also facilitates increased TDF coverage. Thus a natural question to ask is whether it is possible to simultaneously reduce switching activity maximally and achieve maximal fault coverage. The third experiment we conducted was to investigate a method to achieve this dual objective. Results of this experiment are reported in Section IV.C.

A. Maximizing TDF fault coverage achieved for segmented scan designs

We implemented a test generator for TDFs, using launch off capture method, for unsegmented and segmented scan designs and applied to larger ISCAS-89 benchmark circuits. To create the segmented designs we randomly assigned scan flip-flops to different scan segments. In our experiments we used designs with two and three segments. We report TDF coverages achieved, peak WSA and average WSA caused by the launch cycles of tests. As discussed earlier, during the capture cycle all segments are clocked. It is important to state that for all circuits the test generator did not abort on any faults and hence the differences in fault coverages reported for unsegmented and segmented designs are exact. Additionally after a test cube is generated we filled the unspecified values randomly to obtain fully specified test patterns which are fault simulated. Thus the ability to compress test data using available test data compression methods, when employed, will not be impaired.

The results obtained for tests that clock only one segment during launch cycle for segmented designs are given for the two segment case in Table 1 and for the three segment designs in Table 2. The data in these two tables are

Table 1: Experimental results for designs with two segments using T1 test sets

Circuit	# Flts.	FC (%)		# Tests			Peak WSA			Average WSA		
		TS	T1	TS	T1	%Inc.	TS	T1	%Red.	TS	T1	%Red.
s3330	4712	83.55	94.99	162	321	98.15	2576	2148	16.61	1983	1049	47.1
s3384	5520	99.98	99.98	100	146	46	2919	2253	22.82	2385	1466	38.53
s5378	7040	91.08	96.68	167	253	51.5	3732	2779	25.54	2947	1719	41.67
s9234	11328	84.01	85.38	327	451	37.92	7036	5348	23.99	4461	2685	39.81
s13207	15602	80.05	89.85	374	558	49.2	8659	6130	29.21	5691	3288	42.22
s15850	19046	71.06	75.88	183	287	56.83	9537	8049	15.6	6142	4489	26.91
s35932	63502	85.98	88.08	40	157	292.5	28958	24414	15.69	23350	17498	25.06
s38417	49738	98.04	96.77	222	400	80.18	24993	19008	23.95	18597	12065	35.12
s38584	61254	90	92.2	284	538	89.44	27329	22543	17.51	16159	14138	12.51
Average		87.08	91.09			89.08			21.21			34.33

Table 2: Experimental results for designs with three segments using T1 test sets

Circuit	# Flts.	FC (%)		# Tests			Peak WSA			Average WSA		
		TS	T1	TS	T1	%Inc.	TS	T1	%Red.	TS	T1	%Red.
s3330	4712	83.55	96.31	162	383	136.42	2576	1865	27.6	1983	780	60.67
s3384	5520	99.98	100	100	186	86	2919	1899	34.94	2385	1118	53.12
s5378	7040	91.08	97.54	167	339	102.99	3732	2214	40.68	2947	1205	59.11
s9234	11328	84.01	85.78	327	525	60.55	7036	4745	32.56	4461	1968	55.88
s13207	15602	80.05	90.19	374	582	55.61	8659	5212	39.81	5691	2479	56.44
s15850	19046	71.06	77.86	183	369	101.64	9537	7609	20.22	6142	3649	40.59
s35932	63502	85.98	88.13	40	161	302.5	28958	23971	17.22	23350	16033	31.34
s38417	49738	98.04	96.28	222	487	119.37	24993	15652	37.37	18597	9175	50.66
s38584	61254	90	92.74	284	546	92.25	27329	20632	24.51	16159	11835	26.76
Average		87.08	91.65			117.48			30.55			48.29

arranged in identical manner. For ease of reference we denote the standard launch off capture test sets for the unsegmented design by TS and the test sets for the segmented design that clock only one segment during launch by T1. After the circuit name we give the number of TDFs in the collapsed list of faults, followed by fault coverages obtained by TS for the unsegmented design and by T1 for the segmented design. In the next three columns we give the number of test patterns in TS, T1 and the percentage increase in the size of T1 over the size of TS, respectively. In the next three columns we give the peak WSA caused by the launch cycle of TS tests, T1 tests and the percentage reduction in the peak WSA of T1 tests relative to TS tests. Information similar to that for peak WSA is given for average WSA in the last three columns. In the last row we give the data averaged over all the circuits.

From Tables 1 and 2 we can observe the following. The TDF fault coverage for all but one circuit (s38417) is higher using test set T1 for the segmented designs compared to that obtained for the unsegmented designs (which use test set T0). Averaged over all circuits the fault coverage increases by over 4% for designs using two segments and by over 4.5% for designs using three segments. At the same time, the peak WSA and average WSA are reduced by over 21% and 34% for designs with two segments, and by over 30% and 48% for designs using three segments. From Tables 1 and 2, we observe that increasing the number of segments from 2 to 3 increases the TDF coverage on average by over 0.5%. The average percentage reductions in both peak WSA and average WSA are improved as well. However the pattern counts increase.

As noted earlier, additional faults can be detected by allowing more than one segment to be clocked during the launch cycle. This will increase the switching activity caused by the capture cycles but will allow maximizing the fault coverage achieved for segmented scan designs. For the two segment design we generated tests with both segments clocked during the capture cycle. Results of this experiment are given in Table 3.

In Table 3, after the circuit name we give the number of additional faults detected, above those detected when only one segment is clocked, when both segments are clocked during launch cycle. In the next three columns we give the numbers of tests in TS, T1 and T2, where test sets TS and T1 are the same as in Table1 and T2 is the set of tests which clock two segments in the launch cycle. It is important to note that the tests in T2 are only those that were generated to detect the additional faults given in column 2 of this table. The fault coverages are given next. For the unsegmented scan design the fault coverage is given under column TS and for segmented design when only one segment is clocked is given under column T1 and when one or two segments are clocked is given under T2. That is, the fault coverage under T2 is the cumulative coverage by tests generated first with one segment clocking followed by tests with two segments clocking in the launch cycle. In the next three columns we give the peak WSA during the launch cycle for the unsegmented design, the segmented design using single segment clocking in the launch cycle and

Table 3: Results on maximizing fault coverage for designs with two segments

Circuit	#add. flts det	# Tests			FC(%)			Peak WSA		
		TS	T1	T2	TS	T1	T2	TS	T1	T2
s3330	18	162	321	13	83.55	94.99	95.37	2576	2148	2349
s3384	0	100	146	0	99.98	99.98	99.98	2919	2253	-
s5378	15	167	253	7	91.08	96.68	96.89	3732	2779	3223
s9234	97	327	451	20	84.01	85.38	86.24	7036	5348	5378
s13207	322	374	558	19	80.05	89.85	91.92	8659	6130	6883
s15850	224	183	287	30	71.06	75.88	77.06	9537	8049	6953
s35932	237	40	157	5	85.98	88.08	88.45	28958	24414	22552
s38417	919	222	400	32	98.04	96.77	98.62	24993	19008	22621
s38584	850	284	538	45	90	92.2	93.58	27329	22543	24348
WSA %red					87.08	91.09	92.01		21.21	15.67
Av. Ave WSA %red									34.33	24.76

the segmented design with both segments clocked during the launch cycle. It should be noted that peak WSA given in the last column is for only those tests that were generated to detect additional faults by clocking both the segments in the launch cycle. That is, the peak WSA under column T2 is for the tests in T2 only. Since both segments are clocked in the launch cycles for these tests they are similar to the tests for unsegmented design in which both segments are clocked. However as can be noted, the peak WSA of the additional tests generated to maximize fault coverage is smaller than the peak WSA for the tests for unsegmented design. This implies that the faults remaining after using tests that clock only one segment are such that even though detecting them requires simultaneous clocking of all segments the peak WSA is lower than when unsegmented designs are used to detect all faults. A '-' in Table 3 indicates that no additional faults are detected and hence no additional tests are generated using two segment clocking. In the last but one row of Table 3 we give average fault coverage achieved when only one segment is clocked and when one or both segments are clocked in the launch cycle. It can be seen that on the average the fault coverage increases by about 1% by using tests that clock both segments during the launch cycle. In the last two columns of this row we show the average percentage reduction in peak WSA, compared to the unsegmented case, when only one segment is clocked and when one or both segments are clocked in the launch cycle. We give similar averages for average WSA in the last row.

From Tables 1 and 3 we can see that by allowing progressively more segments to be clocked during the launch cycle, we can obtain higher TDF fault coverage than for the unsegmented designs for all circuits. On the average the fault coverage increases by about 5% over that obtained for unsegmented scan designs while reducing the peak WSA and average WSA by over 15% and 24%, respectively.

In Table 4 we give the results for the design with three segments. For designs with three segments one can clock one, two or three segments in the launch cycle. Results of test generation by clocking one segment, followed by clocking two segments and finally clocking all three segments are given under headings T1, T2 and T3, respectively.

Table 4: Results on maximizing fault coverage for designs with three segments

Circuit	#flts.det				FC(%)				Peak WSA			
	TS	T1	T2	T3	TS	T1	T2	T3	TS	T1	T2	T3
s3330	3937	4538	41	0	83.55	96.31	97.18	97.18	2576	1865	1574	-
s3384	5519	5520	0	0	99.98	100	100	100	2919	1899	-	-
s5378	6412	6867	15	3	91.08	97.54	97.76	97.8	3732	2214	1816	2824
s9234	9517	9717	99	0	84.01	85.78	86.65	86.65	7036	4745	3717	-
s13207	12489	14072	424	28	80.05	90.19	92.91	93.09	8659	5212	5404	6223
s15850	13535	14830	298	15	71.06	77.86	79.43	79.51	9537	7609	6422	5585
s35932	54599	55965	298	1	85.98	88.13	88.6	88.6	28958	23971	19370	24070
s38417	48761	47890	1225	44	98.04	96.28	98.75	98.84	24993	15652	17671	17274
s38584	55129	56810	878	37	90	92.74	94.18	94.24	27329	20632	21050	24763
Av FC & Peak WSA %red					87.08	91.65	92.83	92.88		30.55	29.23	24.82
Av. Ave. WSA %red										48.29	42.6	39.72

The data is arranged similar to that in Table 3. Under #flts.det for T2 and T3 we give the number of additional faults detected over those given under T1. The fault coverage reported under T2 includes the faults detected by tests that clock one as well as two segments. Similarly under T3 the faults detected by tests that clock one or two or three segments are included. As in Table 4, the peak WSA reported under Ti, i = 1,2,3, are for the tests that clocked i segments during the launch cycle. Also as in Table 4, in the last but one row we give the average fault coverage over all the circuits. A '-' indicates that no additional tests are generated. The average reduction in peak WSA under Ti for tests that clocked i or fewer segments during the launch cycle and the corresponding values for average WSA are given in the last three columns of the last two rows. From Table 4 we see that segmented designs with three segments have on the average 5.8% higher TDF coverage while the peak and average WSA of tests are reduced by about 25% and 40%, respectively.

From Tables 3 and 4, we note that increasing the number of segments from 2 to 3 increases the TDF coverage on average by about 1.8%. The average percentage reduction in peak WSA is improved from 15% to 25% and the percentage reduction in average WSA is improved from 24% to 40%, respectively. Further increase in the number of

Table 5: The number of tests used when maximizing fault coverage for designs with three segments

Circuit	TS	T1	T2	T3	T
s3330	162	383	22	0	405
s3384	100	186	0	0	186
s5378	167	339	3	2	344
s9234	327	525	39	0	564
s13207	374	582	46	7	635
s15850	183	369	60	10	439
s35932	40	161	6	1	168
s38417	222	487	49	13	549
s38584	284	546	101	7	654

segments is expected to improve reductions in peak and average WSA as well as fault coverage.

In Table 5 we give the numbers of tests in TS, T1, T2 and T3 for the designs with three segments. Under column T we give the sum of the tests in T1, T2 and T3. It can be see that the test set sizes grows modestly while higher fault coverages are achieved as more and more segments are clocked during launch cycle. However as can be seen from Table 4 peak WSA caused by launch cycles is still less for the segmented design compared to the unsegmented design even when all segments are clocked to derive tests to detect additional faults.

B. *Use of only two types of launch cycles*

In order to apply different types of launch cycles the control circuit used may not be acceptable for some designs. For this reason we conducted the following experiment using only two types of launch cycles. We used launch cycles that clock only one segment and launch cycles that clock all segments. For the designs with two clock cycles results are already known and given in Table 3. For the designs with three segments the results are given in Table 6. The data in Table 6 is organized similar to the data in Table 3. In Table 6 under T3 we give the data for the launch cycles that clocked all three segments. Comparing the fault coverage data in Tables 4 and 6, we note that the average fault coverage using only two types of launch cycles decreases to 92.81 compared to the maximum achievable 92.88 when all types of launch cycles are allowed as for the data in Table 4. Thus one can conclude that using only a limited set of launch cycles one can achieve near maximum fault coverage.

Table 6: Using two types of launch cycles for the designs with three segments

	#add.	# Tests		FC(%)		Peak WSA		
Circuit	flts det	T1	T3	T1	T3	TS	T1	T3
s3330	41	383	19	96.31	97.18	2576	1865	2466
s3384	0	186	0	100	100	2919	1899	-
s5378	14	339	4	97.54	97.74	3732	2214	2968
s9234	96	525	20	85.78	86.63	7036	4745	5552
s13207	399	582	27	90.19	92.75	8659	5212	7408
s15850	305	369	37	77.86	79.47	9537	7609	6476
s35932	299	161	4	88.13	88.6	28958	23971	21317
s38417	1261	487	28	96.28	98.82	24993	15652	21874
s38584	847	546	65	92.74	94.13	27329	20632	24921
WSA %red				91.65	92.81		30.55	17.11
Av. Ave WSA %red							48.29	36.29

C. *A method to achieve near maximum fault coverage and maximum reduction in peak WSA*

The next experiment we conducted was to investigate a method that simultaneously achieves near maximum fault coverage and maximum reduction in peak WSA caused by launch cycles. As discussed earlier, the peak or maximum value of WSA is maximally reduced if only one segment is clocked during launch cycle. Let the peak WSA of such

tests for a circuit be P. There are typically many standard launch off capture tests which clock all segments with WSA no greater than P. So one can employ such tests to detect as many faults as possible and use tests that clock only one segment for other faults. By doing this, one can obtain higher fault coverage without increasing the peak WSA caused by the tests. Higher fault coverage is obtained since some of the faults that are not detected when only one segment is clocked during launch cycle are detected when all the segments are clocked by the standard launch off capture tests. Below we formally state this test generation strategy that is shown in Figure 5.

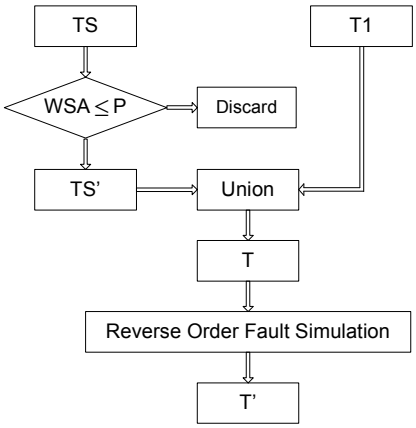

Figure 5: Test generation strategy

Let TS be the set of tests using standard launch off capture test method and let T1 be the test set obtained by generating tests that apply launch clock cycle to only one segment. Let P be the peak WSA for tests in T1. Let TS' be the subset of tests in TS for which the peak WSA is not higher than P. Let T = TS' $\cup$ T1. Next we reduce the test set T by applying a static test compaction procedure such as reverse order fault simulation in which the tests in TS' are simulated ahead of the tests in T1 to obtain the final test set T'.

It should be noted that the peak WSA for any test in T' is not higher than P and the fault coverage of T' is no less than that of TS' or T1. Thus T' may achieve higher fault coverage than TS' and T1. Experiments on benchmark circuits show that the fault coverage of T' is typically higher than either of TS or T1. Furthermore, the number of tests in T' is typically smaller than the number of tests in T1.

In the procedure given above to obtain test set T' one has to generate test sets TS and T1. Instead one can first generate test set T1 and find P, the peak WSA of tests in T1. Then one can generate standard launch off capture tests using WSA of P as a constraint. This will require modifications to TDF test generation procedures.

Results using T' test sets are given in Tables 7 and 8 for designs with two segments and three segments, respectively. The data in these two tables are organized in a manner similar to Tables 1 and 2 except that the test sets for segmented designs are T' instead of T1. It can be seen that, if tests from T' are applied instead of T1, on the

Table 7: Experimental results for designs with two segments using T' test sets

Circuit	FC (%)		# tests			Peak WSA			Average WSA		
	TS	T'	TS	T'	%Inc.	TS	T'	%Red.	TS	T'	%Red.
s3330	83.55	95.29	162	269	66.05	2576	2136	17.08	1983	1386	30.11
s3384	99.98	99.98	100	133	33	2919	2241	23.23	2385	1563	34.47
s5378	91.08	96.65	167	227	35.93	3732	2777	25.59	2947	1924	34.71
s9234	84.01	86.19	327	383	17.13	7036	5346	24.02	4461	4140	7.2
s13207	80.05	91.65	374	465	24.33	8659	6115	29.38	5691	4300	24.44
s15850	71.06	77.06	183	272	48.63	9537	8016	15.95	6142	5512	10.26
s35932	85.98	88.43	40	116	190	28958	24000	17.12	23350	18760	19.66
s38417	98.04	98.56	222	327	47.3	24993	18989	24.02	18597	15646	15.87
s38584	90	92.92	284	394	38.73	27329	22315	18.35	16159	13311	17.62
Average	87.08	91.86			55.68			21.64			21.59

Table 8: Experimental results for designs with three segments using T' test sets

Circuit	FC (%)		# tests			Peak WSA			Average WSA		
	TS	T'	TS	T'	%Inc.	TS	T'	%Red.	TS	T'	%Red.
s3330	83.55	96.63	162	288	77.78	2576	1860	27.8	1983	966	51.29
s3384	99.98	100	100	183	83	2919	1899	34.94	2385	1163	51.24
s5378	91.08	97.51	167	297	77.84	3732	2214	40.68	2947	1330	54.87
s9234	84.01	86.45	327	394	20.49	7036	4737	32.67	4461	3520	21.09
s13207	80.05	91.9	374	507	35.56	8659	5200	39.95	5691	2844	50.03
s15850	71.06	79.42	183	308	68.31	9537	7577	20.55	6142	5001	18.58
s35932	85.98	88.56	40	117	192.5	28958	23942	17.32	23350	18412	21.15
s38417	98.04	98.08	222	420	89.19	24993	15607	37.55	18597	9787	47.37
s38584	90	93.42	284	602	111.97	27329	20039	26.67	16159	12738	21.17
Average	87.08	92.44			84.07			30.9			37.42

average the fault coverage increases by an additional 0.77% for designs with two segments and by about 0.79% for designs with three segments. Furthermore, now the fault coverage is higher for all circuits with segmented scan designs. Additionally the number of tests in T' are less than those in T1 for all circuits. The percentage reduction in peak WSA remains the same as that for T1 test sets. The percentage reduction in average WSA however decreases when T' test sets are used instead of T1 test sets.

Summarizing the results in Tables 1, 2, 7 and 8, we observe that, on average, for the designs using two(three) segments, the fault coverage increases by about 4.8% (5.4%) over that obtained for unsegmented scan designs while reducing the peak WSA and average WSA by 21.64%(30.90%) and 21.59%(37.42%), respectively. The increase in the sizes of the test sets is attributable to higher fault coverages as well as use of tests that cause smaller WSA. However since the unspecified values in the tests are not deterministically filled to reduce WSA the ability to compress test data remains available.

V. Conclusions

In this work we investigated test generation for delay faults in segmented scan designs. We believe this is the first study that has shown using experimental results that segmented scan does not provide only the commonly known benefit of reduced switching activity during test, but also increased delay fault coverage is facilitated. It is hoped that the findings of our research will contribute towards addressing some of the key test challenges in nanometer designs including delay fault test, improved yield through power constrained testing.

References

[1] J. Saxena, K. M. Butler, V. B. Jayaram, et.al., "A Case Study of IR-drop in Structured At-Speed Testing", Proc ITC 2003, pp. 1098 – 1104.

[2] J. Savir, "Skew-Load Transition Test: Part I, Calculus", Proc. ITC 1992, pp. 705-713.

[3] J. Savir and S. Patil, "Broad-Side Delay Test", IEEE TCAD, 1994, pp. 1057-1064.

[4] B. I. Dervisoglu and G. E. Stong, "Design for Testability: Using Scanpath Techniques for Path-Delay Test and Measurement", Proc. ITC 1991, pp.365-374.

[5] S. Bhunia, H. Mahmoodi, D. Ghosh, S. Mukhopadhyaay, K. Roy, "Low-Power Scan Design Using First-Level Supply Gating", IEEE TVLSI , March 2005, pp. 384-395.

[6] S. Gestendorfer and H. J. Wunderlich, "Minimized Power Consumption for Scan-Based BIST", Proc. ITC 1999, pp. 77 – 84.

[7] Y. Bonhomme, P. Girard, L. Guiller, C. Landrault, S. Pravossoudovitch, A. Virazel, " Design of routing-constrained low power scan chains", Proc. DATE 2004, pp. 62-67.

[8] K. Joshi and E. MacDonald, "Reduction of Instantaneous Power by Ripple Scan Clocking," Proc. VTS 2005, pp. 271-276.

[9] R. Sankaralingam and N. A. Touba, "Inserting Test Points to Control Peak Power During Scan Testing", Proc. Intl. Symp. on DFT, 2002, pp. 138 – 146.

[10] S. Sharifi, J. Jaffari, M. Hosseinabady, A. Afsali-Kusha and Z. Navabi, "Simultaneous Reduction of Dynamic and Static Power in Scan Structures", Proc. DATE 2005, pp. 846-851.

[11] V. Dabholkar, S. Chakravarty, I. Pomeranz and S.M. Reddy, "Techniques for Minimizing Power Dissipation in Scan and Combinational Circuits During Test Application," IEEE TCAD 1999, pp. 1325-1333.

[12] X. Liu and M. S. Hsiao, "Constrained ATPG for Broadside Transition Testing", Proc. Intl. Symp. on DFT, 2003, pp. 175 – 182.

[13] I. Pomeranz, "On the Generation of Scan-based Test Sets with Reachable States for Testing under Functional Operation Conditions", Proc. DAC 2004, pp. 928 – 933.

[14] Y.-C. Lin, F. Lu, K. Yang, and K.-T. Cheng, "Constraint Extraction for Pseudo-Functional Scan-based Delay Testing", Proc. ASP-DAC, Jan. 2005, pp. 166 – 171.

[15] X. Wen, Y. Yamashitam, S. Morishima, S. Kajihara, L. T. Wang, K. K. Saluja and K. Kinoshita, "Low-Capture-Power Test Generaion for Scan Based At-Speed Testing", Proc. ITC 2005, pp. 1019-1028.

[16] W. Li, S.M. Reddy and I. Pomeranz,"On Reducing peak

current and power during test," Proc. ISVLSI 2005, pp. 156-161.

[17] L. Whetsel, "Adapting Scan Architectures for Low Power Operation", Proc. ITC 2000, pp. 863-872.

[18] J. Saxena, K.M. Butler and L. Whetsel, "An Analysis of Power Reduction Techniques in Scan Testing," Proc. ITC 2001, pp. 670-677.

[19] P. M. Rosinger, B. M. Al-Hashimi, and N. Nicolici, "Scan Architecture with Mutually Exclusive Scan Segment Activation for Shift and Capture Power Reduction", IEEE TCAD, July 2004, pp. 1142-1153.

[20] K.-J. Lee, S.-J. Hsu and C.-M. Ho, "Test Power Reduction with Multiple Capture Orders", Proc. ATS 2004, pp. 26 – 31.

[21] B. Koenemann, "LFSR-Coded Test Patterns for Scan Designs", Proc.ETC1991, pp. 237-24